DYNAMIC VOLTAGE FREQUENCY SCALING (DVFS) FOR MICROPROCESSORS POWER AND ENERGY REDUCTION

Diary R. Suleiman Muhammed A. Ibrahim Ibrahim I. Hamarash
e-mail: diariy@engineer.com e-mail: ibrahimm@itu.edu.tr e-mail: ibrahim_hamarash@yahoo.com
University of Salahaddin-Hawler, College of Engineering, Department of Electrical Engineering, Erbil, Iraq

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ABSTRACT

This paper presents a methodology for power and energy reduction in general purpose microprocessors, which is known as dynamic voltage frequency scaling (DVFS). The DVFS technique can be considered as an effective mechanism for reducing processor power and energy. In the last decade a lot of works have been done during the hardware and software implementation. In this paper a proposed control loop of DVFS technique has been introduced. SPICE simulation program results confirm the theory.

I. INTRODUCTION

In recent years the processors speed reaches Gigahertz [1], so the power dissipation increases rapidly in a level of the order of ten of Watts and it becomes an important consideration in the design of microprocessors, especially battery-powered portable systems, and emerges as a key technology in the VLSI system design [2].

Processors consume a large portion of energy around 50% of the overall consumed energy of computer systems [3]. Today most digital circuits are constructed using CMOS circuits [4], especially processors, therefore the analysis of power dissipation in CMOS circuits is essential to find out the relation between power, supply voltage, and clock frequency. The power dissipation for CMOS circuits is the summation of dynamic power, static power and short circuit power. These components of power dissipation is as shown in Figure 1 are because of [5],

$P_{dynamic}$ which is due to charging and discharging capacitors (1).
P_{static} which is due to reverse biased diodes (2).
$P_{shortcircuit}$ which is due to switching direct path between V_{dd}-GND (3).

Mathematically,

$$P_{cmos} = P_{dynamic} + P_{static} + P_{shortcircuit} \quad (1)$$

The dynamic power is the main portion of the CMOS power dissipation [5]. It can be expressed as:

$$P_{dynmaic} \alpha C_L V_{dd}^2 f_{clk} \quad (2)$$

Where C_L is the collective switching capacitance, V_{dd} is the supply voltage, and f_{clk} is the clock frequency.

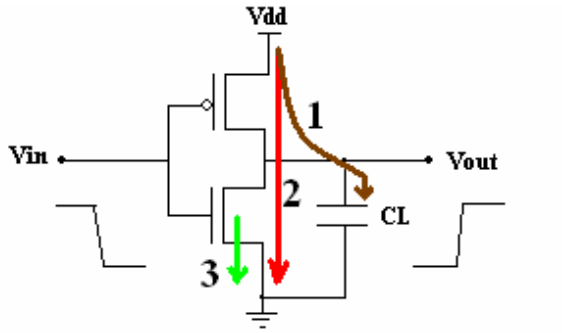

Figure 1. Power dissipation for a simple CMOS inverter

The high power dissipation of a processor has at least the following disadvantages:

- High power systems tend to run hot, that causes the processor and other system components to fail. The failure rate of a processor are doubles every 10°C increase [5].
- It complicates the cooling solutions of integrated circuits for heat removal, and thus increase the production cost. Intel estimates that more than 1$/W per processor chip will be added once the processor power dissipation exceeds 35-40 W [6].
- It increases the operation costs; such as the electricity bills for air conditioning of the computer and system rooms. 8% of US electricity in 1998 was attributed to the internet, growing to about 30% by 2020 [7].
- It shortens the battery or UPS life. The processor power doubles every four years, consequently the average battery or UPS life will be shortened [8].

- It endangers the human body. Current high performance processors consume around 70-100W [7].

The major processor manufactures (Intel) has announced that the processor power dissipation doubles every four years [7], therefore dynamic voltage frequency scaling technique, by lowering the supply voltage, is effective in reducing power dissipation. Lowering the supply voltage restricts the operating frequency accordingly because,

$$(f_{clk} \ \alpha \ (V_{dd} - V_t)^2 / V_{dd}) \qquad (3)$$

Where V_t is the CMOS threshold voltage.
Meaning that changes in frequency are accompanied by appropriate adjustment in voltage.
The energy consumption of a program can be reduced by: reducing the number of operation performed, reducing the switching capacitance of each operation, or by reducing the voltage at which these operations are performed [9].

There has been a significant amount of research relating to hardware support for dynamic voltage frequency scaling. T. Burd presented a voltage scaling hardware loop [2]. Tiware et. al. presented a hardware technique for shutting down unused hardware modules [6]. Throughout this paper a new dynamic voltage frequency scaling (DVFS) control loop is presented which has a high performance due to its accuracy in progress.

II. ANALYSIS OF DVFS TECHNIQUE

Dynamic voltage frequency scaling (DVFS) is accepted as a technique to reduce power and energy consumption of microprocessors [7]. Lowering only the operating frequency f_{clk} can reduce the power consumption but the energy consumption remains the same because the computation needs more time to finish. Lowering the supply voltage V_{dd} can reduce a significant amount of energy because of the quadratic relation between power and V_{dd} as given in Equation 2. Lowering the supply voltage and operating frequency reduces the power and energy consumption further. Figure 2 shows the power saving achievable by using variable V_{dd}.

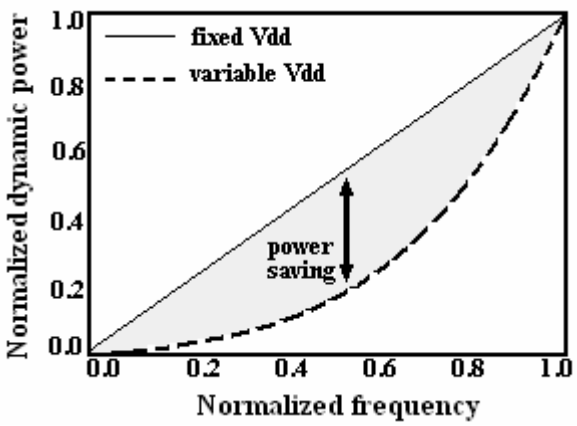

Figure 2. Power saving achievable by Using variable Vdd

When the clock frequency f_{clk} is reduced by half, this lowers the processor's power consumption and still allows task to complete by deadline, the energy consumption remains the same. Reducing the voltage level V_{dd} by half reduces the power level further without any corresponding increase in execution time. As a result the energy consumption is reduced significantly, but the appropriate performance is remained [10]. This is shown in Figure 3:

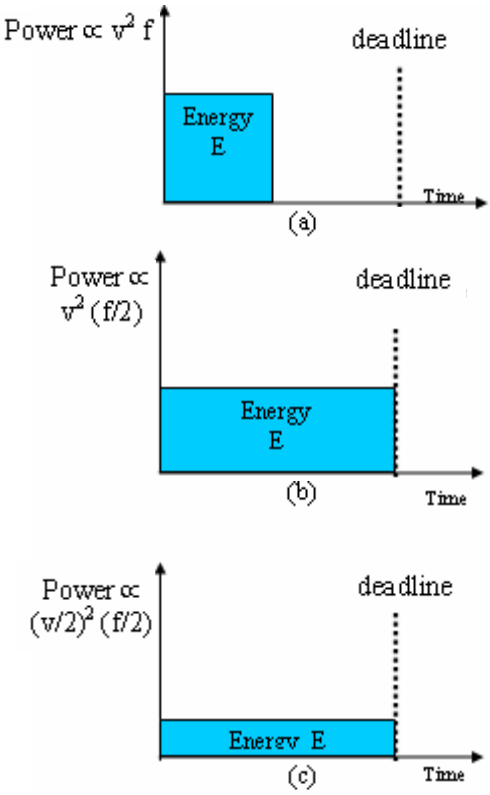

Figure 3. Energy consumption vs. power consumption for a task, which is ready at 0 and complete at T, with maximum clock frequency f_{clk}

There are three key components for implementing DVFS technique in processors [7,10]:
1. An operating system which intelligently vary the processor speed.
2. A control loop which generates the voltage required for the desired speed.
3. A microprocessor which operates over a range of voltages.
The relationship between these three components is shown in Figure 4.

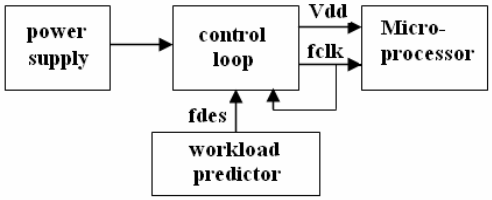

Figure 4. DVFS required components

III. WORKLOAD PREDICTION

To perform this multi-speed functionality of a processor the modern operating system will intelligently vary the processor speed by predict and estimate the future workload of the processor and convert it to a digital word (f_{des}) and save it into a register, whose value is then used by the control loop to adjust the processor clock frequency (f_{clk}) with the voltage level (V_{dd})[11].

Figure 5, shows a typical workload pattern with a sequence of tasks and deadlines between the tasks. By scaling down the voltage, each task is extended into the idle time after it, as shown in Figure 6:

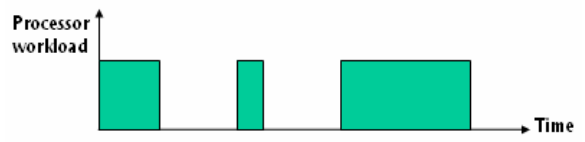

Figure 5. A typical workload pattern with tasks and idle time between tasks.

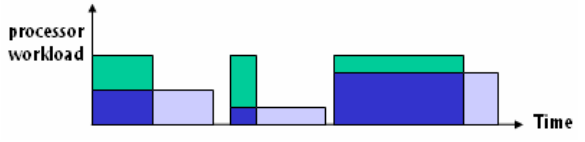

Figure 6. A typical workload pattern with DVFS technique

A processor usually goes to sleep as a result of certain special instruction, and then it is woken up by certain interrupts, this cause producing idle intervals between the tasks [11]. Therefore, work load of the processor usually consists of sequence of tasks and idles between tasks. By scaling down the voltage and frequency each task is extended into the idle time after it. As long as the tasks do not overlap, the dynamic voltage frequency scaling (DVFS) technique is guaranteed to be correct.

Before design the DVFS technique it is essential to model the workload. The concept of an event makes partitioning the workload to be possible. Two parameters, α and β as shown in figure 7, are used to describe an event; both in the unit of time, α measures the length of an event and β measures the length of an event plus idle time before the next event starts. It follows that utilization can be determined by dividing α by β. For example if utilization is 50 percent, it means that this particular event has the potential to be scaled down by a factor of two [11,12].

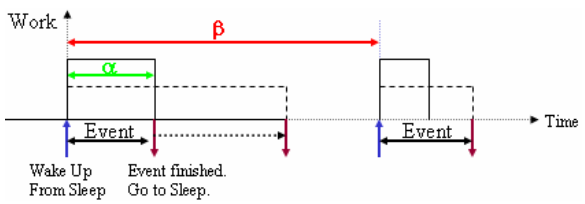

Figure 7: Modelling the workload with DVFS (ideal case)

IV. THE PROPOSED DVFS CONTROL LOOP

A control loop, shown in Figure 8 is proposed in this paper to carry out the appropriate voltage via the frequency.

The operation of this control loop is depending on the difference between the clock frequency f_{clk} from VCO and f_{des} from the operating system predictor, where the output of the VCO, f_{clk}, clocks a counter which is reset at 1MHz intervals. This provides a digital word f_{meas}, and it saved in a register. This value is subtracted from the desired clock frequency f_{des} (which is predicted by the operating system as a digital word and saved in a register) to generate an error frequency value, f_{err}, and is saved in another register. This register has to have an additional bit than the other registers to indicate the sign. This error word will be converted to voltage levels via a digital circuit. The voltage levels are converted to a DC voltage by digital to analog converter (DAC) to be used by a comparator to generate a PWM pulses and then to drive the DC-DC converter.

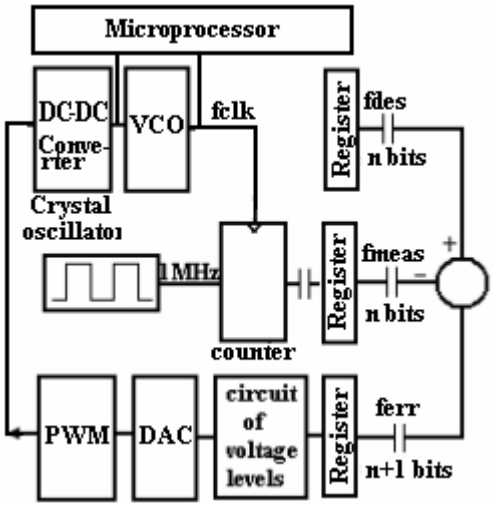

Figure 8. A proposed DVFS control loop

The feed back loop sets V_{dd} to make f_{err} zero The DC-DC converter converts the output DC voltage to a level depending on the incoming pulses from PWM in the control loop. The VCO (ring oscillator) converts the output of the DC-DC converter to a clock frequency. The DC-DC converter output with the generated clock frequency is fed to the processor.

The proposed DVFS control loop has been simulated Using Pspice simulator program. The following waveforms are obtained.

For f_{clk}=500 MHz and f_{des}=300MHz, the input and output voltages of PWM, DC-DC converter, and VCO signals are shown in the Figure 9,10, and 11respectively.

Also, for f_{clk}=300 MHz and f_{des}=500MHz, the input and output voltages of PWM, DC-DC converter, and VCO signals are shown in the Figure 12,13, and 14 respectively.

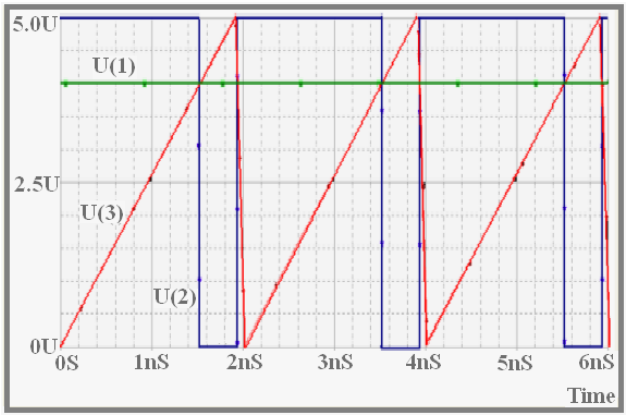

Figure 9. The PWM input (V1), output (V2), and sawtooth signal (V3) for f_{clk}=500 MHz and f_{des}=300MHz.

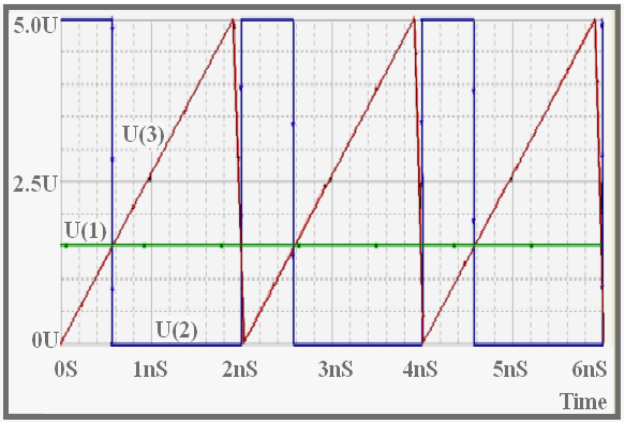

Figure 12. The PWM input (V1), output (V2), and sawtooth signal (V3) for f_{clk}=300 MHz and f_{des}=500MHz

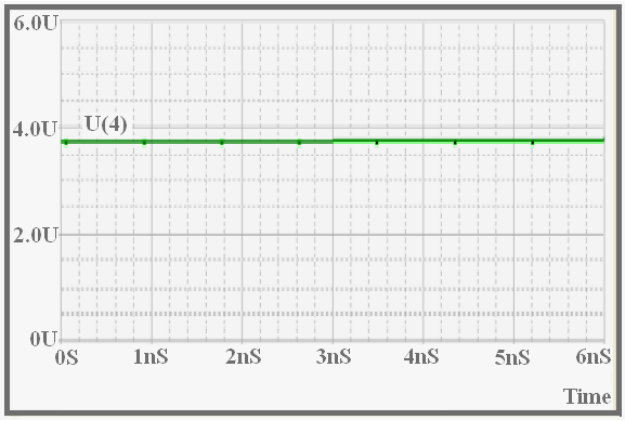

Figure 10. The DC-DC converter output voltage (V4) for f_{clk}=500 MHz and f_{des}=300MHz

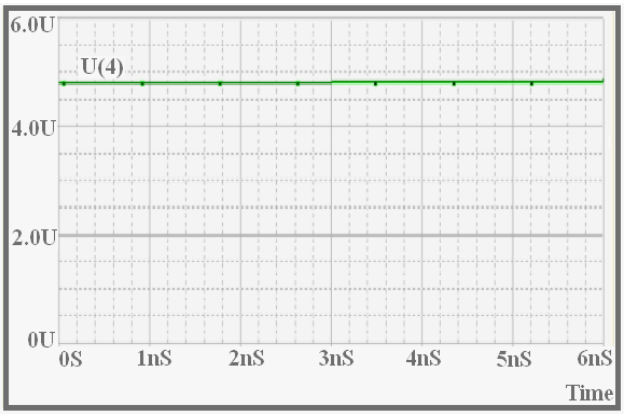

Figure 13. The DC-DC converter output voltage (V4) for f_{clk}=300 MHz and f_{des}=500MHz

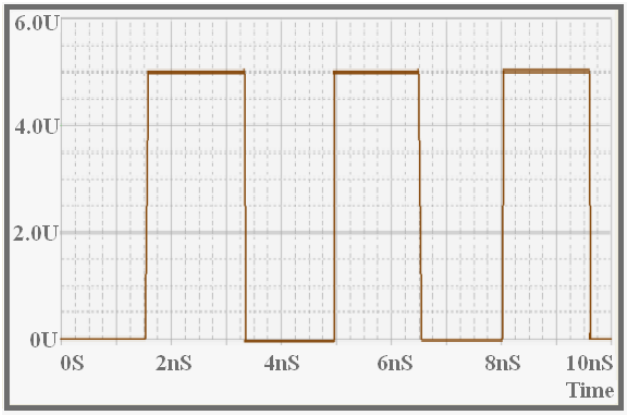

Figure 11. The VCO output signal for f_{clk}=500 MHz and f_{des}=300MHz

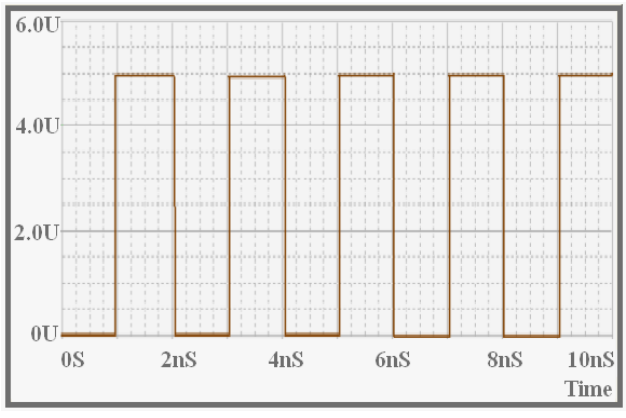

Figure 14. The VCO output signal for f_{clk}=300 MHz and f_{des}=500MH

V. CONCLUSION

The proposed dynamic voltage frequency scaling (DVFS) loop, which is introduced throughout this work, is to vary or set the supply voltage V_{dd} and operating frequency f_{clk} according to the desired frequency f_{des} which is predicted via the operating system and speed control circuit.

The DVFS proposed loop has a high performance due to accuracy in progress, and can significantly improve processor energy efficiency especially for general purpose microprocessors, multimedia interface systems, and battery or UPS powered electronic devices.

The presented technique can decreases the processors average energy consumption at runtime depending on the applications and the limit of the supply voltage V_{dd}.

Therefore, this proposed DVFS technique can be considered as a critical constraint for the current and future processor's performance.

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