

A NEW LOW DISTORTION ANALOG MULTIPLIER

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ABSTRACT

A new method has been proposed to reduce the mobility degradation effect on square-law characteristic of the MOS transistor. This method has been applied to an analog multiplier to form a new low distortion multiplier circuit. This analog multiplier operates with $\pm 5V$ power supply. The operating range for each input is $\pm 3V$. In this operating range the nonlinearity for V_x is 0.6% and for V_y is 0.5%. The 3dB bandwidth is specified for V_x as 33MHz and for V_y as 34MHz, respectively.

I. INTRODUCTION

Analog multipliers are the key elements of signal processing circuits. There are several techniques of implementing four quadrant multipliers including techniques based on square-law characteristic of the MOS transistor operating in the saturation region. Several second order effects influencing the linearity of multiplier circuits are reported in the literature [1-7]. Mobility degradation caused by short channel effect is the most important factor which degrades the linearity of this kind of multipliers. Although there are several analog multiplier circuits [1-7] based on square-law characteristic of MOS transistor, in none of them any special precaution has been introduced to reduce the short channel effect. In this work a new method has been proposed for reducing the mobility degradation effect on square-law characteristic of the MOS transistor. This method has been applied to an analog multiplier [1] to form a new low distortion multiplier circuit. This analog multiplier operates with $\pm 5V$ power supply. The operating range for each input is $\pm 3V$. In this operating range the nonlinearity for V_x is 0.6% and for V_y is 0.5%. The 3dB bandwidth is specified for V_x as 33MHz and for V_y as 34MHz, respectively.

II. METHOD TO REDUCE THE SHORT CHANNEL EFFECT

The method for linearization of the square-law characteristic of MOS transistor is shown in the circuits of Figure-1a and Figure-1b. T3 is the main squaring transistor in Figure-1a and Figure-1b. T1, T2, R and current mirror CM in Figure-1a and T1, T2, R in Figure-1b realize Eq.(1).

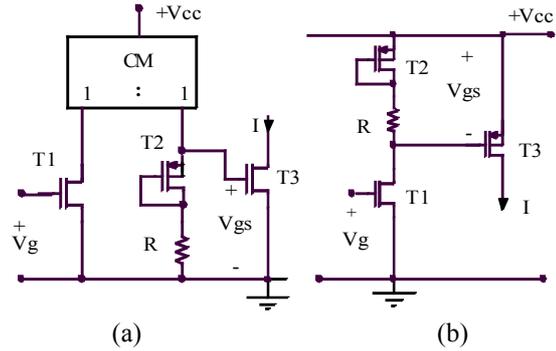


Figure-1. Linearization of the square-law characteristic of MOS transistor

$$V_{gs} = V_g + k(V_g - V_T)^2 \quad (1)$$

Since mobility degradation of NMOS transistor is less than that of the PMOS transistor, the circuit in Figure-1a has been used in proposed multiplier circuit.

By a proper choice of k in Eq.(1) squaring error can be minimized. The drain current I of T3 of in Figure-1a can be expressed as

$$I = \frac{\beta}{2} \frac{(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)} \quad (2)$$

where θ parameter models the short channel effect in SPICE LEVEL-3 Model.

Using Eq.(1) and Eq.(2), we can get

$$I = \frac{\beta}{2} V_x^2 \frac{1 + 2kV_x + k^2V_x^2}{1 + \theta V_x + \theta kV_x^2} \quad (3)$$

where V_x is defined as

$$V_x = V_g - V_T \quad (4)$$

Assuming $k = n\theta$ and choosing $n = 1/2$ Eq.(3) converts to

$$I = \frac{\beta}{2} V_x^2 \frac{1 + \theta V_x + (\theta^2/4)V_x^2}{1 + \theta V_x + (\theta^2/2)V_x^2} \quad (5)$$

Since $\theta \ll 1$ we can easily omit θ^2 and we get from Eq.(5)

$$I \approx \frac{\beta}{2} V_x^2 \quad (6)$$

The main factor that degrades the operation of the circuit in Figure-1a and Figure-1b is the short channel effect of T1 and T2, which are modeled with θ_1 and θ_2 , respectively. The expression of V_{gs} including θ_1 , θ_2 for $\beta_1=\beta_2=\beta$ is shown in Eq.(7) where k is defined in Eq.(8).

$$V_{gs} = V_g + k \frac{(V_g - V_T)^2}{1 + \theta_1(V_g - V_T)} \quad (7)$$

$$k = \frac{\beta}{2} \left(R + \frac{\theta_2}{\beta} - \frac{\theta_1}{\beta} \right) \quad (8)$$

For $\theta_1=\theta$ and $k=n\theta$, the full equation of the drain current I defined by

$$I = \frac{\beta}{2} V_x^2 \cdot E \quad (9)$$

where $V_x = V_g - V_T$ and E is expressed as

$$E = \frac{(1 + \theta(1+n)V_x + \theta^2(1+n)^2V_x^2)}{(1 + \theta V_x)(1 + 2\theta V_x + \theta^2(1+n)V_x^2)} \quad (10)$$

To show the effect of the quantity n on linearization, relative error function $E-1$ is drawn in Figure-2 for $\theta=0.3$.

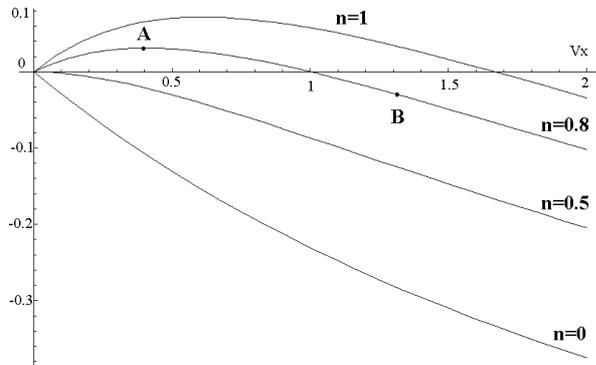


Figure-2. Relative errors of $E-1$ for several n ($\theta=0.3$)

For $n=0$ the circuit behaves as described in Eq.(2). Increasing n also reduces the relative error. In point A the maximum relative error becomes e and in point B ($V_x=V_{xm}$) the relative error becomes $-e$. Using the properties of these points, the maximum input range V_{xm} for a given relative error $|h|$ can be derived from Eq.(10) as

$$V_{xm} \approx \frac{\sqrt{8e} + 3e + \sqrt{e(16 + 12\sqrt{2e} + e)}}{4\theta(1-e)} \quad (11)$$

where $e = |h|$. In that case, n must be chosen as

$$n \approx \frac{1 + \sqrt{8e}}{2} \quad (12)$$

To obtain the required n , R and β must be chosen according to Eq.(8) where $k=n\theta$.

III. THE CONCEPT OF THE MULTIPLIER CIRCUIT

In the proposed analog multiplier [1], circuit in Figure-3 has been taken into consideration but transistors T1, T2, T3 and T4 are replaced with circuit in Figure-1a. An adequate value of k is selected to minimize the harmonic distortion.

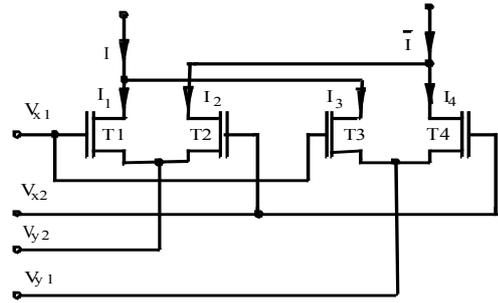


Figure-3. Conventional multiplier circuit

Using Eq.(2) and considering short channel effect for each of the transistor in Figure-3, the output current $I_o = I_1 - I_2 - (I_3 - I_4)$ can be expressed as

$$I_o = \frac{\beta V_{DX} V_{DY} a}{a^4 - a^2 \frac{\theta^2}{2} (V_{DX}^2 + V_{DY}^2) + \frac{\theta^4}{16} (V_{DX}^2 - V_{DY}^2)^2} \quad (13)$$

where $V_{DX}, V_{DY}, V_{CX}, V_{CY}$ and are defined as

$$V_{X1} - V_{X2} = V_{DX}, \quad V_{Y2} - V_{Y1} = V_{DY}, \quad V_{X1} + V_{X2} = V_{CX} \quad (14)$$

$$V_{Y1} + V_{Y2} = V_{CY}, \quad a = 1 + \theta / 2(V_{CX} - V_{CY} - 2V_T)$$

Ignoring θ in Eq.(13), ideal multiplication formula is obtained as

$$I_o = I_o = B \cdot V_{DX} \cdot V_{DY} \quad (15)$$

Ignoring θ^4 in the denominator, the serial expansion of Eq.(13) will be

$$I_o = \beta V_{DX} V_{DY} \frac{1}{a^3} \left[1 + \frac{\theta^2}{2a^3} (V_{DX}^2 + V_{DY}^2) + \frac{\theta^4}{4a^4} (V_{DX}^2 + V_{DY}^2)^2 + \frac{\theta^6}{8a^6} (V_{DX}^2 + V_{DY}^2)^4 + \dots \right] \quad (16)$$

It can be clearly seen that the harmonic distortion is produced by high-order components of V_{DX} and V_{DY} caused by θ .

Eq.(9) is valid for each transistor in the proposed circuit. Neglecting θ^2 in the parentheses of the numerator and the denominator of Eq.(10) we can get Eq.(17) and Eq.(18).

$$I \approx \frac{\beta}{2} V_x^2 \frac{1 + 2\theta(1+n)V_x}{(1+\theta V_x)(1+2\theta V_x)} \quad (17)$$

$$\approx \frac{\beta}{2} V_x^2 \left[\frac{(1+2n)}{(1+\theta V_x)} - \frac{2n}{(1+2\theta V_x)} \right] \quad (18)$$

At this point utilizing Eq.(18) for each transistor, the new multiplication equation can be obtained as

$$I = \beta V_{DX} V_{DY} \left[\frac{1+2n}{a^3 - a \frac{\theta^2}{2} z} - \frac{2n}{b^3 - 2b\theta^2 z} \right] \quad (19)$$

where a, b, z are defined by

$$a = 1 + \theta / 2 (V_{CX} - V_{CY} - 2V_T) \quad (20)$$

$$b = 1 + \theta (V_{CX} - V_{CY} - 2V_T)$$

$$z = V_{DX}^2 + V_{DY}^2$$

The serial expansion of Eq.(19) gives

$$I_o = \beta V_{DX} V_{DY} \left[\frac{1+2n}{a^3} - \frac{2n}{b^3} + \theta^2 \left(\frac{1+2n}{2a^5} - \frac{8n}{2b^5} \right) (V_{DX}^2 + V_{DY}^2) + \theta^4 \left(\frac{1+2n}{4a^7} - \frac{32n}{4b^7} \right) (V_{DX}^2 + V_{DY}^2)^2 \dots \right] \quad (21)$$

It is clearly seen that the third harmonic distortion created by V_{DX}^2 and V_{DY}^2 in the parenthesis can be cancelled selecting n as

$$n = \frac{b^5}{8a^5 - 2b^5} \quad (22)$$

Since $\theta < 1$, then $a \approx 1$ and $b \approx 1$. So Eq.(22) yields 1/6. This shows that the new circuit makes it possible to minimize the distortion by controlling n via $k(k=n\theta)$.

IV. DESCRIPTION OF THE HIGH LINEARITY ANALOG MULTIPLIER

The complete multiplier circuit is illustrated in Figure-4. The output current I_o is produced from the current I and \bar{I} by the output stage given in Figure-5. The inputs voltages V_{X1} , V_{X2} , V_{Y1} and V_{Y2} are generated from active attenuator circuit shown in Figure-6. The subcircuits composed of M17-M22 and CM1, M23-M28 and CM2, M29-M34 and CM3, M35-M40 and CM4, operate like the circuit in Figure-1a. M20, M26, M32 and M37 operate in triode region to simulate the resistor R shown in Figure-1a. M17, M21, M23, M27, M29, M33, M35 and M40 have larger aspect ratios than that of the transistors M18, M22, M24, M28, M30, M34, M36 and M39 to allow them operating in saturation region. For this reason, the channel length modulation of the M18, M22, M24, M28, M30, M34, M36, M39 on multiplication process is reduced. On the other hand M41 and M42 provide the bias of the transistors M18, M28, M30 and M39 so that $V_{GS} - V_T > 0$ is obtained for M18, M28, M30 and M39 in full operating range of V_{DX} and V_{DY} . The subcircuits consisting of M43, M44, Ic3 and M45, M46, Ic4 form two buffers; one between M18, M30 and V_{y2} the other between M28, M39 and V_{y1} .

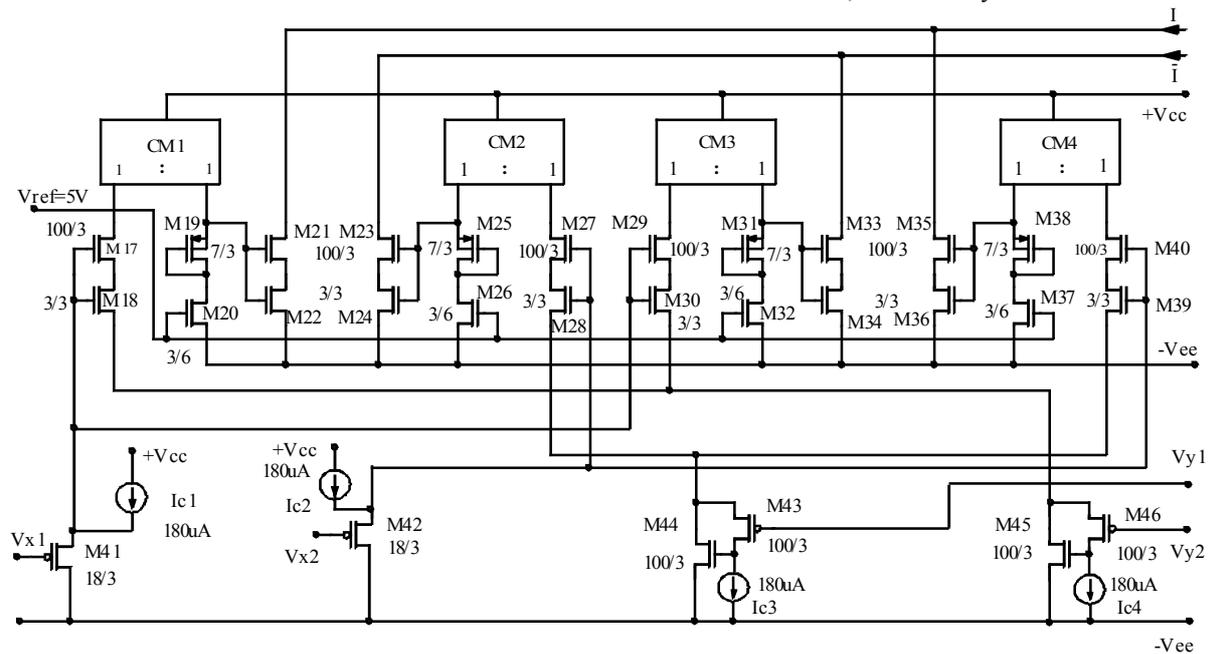


Figure-4. The high-linearity analog multiplier

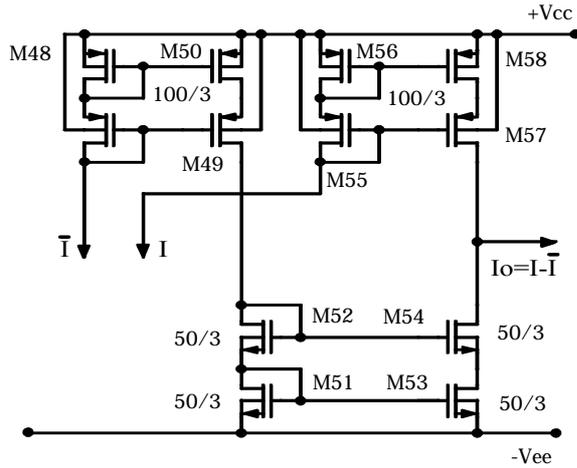


Figure-5. The output circuit

V. ACTIVE ATTENUATOR CIRCUIT

Active attenuator circuit has been discussed in [8]. This circuit generates V_{X1} , V_{X2} , V_{Y1} , and V_{Y2} so that we obtain $V_{X1} - V_{X2} = K(V_x - \bar{V}_x)$, $V_{Y1} - V_{Y2} = K(V_y - \bar{V}_y)$. They not only reduce distortion but also make the voltages V_{X1} , V_{X2} and V_{Y1} , V_{Y2} independent from input bias conditions. Active attenuator circuit X is shown in Figure-6. Active attenuator circuit Y is the same but only transistor numbers are between M9-M16. In Figure-6 transistors M1-M4 form a differential pair. Aspect ratio of M3 and M4 are chosen sufficient large to allow M1 and M2 operating in saturation region. In this case, conductance of the differential pair is determined by M1 and M2 but the output impedance of circuit becomes much larger than conventional differential pair. On the other hand M7 and M8 are operating in triode region and simulate resistor R_d . This resistor R_d is used to cancel the distortion caused by the short channel effects of the transistors.

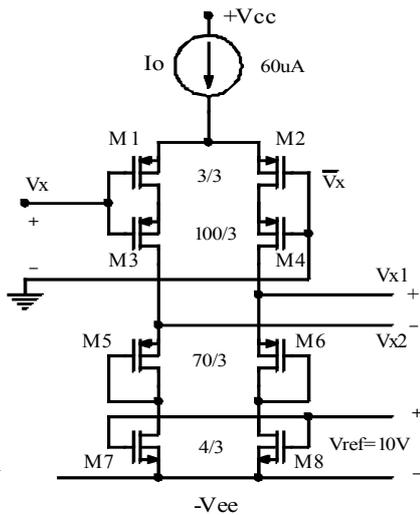


Figure-6. Active attenuator for the inputs X and Y

This resistor R_d is defined as

$$R_d = \theta \left(\frac{1}{\sqrt{\beta_1 \beta_2}} - \frac{1}{\beta_2} \right) \quad (23)$$

where β_1 is the conductance of M1, M2 and β_2 is the conductance of M5, M6 and θ is the short channel effect of PMOS.

For R_d specified in Eq.(23) attenuations for inputs X and Y are defined by

$$V_{X2} - V_{X1} = \sqrt{\left(\frac{\beta_1}{\beta_2} \right)} (V_x - \bar{V}_x) \quad (24)$$

$$V_{Y2} - V_{Y1} = \sqrt{\left(\frac{\beta_1}{\beta_2} \right)} (V_y - \bar{V}_y) \quad (25)$$

To obtain a required value R_d , conductance of M7 and M8 must be selected as

$$\beta_{78} = \frac{1}{R_d (V_{ref} - V_T)} \quad (26)$$

VI. SIMULATIONS

In the simulation SPICE Level-3 parameters of TUBITAK 3 μ process are used. The circuit is supplied with $\pm 5V$. Input ranges of X and Y is $\pm 3V$. The simulated resistors R and R_d described above are chosen as 11K Ω and 5K Ω , respectively. To get a comparison, simulations are performed for optimized case ($k = k_{opt} = 1/6$) providing minimum distortion and for nonoptimized case ($k = 0$) where the circuit behaves similar to multiplier in Figure-3. Figure-7 shows several $I_o - V_x$ curves obtained by taking V_y as parameter in the optimized case and Figure-8 shows linearity errors of the curves in Figure-7. On the other hand Figure-9 shows several $I_o - V_x$ curves for obtained by taking V_x as parameter in the nonoptimized case and Figure-10 shows the linearity errors of the curves in Figure-8. In the optimized case linearity error becomes 0.6% whereas 15% for the nonoptimized case. The circuit is also tested by applying 100KHz sinusoidal signal with 6Vpp. The total harmonic distortion has been determined as 0.2% for the optimized case whereas 1% for the nonoptimized case. Similar results have been also observed for input V_y under the same simulation conditions. In this case total linearity error is 0.5% for the optimized condition and 8% for the nonoptimized condition. On the other hand total harmonic distortion is 0.2% for optimized case and 0.7% for nonoptimized case. The $-3dB$ frequency bandwidth of inputs X and Y are 33MHz and 34MHz, respectively. The results show that the proposed linearization method is robust. Other important property of the circuit is that an external control on distortion can be made by changing V_{ref} in Figure-3.

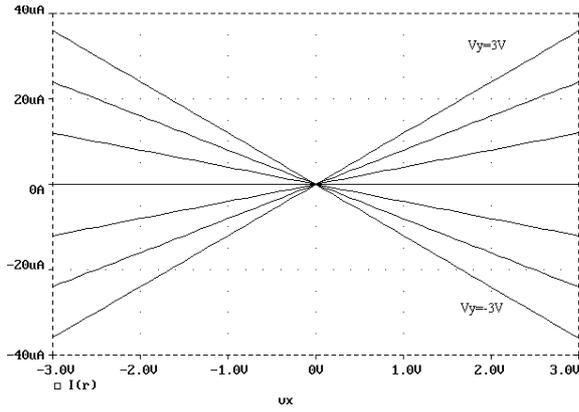


Figure-7. Io-Vx curves for $k=k_{opt}$

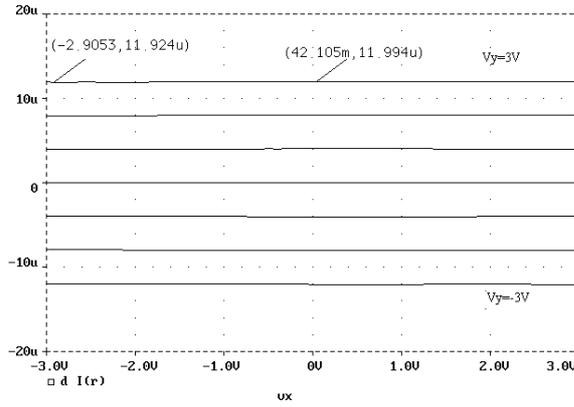


Figure-8. Error performances of the curves in Figure-7

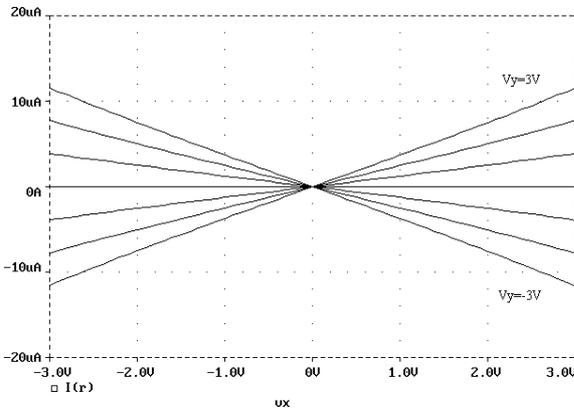


Figure-9. Io-Vx curves for $k=0$

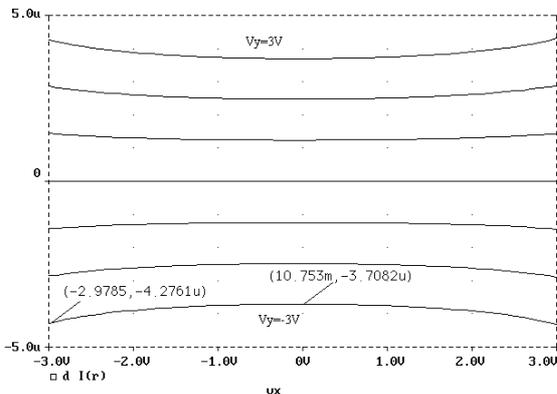


Figure-10. Error performances of the curves in Figure-9

VII. CONCLUSION

A new method has been proposed to reduce the mobility degradation effect on square-law characteristic of MOS transistor. This method has been applied to an analog multiplier to form a new low harmonic distortion multiplier circuit. This analog multiplier operates with $\pm 5V$ power supply. The operating range for each input is $\pm 3V$. In this operating range the nonlinearity for V_x is 0.6% and for V_y is 0.5%. The 3dB bandwidth is specified for V_x as 33MHz and for V_y as 34MHz, respectively. The multiplier topology proposed allows external adjustment of the distortion which can be considered as another important property of the circuit. The simulation results show that the new method is effective for reducing distortion.

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