

# EXPERIMENTAL SETUP FOR A DSP BASED SINGLE-PHASE PWM INVERTER

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## ABSTRACT

**The design and analysis of an experimental study on Digital Signal Processor (DSP) controlled single-phase Pulse Width Modulation (PWM) inverter are presented in this paper. The study also aims to enhance undergraduates' knowledge on experimental studies in the laboratory. The performance of the DSP based PWM inverter design is analyzed through the simulation studies under various switching frequencies and the results are validated through the experimental setup based on TMS320 F2812 DSP board.**

## I. INTRODUCTION

PWM control is the most powerful technique that offers a simple method for controlling of analog systems with the processor's digital output [1]. With the availability of low cost high performance DSP chips characterized by the execution of most instructions in one instruction cycle, complicated control algorithms can be executed with fast speed, making very high sampling rate possible for digitally-controlled inverters [2].

Texas Instruments TMS320 F2812 DSP is best suited to this study for DSP based application development and is used to generate PWM signals for single-phase inverter. The control algorithm is developed in Matlab/Simulink using block diagrams, the code is generated with RTW and compiled, debugged and transferred to DSP board in Code Composer Studio (CCS).

It is observed that a large number of references in the literature, even in educational articles, usually do not give the subject in detail and further reading is required for clear understanding. In references [1], [2] and [3] basic DSP commands and the hardware installation procedures are not mentioned in detail. In [4], the basics of RTW and the hardware features are comprehensively included but DSP controller commands and file system interface are not included. The paper presents the detailed design of a digitally controlled single-phase PWM inverter and DSP code generation process..

## II. PROPOSED SYSTEM CONFIGURATION

The proposed system consists of a PC, an eZdsp F2812 DSP board, a full bridge single phase IGBT inverter circuit, a passive filter circuit, a linear load, adjustable DC sources and measurement devices.

In this study the following subjects are presented in detail to make the proposed study more clearer for students.

- Special DSP instructions, coordination and synchronization of control algorithms
- Matlab to DSP interface
- Setting RTW options and managing CCS files
- PWM signal generation with different carrier frequencies
- Configuration of DSP board and IGBT driver circuit
- Experimental implementation and circuit design tricks

## III. DIGITAL SIGNAL PROCESSOR

In the study, eZdsp F2812 DSP board is used for PWM control application [5]. The application of the PWM algorithm requires a time reference, a comparison mechanism and digital outputs. Event Manager Modules of the DSP have the General Purpose (GP) Timer that can be used as time reference, Full Compare/PWM Units as a comparison mechanism and have dedicated digital PWM outputs. The principles of Event Manager Modules and PWM signal generation process are comprehensively described in the following sections.

There are two event manager modules in TMS320 F2812 called EVA and EVB. TMS320 F2812 has six independent pairs of PWM outputs: three of which are controlled by EVA and the other three are controlled by EVB [5]. In the study, GP Timers, Full Compare/PWM Units and PWM outputs are used to generate the gating pulse for the power circuit.

There are two general purpose (GP) timers that can work independently from each other. GP Timer1 and 2 are controlled by EVA, GP Timer3 and 4 are controlled by

EVB. These timers are used to provide a time base for the operation of compare units and associated PWM circuits to generate the PWM outputs [5]. Each GP Timer has up-down counter TxCNT, compare register TxCMPR, period register TxPR, control register TxCON and direction input TDIRx registers. The simplified block diagram of GP Timer is shown in Figure 1.

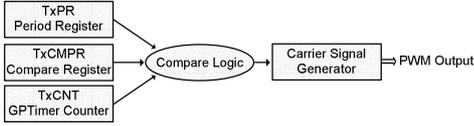


Figure 1. PWM signal generation using EV

There are six compare units: three of which are in EVA module and the other three are in EVB module. These registers depend on the associated GP Timers to generate PWM signals. The generation of PWM patterns comprises the following steps: counting mode, GP Timer compare operation and carrier signal generation. Details of each step are mentioned below. There are two counting modes, controlled by the content of TxCON register, that can be applicable to generate the carrier signal: continuous count up mode results in asymmetric and continuous count up-down mode results in symmetric carrier waveform. The timer values are incremented by one for each GP Timer clock pulse. Figure 2 shows the counting modes that can be used [6].

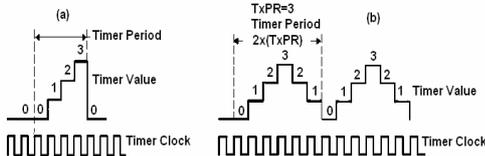


Figure 2. a) asymmetric mode, b) symmetric mode

Each GP Timer has a compare register TxCMPR and an output pin TxPWM. During each timer period, the carrier signal is compared with the value stored in the compare register TxCMPR, the + sign in Figure 3 represents the compare matches. Before the first match, PWMx+1 is logic zero and PWMx is logic one and the value of the compare register is greater than the value of the carrier signal. Between the first and second compare matches, the value stored in the compare register is smaller than the value of carrier signal, as a result of this, the PWM outputs change their states (PWMx+1 is logic one, PWMx is logic zero).

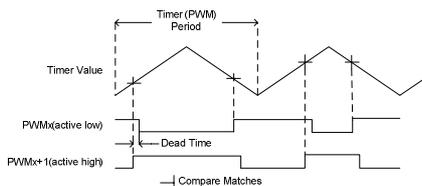


Figure 3. Symmetric PWM generation with compare units

The frequency of the carrier signal depends on the GP Timer period. The oscillator signal XCLKIN is scaled several times to obtain GP Timer clock. The crystal oscillator generates a signal at 30-MHz (XCLKIN). Figure 4 shows the block diagram of GP Timer frequency determination.

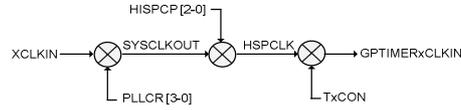


Figure 4. Determination of GP Timer frequency

The period and frequency of the carrier signal are defined as:

$$T_c = \frac{2 * (\text{Amplitude of carrier signal})}{GPTimer * CLKIN} \quad (1)$$

As an instance, it is desired to get a 2-KHz carrier signal in symmetric form. It's period is calculated as  $T_c = 1/2\text{-KHz} = 500 \mu\text{s}$ . XCLKIN is 30-MHz. Using the default value of PLLCR[3-0], SYSCLKOUT becomes 150-MHz. Letting HISPCCP[2-0] to be  $(011)_2 = 3$ , then HSPCLK clock becomes  $\text{SYSCLKOUT}/6 = 25\text{MHz}$ . Adjusting T1CON[10-8] to be  $(000)_2$ , GPTIMER1CLKIN equals  $\text{HSPCLK} = 25 \text{ MHz}$ . According to carrier signal period and frequency equations  $T_c$  is computed as:

$$T_c = \text{Amplitude} * 2 * 40 \text{ ns} \quad (2)$$

The resulting amplitude is 6250. To get 2-KHz carrier signal the following parameters should be adjusted: PLLCR[3-0] = 10, HISPCCP[2-0]=3, T1CON[10-8] = 0, T1PR = 6250

### III. CODE GENERATION PROCESS

In this study, the single-phase PWM inverter controller model is developed in Matlab/Simulink and experiments are performed by using DSP board including interfaces.

Figure 5 illustrates the simulink model for PWM inverter controller. The model consists of a sine wave block, a data type conversion unit, C28x PWM and F2812 eZdsp board. The sine wave block provides a sine reference signal of the same frequency, amplitude and phase as that of the signal of interest. The sine wave generates signal in double data type and data type conversion is needed due to F2812 eZdsp works with uint16 (unsigned integer 16) data type.

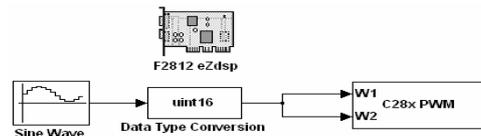


Figure 5. Matlab/Simulink model

C28x PWM generates the PWM signals by comparing the sine wave with a carrier signal and configures the EV modules. This block enables us to activate one of the event manager modules EVA or EVB to generate the carrier signal waveforms. The properties of C28x PWM block are as follows:

- W1: PWM1= Active High, PWM2= Active Low
- W2: PWM3= Active High, PWM4= Active Low

Waveform period (T1PR) is set to 6250 and the waveform type to symmetric. Waveform period also shows the amplitude of the carrier signal. The value of the sine wave must be 6250 (peak to peak, uint16). It is known that the carrier signal is always positive, so the sine wave must be always positive too. To satisfy these conditions, the amplitude of the sine wave is set to 6250/2 with an offset 6250/2 .

### RUNNING THE SOFTWARE

To generate the C code, click the “Build” button of Simulink from the Simulation → Configuration parameters, RTW generates the source code of the model. The generated code from RTW should be compiled in CCS and the compiled code should be loaded to DSP by CCS.

The generated code by RTW is loaded to CCS. The generated code is loaded to CCS but it is not compiled. From “Project” menu by clicking “Rebuild All” (Project>Rebuild All), all of the generated project codes can be compiled. After compiling the source codes and “projectname.out” file is generated, program must be loaded to DSP. From “File” menu by clicking “Load Program”, the “projectname.out” file can be loaded to DSP.

From “Debug” menu, click on “Run” button to run the program. As mentioned before, to get a 2-KHz carrier signal, HISPCP must be set to 3. All other registers must stay with their default value. From (GEL>Watch Clocking and Low-Power Registers) HISPCP register can be changed to 3. Registers or any variables in the program can be observed from the “Watch Window” menu (Right Bottom). For example, generated sine wave is drawn graphically in Figure 6.

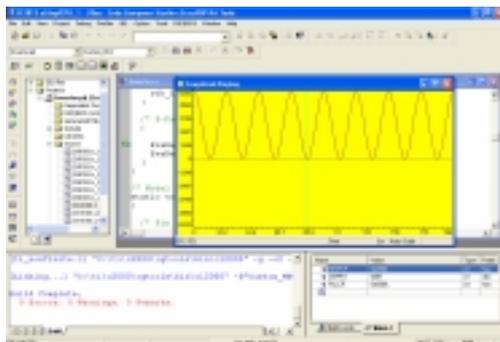


Figure 6. Graph of reference signal and watch window

It can be seen that the maximum value of signal is 6250 and it never decreases below zero. The signal is compared with carrier signal and according to the result, PWM1, PWM2, PWM3 and PWM4 outputs change their state. From PWM output pins, the IGBTs are triggered.

The Figure 7 shows the algorithm of the DSP code for PWM generation. At each sampling interval, the interrupt loop is repeated.

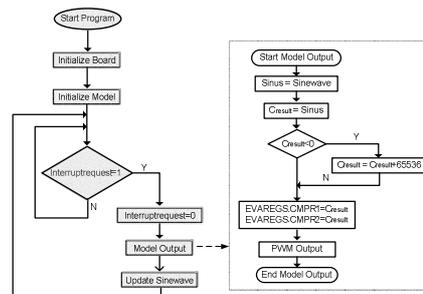


Figure 7. Algorithm of program

When the program is started from CCS, program sets the initial values of DSP board which must be done at the beginning of the program for once. After initializing the DSP board, initial values of the model are set (SineWave). When initialization finishes, program starts to generate PWM output signals as follows: at each sampling interval time program calculates new value of sine wave. The calculated value of sine wave is in float data type. Then the generated float type value is converted to Unsigned Integer 16 (uint16) data type. Result of this conversion is compared with the carrier signal and process ends. The corresponding PWM outputs are energized. In another sample time this process is repeated again until the program is stopped by the user.

### IV. EXPERIMENTAL SETUP

The basic circuit diagram of the DSP controlled single-phase inverter is shown in Figure 8.

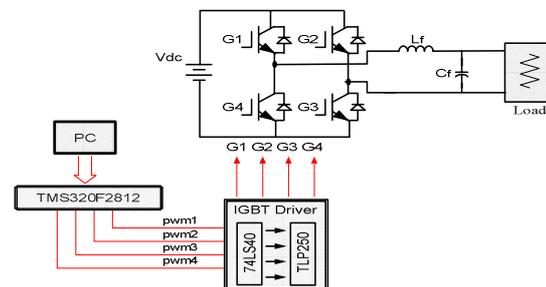


Figure 8. DSP controlled single-phase PWM inverter

Experimental setup procedure can be divided into two sections: the control and power circuit. Electrical isolation between control circuit and power circuit is provided by the optically coupled devices.

### CONTROL CIRCUIT DESIGN

The control circuit section is composed of three parts namely PC, DSP board and IGBT driver. TMS320F2812 eZdsp is programmed to produce gate pulses by comparing a triangular carrier wave in 2-KHz and a sinusoidal reference wave in 50-Hz. The reference wave amplitude adjusts the amplitude of the generated AC voltage and the reference wave frequency determines the frequency of the generated AC voltage.

1MBH50D-060 coded IGBTs are used in PWM inverter circuit. IGBTs are voltage controlled devices and it requires a minimum gate threshold voltage of about 15-V for establishing the rated collector-to-emitter conduction. This requirement makes it difficult to directly interface an IGBT to DSP. For proper operation of IGBTs, correct power levels are required ( $V_{ge(th)}=15\text{ V}$  and  $I_c=50\text{ mA}$ ). Voltage and current levels of DSP output signals fail to operate the IGBTs. IGBT driver circuit amplifies DSP output signal to the required level for triggering the IGBTs and isolates the DSP from the power circuit. TLP250 ICs are commonly used driver ICs for IGBTs. However, DSP output signals does not have enough current level to activate the TLP250. 74LS40 NAND gate IC is used to amplify the current value of signals from DSP at a gain of 50/2.

In the buffer circuit (74LS40) if two inverter gates are connected back to back, the two inversion functions would "cancel" each other out so that there would be no inversion from input to final output. DSP output signals are now ready to activate TLP250. TLP250 consists of a light emitting diode and an integrated photo detector. The output waveform will have the same waveform as the input waveform except the magnitude and power.

### POWER CIRCUIT DESIGN

The power circuit section is composed of four parts namely full bridge inverter circuit, DC power supply, LC filter and load. PWM inverters include semiconductor devices with nonlinear characteristics and can generate dominant harmonics in the system. The waveform quality of the sensitive load is improved by putting an LC filter at the output of the PWM inverter. In order to design an LC filter, there are many methods available. Optimum performance can be obtained by using [6] in simulation and experimental studies. A rule of thumb in control theory is that the frequencies of such a configuration have to have at least a factor of 10 between them to decouple the effects. According to this rule, for 50-Hz fundamental frequency, resonance frequency has to be at least 500-Hz, pulse frequency of the inverter output has to be at least 5000-Hz. Resonance frequency is determined by the product of L and C.

$$w_r = \frac{1}{\sqrt{L_f C_f}} \quad (3)$$

The choice of the individual values of  $L_f$  and  $C_f$  is a remaining degree of freedom. The filter inductor is selected as 0.9 mH. By substituting the inductance value into From (3) the capacitance  $C_f$  is calculated as 110  $\mu\text{F}$ .

### V. SIMULATION MODEL OF PWM INVERTER

The single-phase full wave inverter bridge is built using 4 ideal switches (S1, S2, S3, S4) and 4 anti-parallel diodes (D1, D2, D3, D4) in Simulink. In the model, sinusoidal wave at 50-Hz and carrier wave are compared to generate PWM signals. The relay block allows the output to switch 0 or 1 values. The output of Relay2 has inverse value of Relay1 output. PWM inverter uses self-commutating IGBT solid-state power electronic switches. The switching frequency of the inverters is in a frequency range from 2-KHz to 6-KHz. The single-phase inverter is connected to the common 30-Vdc voltage source. LC filter blocks high frequency harmonics caused by DC to AC conversion to reduce distortion in the output. The inductance and capacitance of the filter is 0.9 mH and 110  $\mu\text{F}$  respectively. The load is rated at 36.5-k $\Omega$  and receives power from LC filter output. 0.8-ms sample time (1.25-KHz sampling frequency) is used for measurements and sine wave generation. The simulink model is shown in Figure 9 and the simulation results are compared with the experimental results.

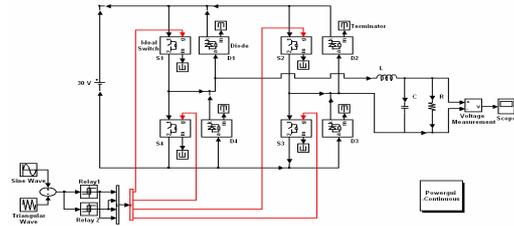


Figure 9. Simulation model of PWM inverter

### VI. RESULTS AND DISCUSSION

The experimental setup is composed of PC, DSP board, IGBT driver circuit, full bridge inverter circuit, DC power supply, LC filter and oscilloscope as shown in Figure 10. The proposed system is designed to provide a 50-Hz sinusoidal waveform on the load with varying carrier signal (2, 4 and 6-KHz). The sampling frequency of the DSP controller is set at 1.25-KHz. The design parameters of the test device are shown in Table 1.

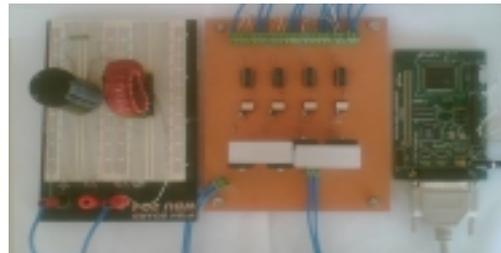


Figure 10. Experimental setup

Table 1.Design parameters

<b>System Frequency</b>	50-Hz
<b>Sampling Frequency</b>	1.25-KHz
<b>IGBTs 1MBH50D-060</b>	Semiconductor Voltage: 30- $V_{dc}$ Switching frequency: 2,4,6-KHz Threshold voltage: 15-V Threshold current: 50-mA
<b>Inverter filter</b>	Capacitance: 110- $\mu$ F, 250-V Inductance: 0.9-mH Resonance Frequency: 500-Hz
<b>74LS40</b>	High level input voltage: 3.3-V High level input current: 2-mA
<b>TLP250</b>	High level input voltage: 3.3-V High level input current: 50-mA

In Figure 11, the 50-Hz fundamental frequency is compared with 2-KHz carrier signal. The next step is increasing the frequency of carrier signal to 4-KHz and 6-KHz by observing the load voltage waveform. The resulting waveforms are depicted in Figure 12 and 13 respectively.

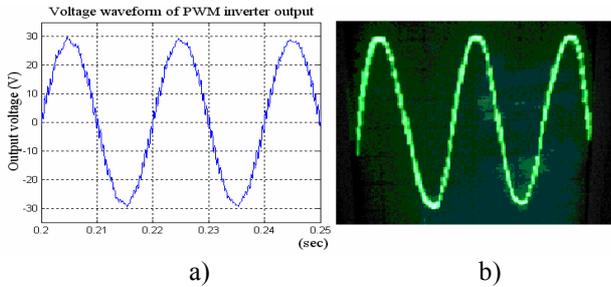


Figure 11. Simulation (a) and experimental (b) results at 2 kHz of switching frequency

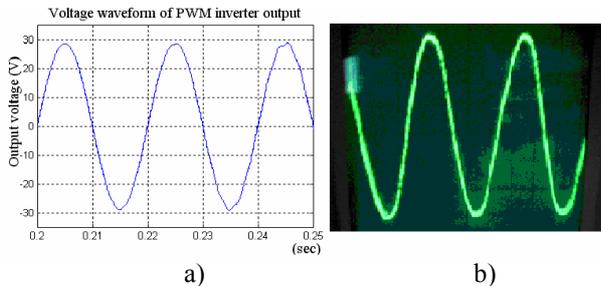


Figure 12. Simulation (a) and experimental (b) results at 4 kHz of switching frequency

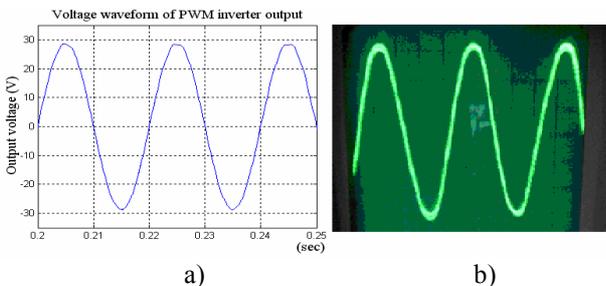


Figure 13. Simulation (a) and experimental (b) results at 6 kHz of switching frequency

The output voltage waveforms show that the experimental results are very similar to simulation results. As expected, the higher the switching frequency, the smoother the output voltage waveform.

## VII. CONCLUSION

This paper presents the analysis and design of a digitally controlled single-phase PWM inverter to develop more theoretical and practical knowledge on DSP based control applications. The basics of software optimization and hardware installation for proposed system have been presented in detail. The detailed architecture and signal processing components of the eZdsp F2812 from Texas Instruments have been clearly described. The effectiveness of the simulation results are verified experimentally at 2, 4 and 6-KHz switching frequency. The very close agreement of experimental and simulation results illustrates the efficiency, accuracy and dynamic response of DSP based PWM inverter design.

## VIII. ACKNOWLEDGEMENTS

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