An Ultra Low Power Frequency Divider for 2.4GHz Zigbee Frequency Synthesizer

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Abstract

This paper introduces an ultra low power frequency divider utilized in Integer-N frequency synthesizers, which operates in 2.4GHz IEEE 802.15.4/ZigBee frequency band. The proposed frequency divider consists of a dual modulus prescaler and a divide-by-64. In order to reduce the power consumption, Swallow counter has been replaced by a simple digital circuit. Simulation results exhibit 410µw power consumption for 4 bit frequency divider in 2.4GHz frequency band that proves 40% reduction compared to previous works. All of the circuits have been designed in 0.18µm TSMC CMOS technology with a single 1.8V dc voltage supply.

1. Introduction

Increasing the use of short range wireless communications created new protocols that define all parts of communication network including physical layer. ZigBee is one of the wireless technologies developed as a free global standard to lead to the unique requirements of low-cost and low-power wireless networks. The Zigbee standard operates on unlicensed bands of 860MHz, 920MHz and 2400MHz.

Majority of networks based on ZigBee protocol are powered by battery. Power consumption reduction of network nodes is one of the salient challenges for designers. Frequency synthesizer used for ZigBee transceivers is usually Integer-N phase locked loop (PLL). In this kind of PLL, programmable frequency divider is one of the important blocks that consume a large portion of energy. In [1] a new structure for frequency divider has been introduced that operates up to 5GHz with power efficiency of 1.79GHz/mW. A common method to implement a low power and high frequency divider in high frequency Integer-N PLLs, is based on pulse swallow divider [2 - 5]. In the conventional pulse swallow divider, the swallow counter is a loadable counter, so it has a quite complicated structure and wastes a large amount of energy. In this paper a new method for designing a frequency divider has been proposed which replaces swallow counter by a simple digital circuit that reduces 40% power consumption of frequency divider, compared to previous works. Proposed frequency divider has been designed to be used in Integer-N PLL, based on 2.4GHz IEEE 802.15.4/ZigBee transceiver with reference frequency of 5MHz that covers all 16 available channels.

The organization of this article is as follows: In section II, the Integer-N pulse swallow frequency divider will be described briefly and section III describes the building blocks of the proposed frequency divider. Finally, the simulation results are presented.

2. Integer-N Pulse Swallow Frequency divider

Fig. 1 shows a simple schematic of programmable frequency divider based on pulse swallow divider. As it is clear, this structure has a dual modulus (M) prescaler, a program (P) counter and a loadable swallow (S) counter. The prescaler has the ability of dividing its high frequency input by M+1 or M, depending on the logic level of the modulus control input. The program counter divides the output of the prescaler by a fixed count P. Finally the swallow counter also divides the prescaler output by S and controls the modulus selection of the prescaler. The swallow counter is reset by the program counter, every time it counts P input cycles. To explain the operation of the frequency divider, let us assume the prescaler starts dividing by M + 1; this process continues until the swallow counter reaches its count S and the modulus control of the prescaler is changed to divide-by-M. At this point, $(M + 1) \times S$ input cycles have been counted, and $(P - S)$ counts are left in the program counter. The program counter continues counting until it reaches P counts, which is reached with $M \times (P - S)$ input cycles. From the previous explanation it can be noticed that one complete cycle is achieved with $(M + 1) \times S + M \times (P - S) = M \times P + S$ cycles at the input. The previous result implies that the product $M \times P$ sets the lower limit of the frequency band that needs to be synthesized and S selects the desired channel [6].

Fig. 2 illustrates the proposed frequency divider. As it is obvious, we have replaced P counter and S counter with an integrated P&S counter. Modulus logic bit of prescaler is controlled by the output of Integrated P&S counter. As the

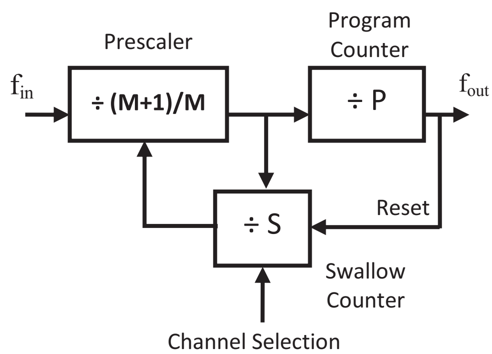

Fig. 1. Pulse Swallow frequency divider

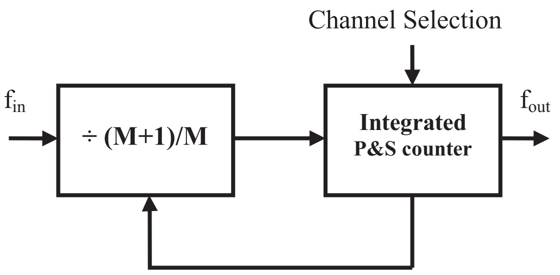

Fig. 2. Proposed frequency divider

ZigBee works in frequency band from 2405MHz to 2480MHz with channel space of 5MHz, we need a frequency divider from 481 to 496 to cover all 16 available channels. These numbers are obtained by a divide-by-7/8 dual modulus prescaler (M=7), P = 64 and $33 \leq S \leq 48$.

3. Building Blocks

3.1. Dual Modulus Prescaler

As mentioned in previous section, we have used a divide-by-7/8 dual modulus prescaler. Fig. 3.a illustrates the block diagram of dual modulus prescaler used in this structure. This prescaler consists of a divide-by-3/4 dual modulus prescaler and a divide-by-2. When the modulus bit is zero, the prescaler divides input frequency by 8. When the modulus bit changes to 1, output of Q_1 is reset by M_1-M_3, as Q_2Q_3=11. So the number of $Q_1Q_2Q_3$=111 is eliminated and the input frequency is divided by 7. Fig. 3.b shows a conventional true-single-phase-clocking (TSPC) D-Flip Flop (DFF) that has been used in the dual modulus prescaler. Table I listed the size of transistors that has been used in dual modulus prescaler.

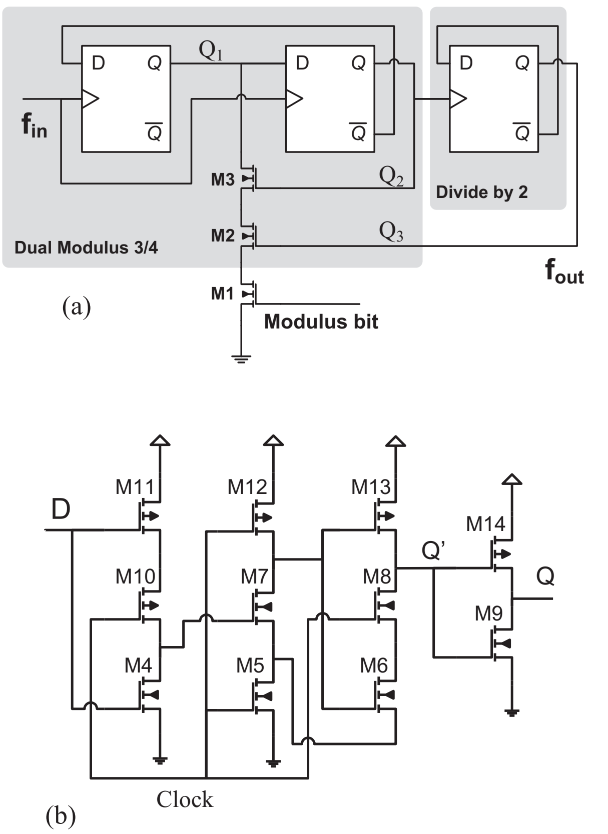

Fig. 3. a) 7/8 Dual modulus prescaler, **b)** Conventional TSPC DFF

Table I. Size of transistors used in prescaler

	Width (µm)	Length (µm)	Type
M_1-M_3	2	0.18	N
M_4-M_9	0.5	0.18	N
M_{10}-M_{13}	1	0.18	P
M_{14}	1.5	0.18	P

3.2. Integrated P&S counter

Fig. 4 shows the block diagram of Integrated P&S counter. As it is apparent, this counter consists of a divide-by-64 (P counter) that is made up of 6 divide-by-2. Digital circuit consists of XNOR gates (X_0 - X_4), AND gates (A_0, A_1) and a RESET-SET Flip Flop (RSFF). This digital section has replaced S counter in conventional ones and has the duty to control modulus bit of dual modulus prescaler. A_1 gate is driven by XNOR gates (X_0 - X_4). Table II shows the output of XNOR block for 4 available inputs. As it's clear, XNOR gate is an equality block. When inputs of XNOR are equal (both of them are 0 or 1), output of XNOR gate is logic one. So when the value of P counter ($P_5P_4P_3P_2P_1P_0$) is equal to predefined C number ($1C_4C_3C_2C_1C_0$), output of A_1 gate becomes logic 1 (C_4-C_0 bits are defined by transceiver system that changes the frequency channel of PLL). In this moment, as P_5 is 1 as well, RSFF is set by A_2 gate and dual modulus prescaler divide input frequency by 7. When P_5 changes to 0, RSFF is reset and dual modulus prescaler return to divide-by-8 state. For more details, assume the P counter is in ZERO condition {$P_5P_4P_3P_2P_1P_0$=000000}. As P_5 is equal to 0, RSFF is reset and

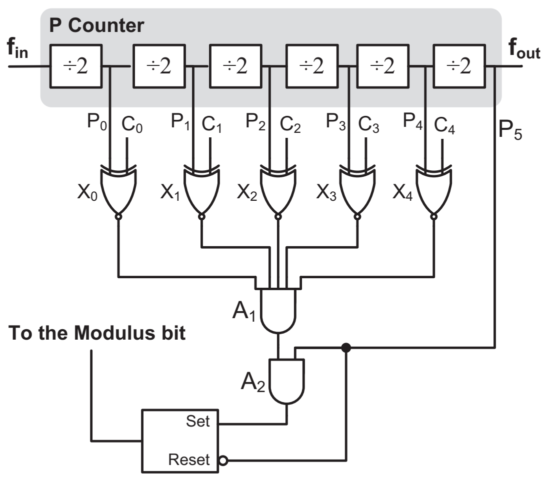

Fig. 4. Proposed Integrated P&S counter

Table II. True table of XNOR gate

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	1

dual modulus prescaler divides input frequency by 8. Suppose we want the PLL to work in 6th frequency channel and we load the number of 6 on C_4-C_0 $\{C_4C_3C_2C_1C_0=00110\}$. Input signal is applied and P counter increases until the value of P counter reaches the predefined C $\{P_5P_4P_3P_2P_1P_0=1C_4C_3C_2C_1C_0\}$. (For this example: $P_5P_4P_3P_2P_1P_0=100110$). In this value of P counter, output of XNOR blocks and P_5 are logic 1 that causes RSFF to be set by A_1 and A_2 gates. After this time, the prescaler divide input frequency by 7 till the P counter reaches to its maximum value (111111) and next value is 000000. RSFF is reset by P_5, prescaler returns to divide-by-8 situation and the cycle repeats again. In this cycle the events occurred similar to conventional pulse Swallow divider. For the quantity of predefined C ($1C_4C_3C_2C_1C_0=C$), prescaler divide input frequency by 8 and for rest of number (64 − C) it divides input frequency by 7. For a cycle we will have:

$$N = 8*C + 7*(64 - C) = 7*64 + C \quad (1)$$

$$f_{vco} = f_{ref} * N = 5MHz * (448 + C) \quad (2)$$

$$2405MHz \leq f_{vco} \leq 2480MHz \qquad 33 \leq C \leq 48 \quad (3)$$

For the example that was stated above, C= 32 +6, so f_{vco}=2430MHz, that is center frequency of 6th frequency channel of ZigBee standard. To increase operating speed, XNOR block has been implemented by pass-gate logic and divide-by-2 block has been made by TSPC DFF, similar to DFFs used in prescaler block.

4. Simulation Results

The proposed frequency divider has been designed to be used in PLL frequency synthesizer, to work in 2.4GHz ZigBee standard. All of the circuits have been designed and tested by Cadence spectre in 0.18µm TSMC CMOS technology. The power consumption of the previous programmable dividers and proposed programmable divider at the supply voltage of 1.8V is shown in Table III. Total power consumption of circuits is 410µw from a single 1.8V supply.

5. Conclusion

An ultra low power frequency divider for PLL frequency synthesizer working in ZigBee 2.4GHz standard has been proposed. The Swallow counter which consumes a large portion of energy in conventional frequency divider is replaced by a simple digital section in this structure. The divide-by-7/8 prescaler has been chosen for prescaler to decrease the frequency and power consumption of Integrated P&S counter. The simulation results show power consumption of 410µw that is 40% lower than previous works.

Table III. Comparison of proposed method with previous ones.

	[1]	[3]	[5]	[7]	**This work**
Frequency (GHz)	5.8	2.4	2.4	1.4	**2.4**
Power (mW)	3.24	2.6	0.7	1.8	**0.41**
Power Efficiency (GHz/mW)	1.79	0.92	3.4	0.78	**5.85**
Technology (µm)	0.18	0.18	0.18	0.18	**0.18**

6. References

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