SPICE MODELING OF INTERFACE TRAPS

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Abstract

We have simulated the experimental charge pumping technique by the implementation of a model in the electrical simulator SPICE 3F4. This model considers the temperature, the source and drain reverse bias, the frequency and the interface state density effects on the charge pumping current I_{CP}. The simulated results are in a good agreement with recent and different experimental results.

Key Words

Charge pumping, Modeling, Interface traps.

1. Introduction

Since the demonstration of the existence of surface states at the silicon/silicon dioxide interface, several techniques have been proposed for the determination of the density of these states and their energy distribution in the forbidden energy gap of silicon. Most of these techniques are based on measurements on MOS capacitors and have been studied in great detail. Consequently, they have become sufficiently reliable to be used routinely in most laboratories. For the determination of the surface states densities, directly on MOS transistors, only a few techniques are available. However, none of these techniques accepted for MOS transistors.

The charge pumping technique has been successfully applied, in the past years, to characterize the interface traps in the MOS transistors [1-5]. Many authors have developed and presented different ways of applying this technique for the determination of the interface traps average density, their energy distribution in the forbidden energy gap of silicon and the geometric mean value of the capture cross section for electrons and holes.

Charge pumping is a well-established technique for the characterization of interface traps in MOS transistors. It is studied and applied a lot, and is highly understood from the physical point of view. The charge pumping effect in MOS transistor was reported for the first time by Brugler and Jespers in 1969 [4], when applying rectangular pulses to the gate of a MOSFET, while source and drain are kept at a small reverse voltage. At the substrate contact, a recombination current proportional to the SiO_2 interface trap density is measured. It is based on the exploitation of a repetitive process whereby majority carriers coming from the substrate recombine with minority carriers previously trapped in interface states. Considering the emission processes, which control the exchange of charges at the interface, the information concerning the capture cross-section and the energy distribution of the interface states can be obtained. A lot of work has been published over the last two decades in order to improve the understanding of the technique.

In this work, we have implemented the three models of the charge pumping technique in SPICE 3F4. We have used the MOSFET level 1 of SPICE, to which we added a generator of current between drain and substrate for the measurement of the charge pumping current. This current, measured versus the different levels of the gate bias, can provide many interesting results concerning the parameters of the considered MOSFET.

2. Charge pumping principle

Brugler and Jespers [4] have already proposed a simple model for the origin of the charge pumping current. When an n-MOS transistor is pulsed into inversion, electrons will flow from the source and drain regions into the channel, where, a fraction of these electrons will be captured by the interface traps. When the gate pulse is driving the surface back into accumulation, the mobile electrons drift back to the source and drain. But the charges that are trapped at the interface traps will recombine with the majority carriers coming from the substrate. This gives rise to a net flow of negative charge into the substrate, given by [5]:

$$Q_{CP} = qA_{eff} \int_{E_{F,acc}}^{E_{F,inv}} D_{it}(E)dE \tag{1}$$

where q is the electron charge, A_{eff} is the channel area of the transistor (cm^{-2}), $D_{it}(E)$ is the interface trap density at an energy level E($cm^{-2}eV^{-1}$), and $E_{F,inv}$ and $E_{F,acc}$ are the Fermi levels respectively in inversion and accumulation. When applying repetitive pulses with a frequency f, this charge Q_{cp} will gives rise to a net DC-current in the substrate, which can be written as [2]:

$$I_{cp} = fQ_{cp} = fqA_{eff} < D_{it} > \Delta E \tag{2}$$

where $<D_{it}>$ is the mean interface trap density over the energy range $\Delta E = E_{F,inv} - E_{F,acc}$.

In this simple first–order theory, Brugler and Jespers [4] assume tacitly that the carriers that are trapped in the interface traps during the first half of the pulse period, remain trapped until they recombine with the opposite type of carriers during the second half of the pulse period. As a result, all interface traps between the Fermi levels inversion and accumulation are participating to the charge pumping process. However, this is true only for zero transition times between inversion and accumulation. In practice, this switching between inversion and accumulation requires a finite time. During this time, part of the carriers trapped in the interface states can be released from the traps by thermal emission, and become free carriers, which are also swept out of the channel. Both the capture of the carriers from the silicon bands into the traps and the thermal emission of the carriers from the traps towards the silicon bands are described by the Shockley-Read-Hall (SRH) generation recombination theory. Therefore, an improved model was developed.

2.1. Thermal emission/recombination model

The charge pumping process, and especially what happens during the transitions from accumulation to inversion and vice versa, is essentially governed by the dynamic charge of the MOS system submitted to the varying gate voltage, and the response of the interface traps to this varying gate voltage. This dynamic charge of the MOS system under the influence of a gate linearly ramped voltage was extensively studied by G. Groeseneken et al. [3] and Simmons et al. They have solved the problem by dividing it in two separate parts. The first one is called the steady-state situation, when the charge in the interface traps remains in dynamic equilibrium with the energy bands of the silicon during the voltage ramp. The second one is called the non-steady-state period, when the charges in the interface traps are not able to follow the voltage ramp, and the trap are not longer in equilibrium with the bands. Based on this theory, it was demonstrated [5] that only the traps, that are not able to emit electrons to the conduction band during the falling gate pulse edge and holes to the valence band during the rising gate pulse edge, contribute to the charge pumping current. As a result, four different currents can be distinguished, which can be associated with the various parts of the gate pulse period and with the various regions in the band gap, as is schematically shown in Fig. 1, where I_1 is the electron trapping current, occurring primarily in the inversion part of the pulse, I_2 is the electron emission current, dominant during the falling pulse edge, I_3 is the hole trapping current, dominant during the accumulation part of the pulse and I_4 is the hole emission current, dominant during the rising edge of the pulse. The electronic current, which flows through source and drain, is thus given by [4,5]:

$$I_E = I_1 + I_2 = +q < D_{it} > (E_{em,h} - E_{em,e}) \quad (3)$$

Likewise, the hole current, which flows through the substrate, I_{sub}, is thus given by:

$$I_{sub} = I_3 + I_4 = +q < D_{it} > (E_{em,h} - E_{em,e}) \quad (4)$$

The expressions (3) and (4) are identical. Then:

$$I_{CP} = I_3 + I_4 = +q < D_{it} > (E_{em,h} - E_{em,e}) \quad (5)$$

where $E_{em,h}$ and $E_{em,e}$ correspond to the end of the non-steady hole emission and to the end of the non-steady-state electron emission. We need to express them in more detail to be able to derive a usable expression for current I_{CP}.

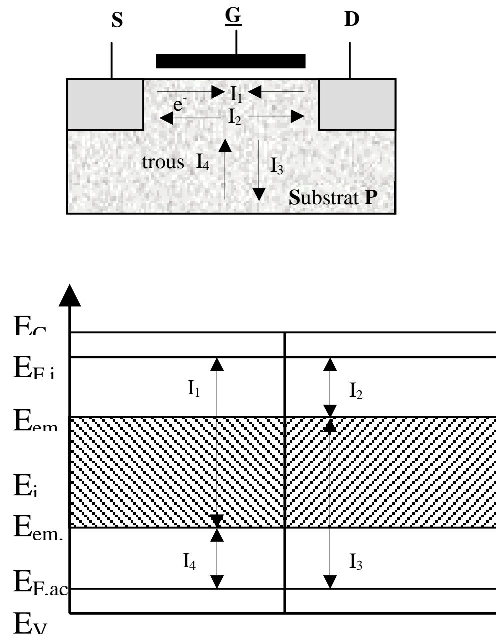

Fig. 1. Different energy regions associated with the four components of the charge pumping current.

2.2. Calculation of the emission level

A simple reasoning allows us to assess the demarcation levels. To determine the level $E_{em,h}$, we consider that the interface states situated between $E_{F,acc}$ and $E_{em,h}$ have a hole emission time constant $\tau_{em,h}$ which is small compared with $t_{em,h}$, (the time period during which these traps can emit holes). Closer to the valence band, the easier it is for the

traps to re-emit holes into it. According to the Shockley-Read-Hall (SRH) theory [3], $\tau_{em,h}$ can be expressed as:

$$\tau_{em,h} = \frac{1}{\sigma_p v_{th} n_i e^{\frac{E_i - E_t}{KT}}} \quad (6)$$

with σ_p is the capture cross-section of holes, v_{th} is the thermal velocity of carriers, n_i is the intrinsic carriers concentration, E_i is the intrinsic Fermi level and E_t is the energy level of interface trap.

Therefore, for those interface traps located between $E_{em,h}$ and $E_{F,inv}$, the emission time constant is greater than $t_{em,h}$. Demarcation level $E_{em,h}$ is thus given by the condition $\tau_{em,h}=t_{em,h}$:

$$E_{em,h} - E_i = K.T.\ln\left(v_{th}.\sigma_p.n_i.t_{em,h}\right) \quad (7)$$

$$E_{em,e} - E_i = -K.T.\ln\left(v_{th}.\sigma_n.n_i.t_{em,e}\right) \quad (8)$$

with σ_n is the capture cross-section of electrons.

when V_g is between V_{FB} and V_T (Flat band and Threshold voltages of MOS transistor respectively). The emission durations $t_{em,h}$ and $t_{em,e}$ are given by:

$$t_{em,e} = \frac{|V_T - V_{FB}|}{\Delta V_g} t_f \quad \text{and} \quad t_{em,h} = \frac{|V_T - V_{FB}|}{\Delta V_g} t_r$$

where $\Delta V_g=V_{gh}-V_{gl}$ is the amplitude of the gate voltage pulse, V_{gh} is the upper level of the gate voltage pulse, V_{gl} is the lower level of the gate voltage pulse, t_r is the rise time of the gate pulse and t_f is the fall time of the gate pulse.

$$E_{em,h}(t_r) = E_i + KT\ln\left[v_{th}\sigma_p n_i\left(\frac{|V_T - V_{FB}|}{\Delta V_g}\right)t_r\right] \quad (9)$$

$$E_{em,e}(t_f) = E_i - KT\ln\left[v_{th}\sigma_n n_i\left(\frac{|V_T - V_{FB}|}{\Delta V_g}\right)t_f\right] \quad (10)$$

K is the Boltzmann constant and T is the temperature.

Basing on the SRH theory, the energy region can be expressed as:

$$\Delta E = 2.qKT\ln\left[V_{th} n_i \sqrt{\sigma_n \sigma_p}\frac{|V_T - V_{FB}|}{\Delta V_g}\sqrt{t_r.t_f}\right] \quad (11)$$

Thus, for trapezoidal waveforms, I_{cp} varies linearly with frequency. Since the rise and full times remains constant when f varies:

$$I_{cp} = 2qKTf\langle D_{it}\rangle A_{eff}\ln\left(v_{th} n_i \sqrt{\sigma_n\sigma_p}\frac{|V_T - V_{FB}|}{\Delta V_g}\sqrt{t_r t_f}\right) \quad (12)$$

2.3. Effect of the source and drain reverse bias, oxide charge and interface states on I_{cp}

When the reverse bias V_R is increased, we observe a variation in the charge pumping current. For an n- chanel transistor, I_{cp} decreases when V_R decreases. This is because both threshold voltage and channel length varies with V_R.

$$V_T = V_{FB} + 2|\psi_B| + |V_R| + \frac{T_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{Si}N_a\left(|V_R| + 2|\psi_B|\right)} + \Delta V_T \quad (13)$$

$$\Delta V_{T1} = -\frac{qNaL_{S,D}r_j}{C_{ox}}\left[\sqrt{1 + \frac{2L_{S,D}}{r_j}} - 1\right] \quad (14)$$

where $L_{S,D}$ is the width of the space charge regions of the source/substrate and drain/substrate junction, N_a is the concentration of the acceptors (cm^{-3}), r_j is the depth of the source/substrate junction, ψ_B is the potential of the substrate bulk, C_{ox} is the oxide capacitance per unit area and ε_{Si} is the permittivity of silicon.

From (13) we note that an increase of V_R produces an increase of $|V_{FB}-V_T|$ and therefore, as predicted by the expression of $t_{em,e}$ and $t_{em,e}$, a decrease of the charge pumping current.

By increasing the reverse voltage applied to the source/substrate and drain/substrate junctions, we increase the width $L_{S,D}$ and thus decrease the effective length L_{eff} of the channel, given by $L_{eff}=L-2L_{S,D}$. It follows that the effective gate area A_{eff} and thus I_{cp} decrease. The width $L_{S,D}$ is given by:

$$L_{S,D}(V_R) = \frac{2\varepsilon_{Si}}{qN_a}\left[|V_R| + |\psi_B|\right]^{1/2} \quad (15)$$

Thus by using a simple one-dimensional model, the effective gate area A_{eff} can be expressed as:

$$A_{eff}=W-(L-2L_{S,D})$$

The variations of V_T and V_{FB} due to the interface states are:

$$\Delta V_{T2} = -Nq\frac{\langle D_{it}\rangle}{C_{ox}}KT\ln\left(\frac{N_a}{V_{th}\sigma_p n_i^2 t_{em,h}}\right) \quad (16)$$

$$\Delta V_{FB1} = -Nq\frac{\langle D_{it}\rangle}{C_{ox}}KT\ln\left(\frac{N_a}{V_{th}\sigma_n n_i^2 t_{em,e}}\right) \quad (17)$$

With N=+1 for a positive charge and –1 for a negative charge, q is the electron charge [C]. The variations of V_T and V_{FB} due to the oxide charge are:

$$\Delta V_{T3} = \Delta V_{FB2} - Nq\frac{N_{ox}}{C_{ox}}(1 - \frac{\overline{X}}{t_{ox}}) \quad (18)$$

where N_{ox} is the oxide charge number (cm^{-3}), t_{ox} is the oxide width (μm) and $\overline{X} = t_{ox}/2$. The global variations of V_T and V_{FB} are [6,19]:

$$dV_T = -Nq\frac{t_{ox}}{\varepsilon_{ox}}\left[\frac{N_{ox}}{2} + \langle D_{it}\rangle KT\ln(\frac{N_a}{V_{TH}\sigma_P n_i^2 t_{em,h}})\right] \quad (19)$$

$$dV_{FB} = -Nq\frac{t_{ox}}{\varepsilon_{ox}}\left[\frac{N_{ox}}{2} + \langle D_{it}\rangle KT\ln(\frac{N_a}{V_{TH}\sigma_n n_i^2 t_{em,e}})\right] \quad (20)$$

The total variation of ΔV_T which will be simulated is the summation of (14), (20) and (19).

2.4. Effect of the temperature on I_{cp}

Equations (9) and (10) are directly dependent on temperature because, physically, carrier emission from the interface traps depends strongly on temperature. CP measurements are also very sensitive to temperature. When T increases, the emission process from the traps increases while the recombination process decreases. Van den Bosch et al. have expressed the dependence of charge pumping current I_{cp} on T by:

$$I_{CP} = -aT - bT\ln(T) + c \quad (21)$$

where:

$$a = 2.qKfA_{eff}\langle D_{it}\rangle \ln\left[\sqrt{\sigma_n\sigma_p}\right]\sqrt{\frac{3.K}{m^*}}.K_i\frac{|V_T - V_{FB}|}{\Delta V_g}\sqrt{tr.t_f}$$

$$b = 4qKfA_{eff}\langle D_{it}\rangle$$

$$c = qfA_{eff}\langle D_{it}\rangle E_G$$

m^* is the average effective mass of the carriers, E_G the silicon bandgap and K_i is a constant. We note here that the electrical and geometrical parameters of the transistors are not dependent on temperature.

4. Results and discussion

Many models of the MOSFET, with different complexities and sensitivities, are included in SPICE 3F4. To develop our model, we have used the MOSFET LEVEL 1 of SPICE 3F4, and we have added to it a current source to simulate the charge pumping current. We have considered the three following effects on the threshold tension V_T:

1. the channel length modulation,
2. the reduction of V_T (due to interface states and oxide charges),
3. the effect of V_R on V_T.

The simulation results have been obtained with conventional n-channel MOSFET's. These results, described, are obtained for trapezoidal pulses with an amplitude ΔV_g. In the first part we assume that the electrical and geometrical parameters of the MOSFET are independant to the temperature.

Fig. 2 shows the charge pumping current I_{cp} versus V_{gh} at V_{gl}=-4V. The oxide thickness T_{ox}=25nm, the channel length and width are, respectively, L=100μm and W=100μm (canal long), the intrinsic concentration n_i(Si)=1.45.10^{10}cm^{-3}, the thermal carrier velocity v_{th}=10^{7}cm.s^{-1}, the capture cross-sections for electrons and holes are σ_n=σ_p=10^{15}cm^2, the interface trap density $\langle D_{it}\rangle$ =10^{10}cm^{-2}eV^{-1}, the flat band voltage V_{FB}=0.75V and N_a=2.10^{16}cm^{-3}. These curves, obtained for a frequency f=100KHz and a reverse voltage V_R=2V, 4V and 8V show the effect of V_R on the charge pumping current I_{cp}. We see that I_{cpmax} decreases when V_R increases because the gate area is reduced and the variation of I_{cp} begins only when V_{gh}=V_T. In addition, the variation of the registered threshold voltage is due to the variation of V_R. We note that the charge pumping edge also broaden when V_R varies.

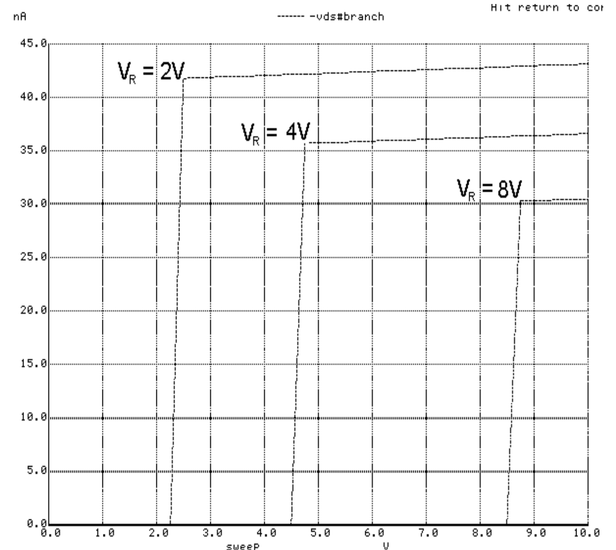

Fig. 2. The charge-pumping current versus the top gate pulse level V_{gh} at a base gate pulse level V_{gl}=-2V, with the reverse voltage V_R as parameter.

Fig. 3 shows the charge pumping current I_{cp} versus V_{gl} at V_{gh}=2V, T_{ox}=12nm, L=0.8μm, W=4μm and V_R=0.1V, with

the same values of n_i(Si), v_{th}, $\sigma_{n,p}$ V_{FB} and f, used for Fig. 2. This curve shows that an increase of the interface trap density does not only result in an increase of maximum CP current, but the CP edges also broaden. This is due to the charging and discharging of the fast interface traps.

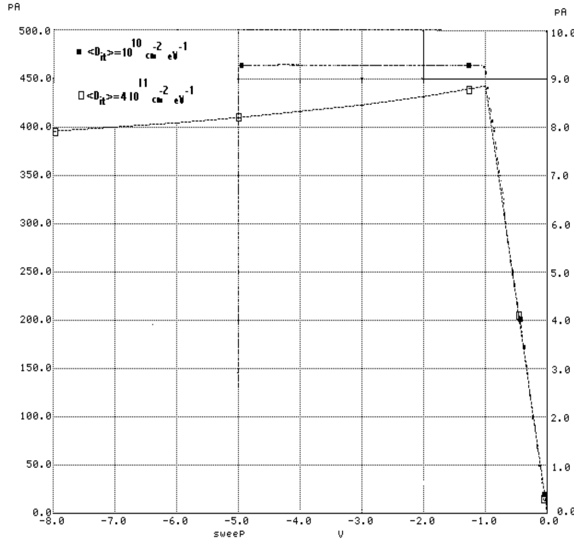

Fig. 3Charge pumping current versus the low level V_{gl} of the gate pulse.

In Fig. 4, the maximum of the base-level CP curves is shown as function of the temperature. We can note that I_{cp} is well described by (21), implying an interface trap distribution, which is not strongly varying over the band. In the lower temperature range, the CP process behaves as expected from theory at least down to 77°K.

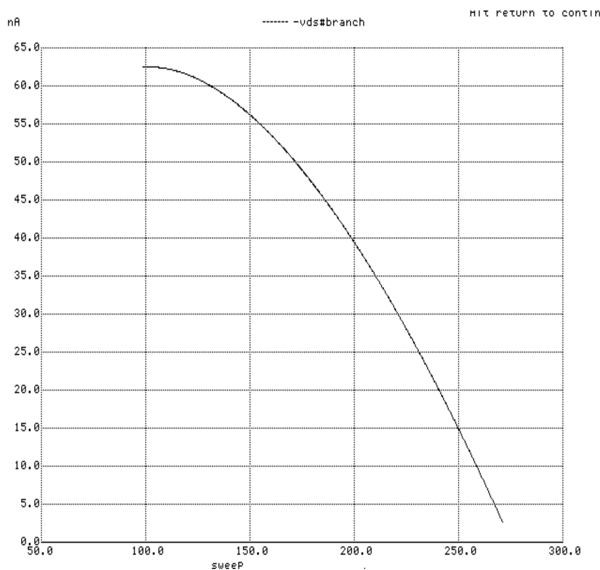

Fig. 4. Maximum of I_{cp} versus base level as function of the temperature(°K).

5. Conclusion

In this work, we have developed a 2-level and spectroscopic charge-pumping model that we implemented in SPICE 3F4. We have plotted I_{cp}=f(V_{gl}), I_{cp}=f(V_{gh}) for different transistor dimensions and I_{cp}=f(V_{gl}) for different temperatures. We have also plotted the spectroscopic signals versus the temperature for various energy windows. Our simulated results are in good agreement with other recent experimental results, which proves the efficiency of the developed model.

7. References

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