

A NEW NEGATIVE RESISTANCE CIRCUIT AND AN APPLICATION FOR LOSS COMPENSATION IN A DISTRIBUTED AMPLIFIER

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ABSTRACT

This paper presents a new negative resistance (NR) network which is designed to compensate losses in a distributed amplifier (CDA). The byproduct of the new NR network in the CDA is significant improvement of bandwidth (~20%). The simplicity of the NR network makes it amenable to MMIC technology and for other applications too.

I. INTRODUCTION

Traditionally negative resistance (NR) circuits have been used in various applications such as oscillators and filters [1,2]. Other interesting application of NR circuits has been presented for loss compensation in a conventional distributed amplifier (CDA) [3]. A conventional distributed amplifier employs two artificial transmission lines that show a low-pass filter characteristic. When designing a CDA, the main consideration is usually increasing the bandwidth of the amplifier. However, one of the major problem usually encountered is the frequency behavior of the input conductance of the transistors, which increases rapidly with frequency and causes increased attenuation with frequency [4]. The effect of this is degradation in the CDA performance. Therefore, the upper frequency limit of a CDA is always lower than the cut-off frequency of the artificial line.

A negative resistance circuit has been presented previously in the literature in order to compensate a CDA for the gate line losses [3]. This circuit uses an FET in the common-gate configuration, the drain port of which offers NR behavior. For a good compensation of the inherent losses, NR circuit is placed in the gate line of a CDA. Obtaining NR behavior from the gate port of a FET has an advantage from the compactness point of view.

In this work, we propose a new NR network using a FET in the common-source configuration, the gate port of which offers NR behavior. The offshoot of the new NR circuit is in considerable bandwidth extension and the cut-off frequency of a CDA.

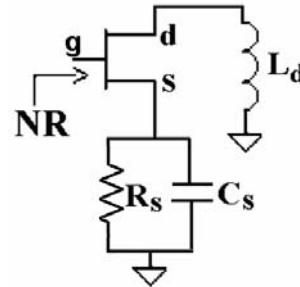


Fig. 1 The proposed NR circuit.

II. THE NEW NR CIRCUIT

It is known from the literature that an overcompensated common-source circuit with a parallel R_S - C_S combination at the source port offers NR behaviour in a predetermined frequency band [5]. Here, we propose an additional element (i.e. inductance, L_d) at the drain port, which has the property of improving the NR behaviour of the network at high frequencies. The new NR circuit is shown in Fig.1.

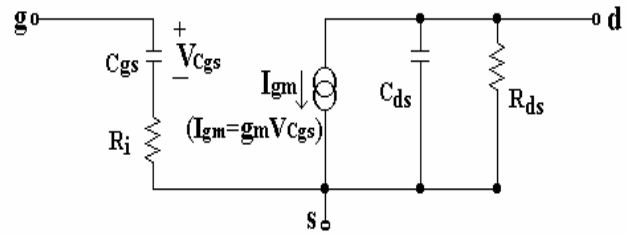


Fig.2 Simplified small-signal FET model

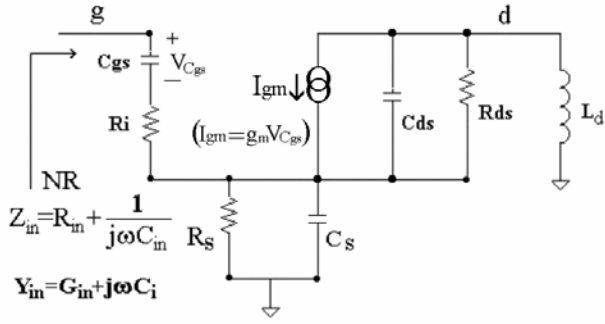


Figure 3 The small-signal equivalent of the new NR circuit.

The simplified small-signal FET model is shown in Fig. 2. By using this figure the small-signal equivalent of the new NR circuit is obtained as Figure.3. From Fig.3 the input impedance (Z_{in}) of the proposed NR network can be expressed with the following equation:

$$Z_{in} = \frac{1}{j\omega C_{gs}} + R_i + \frac{U_r + jU_i}{D_r + jD_i} \quad (1a)$$

$$U_r = R_s R_{ds} - \omega^2 L_d R_s (C_s R_s + C_{ds} R_{ds}) \quad (1b)$$

$$U_i = -\frac{R_s R_{ds} g_m}{\omega C_{gs}} + \omega L_d R_s - \omega^3 L_d C_s C_{ds} R_s^2 R_{ds} \quad (1c)$$

$$D_r = R_{ds} + R_s - \omega^2 L_d (C_s R_s + C_{ds} R_{ds}) \quad (1d)$$

$$D_i = \omega R_s R_{ds} (C_s + C_{ds}) + \omega L_d - \omega^3 L_d C_s C_{ds} R_s R_{ds} \quad (1e)$$

The real part of Z_{in} for the DC case is obtained as:

$$Re\{Z_{in}\}_{DC} \cong R_i + R_s \left\{ 1 - \frac{g_m}{C_{gs}} \left[R_s (C_s + C_{ds}) + \frac{L_d}{R_{ds}} \right] \right\} \quad (2)$$

It is obvious from Eqn. (2) that $Re\{Z_{in}\}$ can be made negative for appropriate values of R_s , g_m , C_s and L_d . On the other hand, investigating Eqn. (1) reveals that $Re\{Z_{in}\}$ has a maximum value at high frequencies, and that the maximum value is achieved within the frequency interval of

$$\sqrt{\frac{2 - R_s g_m \frac{C_s}{C_{gs}}}{2 L_d C_{ds}}} < \omega_{max} < \sqrt{\frac{1}{L_d C_{ds}}} \quad (3)$$

An expression for the calculation of L_d can be obtained from Eqn. (3);

$$L_d = \frac{1}{\omega_{max}^2 C_{ds}} \quad (4)$$

where ω_{max} can be chosen as the frequency at which the negative conductance is needed to be maximum. Detailed investigation of Eqn. (1) shows that the proper values of R_s and C_s can be obtained for good performance from CDA. The R_s should be chosen in the interval of

$$1/g_m < R_s < 3/g_m \quad (5)$$

and C_s should be chosen as

$$C_s \approx C_{gs} - C_{ds} \quad (6)$$

On the other hand, Eqns. (4), (5) and (6) can be used in the first step of a CDA design. The exact values of L_d , R_s and C_s are determined after the optimisation of the CDA.

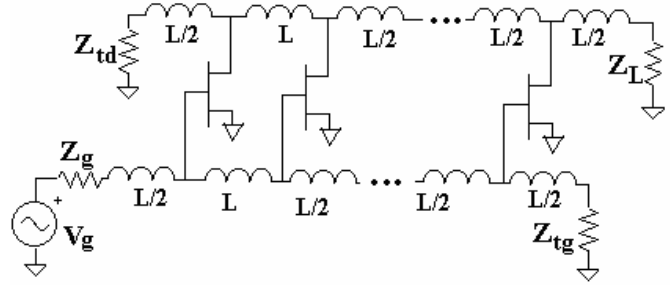


Fig.4 A conventional distributed amplifier.

III. USING NR IN A CDA

A conventional distributed amplifier is shown in Fig.4. In this figure it is assumed that input and output parasitic capacitances of the transistors are the same. One of the important problems, which degrade the performance of a CDA, is the frequency behaviour of the input conductance of the transistors.

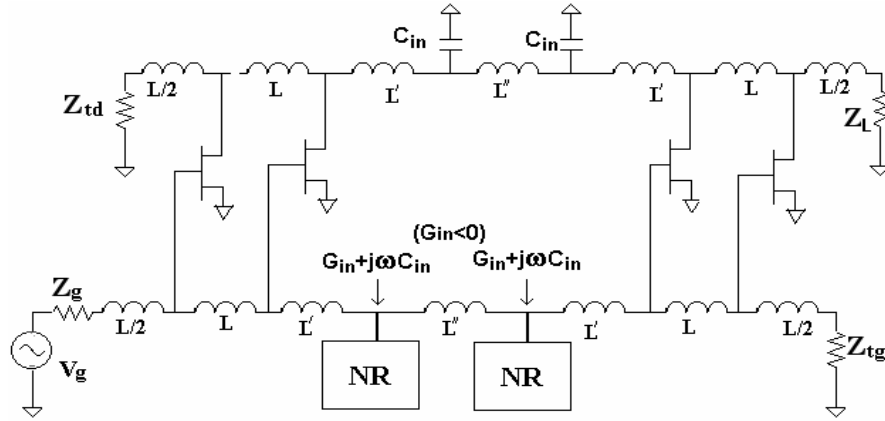


Fig. 5 The distributed amplifier using NR circuits.

The FETs input resistance, R_i , (see Fig. 2) causes a shunt conductance at the input of the active device, which increases rapidly with frequency and causes increased attenuation with frequency in the gate-line. This shunt conductance at high frequency region can be approximated as [3]:

$$G_I \cong \omega^2 C_{gs}^2 R_i \quad (7)$$

Therefore, the upper frequency limit of a CDA is always lower than the cut-off frequency of the artificial line [3].

The proposed distributed amplifier uses NR networks in order to compensate for the gate line losses of a CDA is shown in Fig.5. This circuit uses a FET in common-gate configuration, whose drain port offers NR behaviour. For a good compensation for the losses, NR networks are placed in the gate line of a CDA. The number and the location of the NR networks are important. In the design presented here two NR networks are used, which are placed between the second and the third transistors. In this case, the input capacitances of the NR networks serve also as the parallel capacitances of the T-sections. If the input capacitance of a NR network is very low compared to the input capacitance of the FETs used for the required gain, the NR network can be placed at the input of one of the FETs.

IV. SIMULATION RESULTS

In this section, a CDA and an NR-CDA are designed for comparison. The FET used in both amplifiers is a NE3210S01 packaged device from NEC. The number of transistors as the gain cells is four. In the amplifier design, the operating point voltages of the FETs are chosen at $V_{DS} = 2V$ and $V_{GS} = -0.4V$. The dielectric medium chosen for the realization of the circuits is Duroid™ with a thickness of 0.793 mm and relative dielectric constant of 2.17.

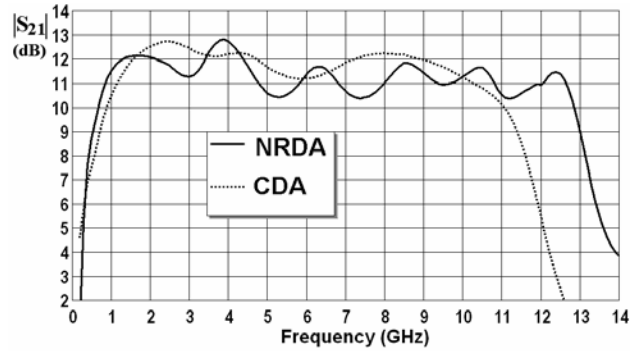


Fig. 6 Gain responses of the CDA and the NRDA.

The frequency responses of both amplifiers are shown in Fig. 6. The upper cut-off frequencies are 11 GHz and 12.9 GHz for the CDA and the NRDA, respectively. Note the gain increase in the upper frequency region of the NRDA in order to observe the effect of the NR circuits (on the other hand, the NR networks have been causes ripples within the band). The results indicate that the upper cut-off frequency for the NRDA has increased by 17%.

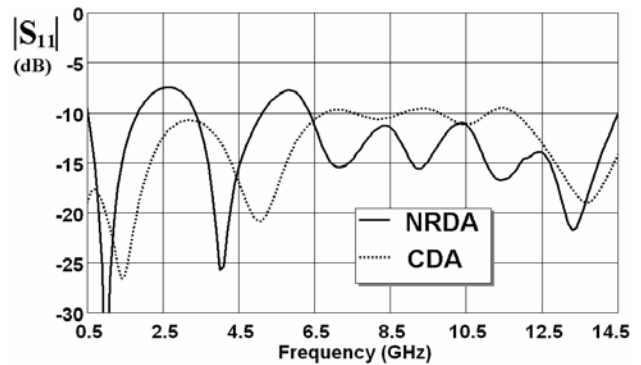


Fig.7 input matching performances of the amplifiers

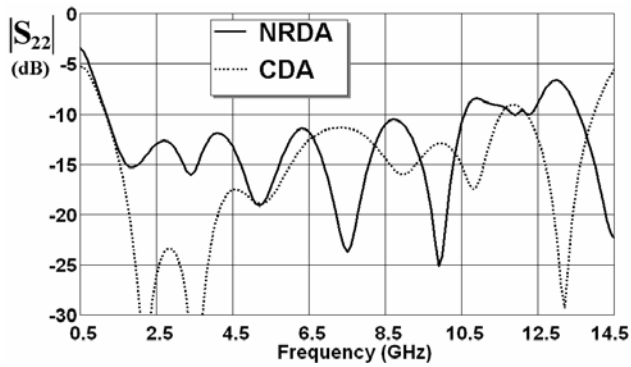


Fig.8 output matching performances of the amplifiers

Input and output match performances of the CDA and the NR-CDA are shown in Fig.7 and 8. These figures show that the matching performances of both amplifiers are satisfactory across the bandwidth shown.

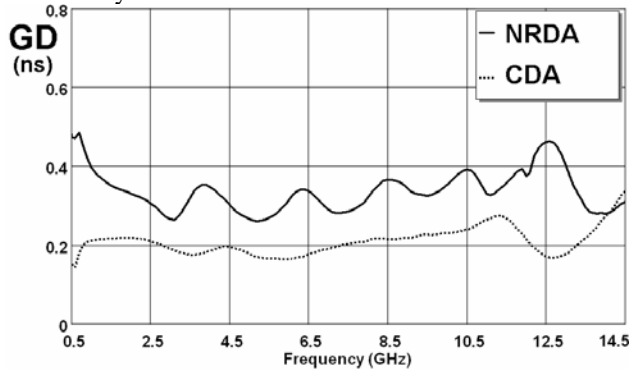


Fig. 9 GD performances of the CDA and the NRDA

Fig.9 shows group delay (GD) performances of the circuits. The GD performance of the CDA is a little better than that of the NRDA. However, it can be sad that the NRDA has given a good GD performance.

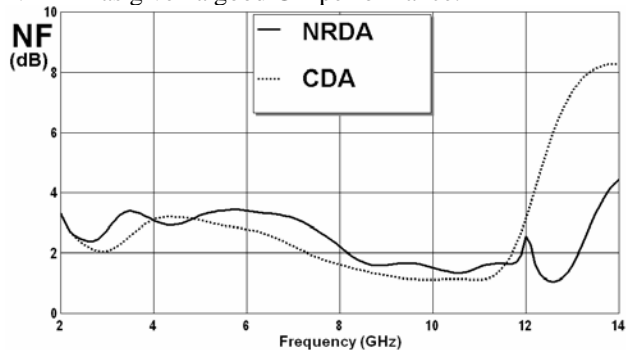


Fig. 10 NF performances of the CDA and the NRDA

Noise figure (NF) performances are given in Fig.10. As seen from the figure, the CDA and the NRDA have given similar NF performances till 11GHz (the performance of

the CDA is a little better than that of the NRDA). After ~11GHz the NF value of the CDA increases because of the decreasing gain. The same thing is valid for the NRDA after ~13GHz.

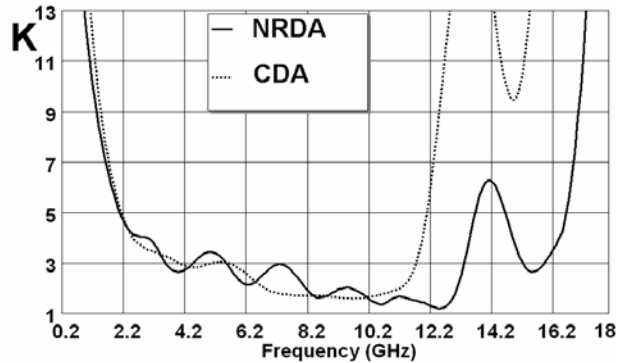


Fig.11 Stability factors (K) of the CDA and the NRDA

Stability factors of the CDA and the NRDA were also investigated and the results are shown in Fig.11. As seen from the figure, the stability factors are higher than 1 for both amplifiers.

V. CONCLUSION

In this paper a new negative resistance network topology is shown to provide loss compensation to a conventional distributed amplifier with an added feature of bandwidth extension (~20%) over a conventional distributed amplifier employing the same active devices. This negative resistance network is simple and can be implemented in MMIC distributed amplifiers with enhanced performance.

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