IGBT BASED INVERTER WITH Soft Switching AUXILIARY CIRCUIT FOR INDUCTION-COOKING APPLICATIONS

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Abstract- this paper presents a half-bridge inverter with active auxiliary circuit. The auxiliary circuit is implemented to provide ZVS transition for all switches. Characteristic curves of the inverter are presented in order to provide a detailed design which leads to reduce conduction losses. The simulation results are provided by PSCAD/EMTDC software.

I. INTRODUCTION

Induction heating (IH) systems for cooking applications received great attention in recent years owing to their merits of very high thermal conversion efficiency, rapid heating, local spot heating, direct heating, high power density, high reliability, low running cost and non-acoustic noise. Most of the IH systems are constructed of resonant inverters operating at high frequencies. However, they have caused some difficulties due to the high commutation losses in the switching and the appearance of EMI. These factors occur mainly in inverter topologies that use the bridge inverter configuration.

Recently, two main solutions such as passive techniques and active techniques were proposed in literature in order to solve these problems. The passive techniques which do not use any switch in their structure have got good performance in the majority of their applications. But they can not regenerate the energy losses of the switches. The active techniques are introduced by controlled switches in their circuits. The main active solutions are those that use pulse width modulation (PWM), with the need for no special control circuits. Several of these works are proposed in [1]-[5] but these suffer from one or more of the following drawbacks.

1) The auxiliary circuit consists of several components [1].
2) The voltage and current stresses on the auxiliary circuit components are high and accordingly the conduction losses, [3] and [4].
3) The auxiliary switch of most ZVS converters has a hard turn-off and this limits the gain in efficiency of the inverter [5].

This paper presents and analyses the operation of new topology inverter which contains auxiliary single switch snubber circuit. The proposed high-frequency PWM controlled inverter can prepare soft switching operation over a wide output power regulation range with a high efficiency. Design is based on the steady-state characteristic curves to provide a detailed analysis of the reduction in conduction losses of the proposed inverter. Simulation results from a 310 V input prototype switching at 20 kHz is given which verify the feasibility of the design process and advantages of the proposed topology. The proposed inverter can be used in single phase home-cooking application with a high thermal efficiency and high safety at power levels up to 3.2 kW.

II. CIRCUIT DESCRIPTION AND CONTROL PRINCIPLES

The proposed topology is illustrated in Fig. 1. It presents a half-bridge inverter configuration, where the $Q_1$ and $Q_2$ are the main switches. The auxiliary resonant circuit, surrounded by the dotted line, composes of the auxiliary resonant inductor $L_a$ and capacitor $C_a$ with the auxiliary active switch $Q_3$ connected in parallel to the upper side of the main active switch $Q_1$. The power circuit the active switches are IGBTs (insulated gate bipolar transistors), suitable for large IH cooking heater. The values of the load of this inverter $R_o$ and $L_o$ are determined by assuming its application for an IH cooking heater, and its frequency is fixed as 20 kHz.

This inverter can be operated under soft-switching operation by feeding gate pulse signals as shown in Fig. 2 and then its output power can be regulated continuously by adjusting the PWM technique as changing the total turn-on time of the switch sets $Q_j$ and $Q_i$ ($T_{sw}$) during its one cycle of inverter operation $T_s$. The maximum output power is obtained at $D_{opt} = 0.46$ which is depicted in Fig. 2 (a) and is defined as:

$$D_s = \frac{(T_{sw1} + T_{sw2} + T_{sw3})}{T_s} = \frac{T_{sw}}{T_s}$$

The minimum output power is obtained at $D_{min} = 0.14$ which is depicted in Fig 2 (b) and is defined as:

$$D_s = \frac{(T_{sw1} + T_{sw2})}{T_s} = \frac{2 T_{sw}}{T_s}$$
It can be seen that in Fig 2 (b) the second part of the turn-on duration of the switch set $Q_3$ is omitted to achieve lower output power.

![Proposed ZCS PWM high-frequency inverter](image)

**III. CHARACTERISTIC CURVES OF THE INVERTER**

Characteristic curves of the inverter are presented in this section to assist in the design process of the converter. These curves show how variables such as auxiliary switch peak current and peak voltage vary as circuit parameters are changed. These curves are obtained from analytically solving the equations given in the steady state analysis by using an iterative procedure such as the Newton-Rapson method. The auxiliary characteristic impedance is given by

$$Z_a = \sqrt{\frac{L_a}{C_a}}$$

(3)

The curves are drawn for particular values of the variable $K = C_p/C_a$. The value of the dc blocking capacitors $C_1$ and $C_2$ are taken to be constant (i.e. $C_1=C_2=0.47 \mu F$) because these circuit parameters have almost no significant bearing on the characteristic curves. This section attempts to analyze the inverter and its characteristic curves in order to provide a detailed design which leads to obtain both the minimum auxiliary circuit rating and reduce its conduction losses. The procedure of choosing suitable value of the coefficient $K$ and auxiliary resonant impedance $Z_a$ is discussed in sections A through E.

**A. PEAK CURRENT OF AUXILIARY SWITCH $i_{3p}$**

Fig. 3 shows the variation of peak current of the auxiliary switch $Q_3$ ($i_{3p}$) versus auxiliary resonant impedance $Z_a$. From the graph it is clear that the value of the $i_{3p}$ decreases with increasing $Z_a$ for all $K$, this is because by increasing $Z_a$, the auxiliary resonant inductance $L_a$ is being increased compare to $C_a$ as seen in Eq. (3). Additionally, for the output power of 3200 W the output peak current is about 56.57 A. therefore to obtain both the minimum auxiliary circuit rating and reduce its conduction losses it is reasonable to choose the ratio of $i_{3p}/i_{op}$ less than one. With reference to Fig. 3, it can be deduced that $Z_a$ should be chosen bigger than 0.3 pu. The value of the coefficient $K$ does not affects the curve significantly.

![Peak current of the auxiliary switch $Q_3$](image)

**B. PEAK VOLTAGE ACROSS AUXILIARY SWITCH $V_{3p}$**

Fig. 4 shows the peak voltage across auxiliary switch...
versus the resonant impedance $Z_a$ in pu. From the curve it is clear that the peak voltage across switch, $V_{3p}$ increases as $Z_a$ increases. From both the previous section discussion, choosing $Z_a > 0.3$, and Fig 4 it can be concluded that to reduce the rating value of auxiliary switch it is reasonable to choose the coefficient $K$ bigger than one.

C. ZVS INTERVAL OF MAIN SWITCH $Q_1$ AT TURN-OFF

The variation of the ZVS available turn-off interval of $Q_1$ versus resonant impedance, $Z_a$ is shown in Fig. 5. From the graph it is clear that for $K \geq 1$ the ZVS interval decreases with increasing $Z_a$. With reference to Fig. 5 it can be deduced that by increasing $K$ the time interval $[t_2-t_1]$, in which the load current flowing through body diode of $Q_1$ is increased. This increased conduction of diode results in a much more ZVS interval available for turning-off. So it could be suitable to choose $K=3$ and $Z_a=0.3$.

D. ZVS INTERVAL OF MAIN SWITCH $Q_2$ AT TURN-ON

The graph shows variation of ZVS interval of main switch $Q_2$ versus resonant impedance, $Z_a$. As it can be seen from the graph, shown in Fig. 6, it is clear that for $K = 3$ and $Z_a= 0.3$ the ZVS interval of main switch $Q_2$ states in a good condition. This section is the time interval $6 [t_5-t_6]$ with respect to Fig.9.

E. PEAK CURRENT OF MAIN SWITCHES $Q_1$ AND $Q_2$

Fig. 7 shows variation of peak currents $i_{1p}$ and $i_{2p}$ of the main switches ($Q_2$ and $Q_1$) versus $Z_a$. It is clear that, if we choose $Z_a \geq 0.4$ and $K \geq 3$ the peak currents maintain at their almost minimum values during the operation condition. Consequently, in order to decrease the peak currents of all switches, it could be suitable to choose the parameters $K$ and $Z_a$ as follows:

$$Z_a \geq 0.4$$

$$K \geq 3$$

IV. DESIGN PROCEDURE AND EXAMPLE

This section presents the design procedure for selecting the auxiliary circuit components from the characteristic curves given in previous section.

A. INPUT DATA

A design example is also given for fully understanding the procedure. The following assumption is made to provide a reasonable design procedure.

$$f_a = 5 \times f_s$$

Where, $f_a$ and $f_s$ are the resonant frequency of the auxiliary circuit and switching frequency respectively. The switching frequency is about 20 kHz.
Basic values:
Base Voltage: The DC link voltage, $V_{dc}$ is taken as the base voltage
\[ V_b = V_{dc} = 310 \text{ V} \] (7)

Base Current: The maximum output current is taken as the base current
\[ I_b = \frac{\sqrt{2} P_a}{V_{dc}} = \frac{\sqrt{2} \times 3200}{0.95} \times 310 = 15.36 \text{ A} \] (8)

Base Impedance:
\[ Z_b = \frac{V_b}{I_b} = \frac{310}{15.36} = 20.1735 \text{ } \Omega \] (9)

B. CALCULATING THE AUXILIARY INDUCTOR AND CAPACITOR

From (4) and (6) we have $Z_a = \frac{V_a}{I_a} = 0.4 \text{ pu}$ and $f_p = \frac{1}{\sqrt{C_a L_a}} = 100 \text{ kHz}$. So the auxiliary inductor and capacitor are obtained $L_a = 12.843 \text{ } \mu \text{H}$ and $C_a = 0.19723 \text{ } \mu \text{F}$.

C. CALCULATING THE PARALLEL CAPACITOR $C_p$

From Eq. (5) the parallel capacitor is obtained $C_p = 0.5917 \text{ } \mu \text{F}$.

In the next section simulation results will be given to prove the validity of the design which has been discussed in this section.

IV. PROPOSED INVERTER OPERATION INTERVALS

The operation intervals of the inverter are shown in Fig. 8. Explanation of each interval is carried out on the basis of the illustration for the circuit operation conditions and the results of simulation analysis at $D = 0.46$, shown in Fig. 9. Fig. 1 defines the signal and the positive direction of each voltage and current in the inverter. The operation of each interval and the transition between the intervals are described as follows:

Interval 1 [$t_0$-$t_1$]: When $Sw1$ is turned on, the resonant current $i_R$ begins to flow through the load. Accordingly, the output power is supplied into the load from the DC link source voltage, $V_{dc}$. Then, $Sw3$ turns on so that the auxiliary resonant current $i_j$ begins to flow via $L_a$ and $C_a$. Accordingly; interval 1 is converted to interval 2.

Interval 2 [$t_1$-$t_2$]: During this interval, both $Sw1$ and $Sw3$ turn on. The current flowing through $Sw1$ ($i_j$) is forced to convert into diode $D_1$ owing to the auxiliary resonance between $L_a$ and $C_a$ mentioned above. The active power switch $Sw3$ turns on under ZCS operation due to the current $i_j$. The current $i_j$ begins to charge $C_a$. When the current $i_j$ is converted from $Sw1$ into $D_1$, interval 2 is transferred into interval 3.

Interval 3 [$t_2$-$t_3$]: When $Sw1$ turns off while diode $D_1$ is conducting, so it turns off under ZCS and ZVS condition. As the current flowing through the diode $D_1$ is removed by the auxiliary current $i_j$, diode $D_1$ turns off so that interval 3 changes to interval 4.

Interval 4 [$t_3$-$t_4$]: The auxiliary resonant current flows through $C_a$, the load ($R_p$ and $L_a$), $C_3$ and $C_4$ via $Sw3$. When the voltage across $C_a$ goes over the DC link source voltage of $V_{dc}$, the diode $D_3$ in the switchers $Q_3$ becomes conducting. Hence, interval 4 becomes interval 5.

On the other hand, when this interval jumps from interval 7, as shown in Fig. 8, the current flowing through $Sw3$ is removed by the resonance among $L_a$ and $C_a$. Then, $D_3$ turns on and this interval returns into interval 8.

Interval 5 [$t_5$-$t_6$]: During this mode, the current $i_j$ flows through $D_3$ so that the active switch $Sw3$ can be turned off under ZCS and ZVS condition as cutting off the gate signal fed to $Sw3$. When $D_3$ turns off while $D_1$ is conducting this interval is converted into interval 6.

Interval 6 [$t_6$-$t_7$]: As it is shown in Fig. 9 the current, $i_j$ is reversed in its direction and resonant current flows through load, $C_3$ and $C_4$. The current flowing through $D_3$ is removed as the resonant load current reaches zero. While $D_1$ is conducting, the gate signal is fed to $Sw2$ to turn it on. Then, the current flowing through $D_3$ can be converted naturally into $Sw2$. So that $Sw2$ turns on under ZCS and ZVS condition. As $Sw2$ turns on this interval turns to interval 7.

Interval 7 [$t_7$-$t_8$]: As the gate signal of $Sw2$ in cut off the switch turns off under some turning off current. So some turn off losses occur during this interval. Simultaneously, $Sw3$ turns on under ZVC condition because of auxiliary resonance circuit.

Interval 8 [$t_8$-$t_9$]: by applying the gate signal of $Sw1$ it turns on under ZVS condition due to the auxiliary resonance current. The resonance current between $L_a$ and $C_a$ goes to completion and the current flowing through $D_3$ reaches zero therefore $D_3$ turns off during this interval. Then, $Sw3$ turns on under ZCS and ZVS condition and the interval returns into the initial interval (interval 1).

V. CONCLUSION

This paper presents a ZVS PWM half-bridge inverter with active soft switching auxiliary circuit. This inverter featured soft switching of both the two main switches and the auxiliary switch. Additionally it reduces both peak flowing current of all switches and voltage of the auxiliary switch to achieve low switching stress. The step-by-step design procedure, based on the inverter characteristic curves of the inverter, has been given.

The results of computer-aided simulation analyzer, PSCAD/EMTDC are provided to indicate both the circuit operation intervals and evaluation of the performance of the proposed inverter.
Fig. 8. Operating principle and equivalent circuits during one switching cycle

Fig. 9. One switching cycle operating waveforms at $D=0.46$

REFERENCE


