A Novel Square Root Domain Lossless Integrator and Its Application to KHN Biquad Filter Design

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Abstract

In this paper, a novel square root domain lossless integrator and its application to KHN (Kerwin-Huelsman-Newcomb) biquad are proposed. The presented lossless integrator based on quadratic characteristics of MOS transistor was designed by using state space method. It consists of a geometric mean circuit, a current mirror and a capacitor. The scaling factor of the integrator is electronically tuneable by an external bias current. The KHN biquad consists of two lossless integrator blocks and a summer circuit. The summer circuit is developed by using linear transconductors. KHN biquad filter was simulated by using SPICE simulation program, simulation results are good in agreement with the theoretical analysis.

1. Introduction

There is a growing research area of square root domain circuits. Square root domain circuits are based on quadratic relationship between drain current (I_D) and gate-source voltage (V_{GS}) of the MOS transistors operating in strong inversion and MOS translinear principle [1,2]. Square root domain circuits are subclass of continuous time companding (compressing-expanding) circuits [3,4]. Due to their companding nature, square root domain circuits are suitable for low voltage, low power, large dynamic range, high frequency applications, and electronic tuneability [1,2,4,5]. Since the circuits are designed with MOS transistors operating in the saturation region, square root domain circuits are very compatible with CMOS VLSI technology. There are different synthesis methods for square root domain circuits as state space synthesis, signal flow graph synthesis, and the substitution of the LC ladder of the corresponding prototype by their square root domain equivalents in the literature [1,5,6]. In the state space synthesis method, the state space description of the transfer function is mapped on the state variables [7]. This method is also suitable for externally nonlinear internally nonlinear circuits [8] like square root domain circuits.

In the literature, a square root domain lossless integrator designed by using signal graph method was proposed in [9]. This lossless integrator consists of geometric-mean and multiplier/divider circuit blocks. In this work, a new square root domain lossless integrator is designed by using state space synthesis method. The proposed lossless integrator consists of only a geometric mean circuit.

Lossless integrator circuits are useful for designing high-order filters and biquad filters. In this study, a KHN biquad filter that is constructed with two lossless integrator and a summer blocks was presented. The KHN filter provides lowpass, highpass and bandpass filter outputs at a time. The cut-off frequency and quality factor of the presented voltage-mode KHN filter can be electronically tuneable.

Due to decreasing in dimensions of MOS transistors, the secondary effects cause deviations in ideal characteristics of MOS transistors. In literature, there is a method to reduce these deviations [10]. By using this method the performance of the circuit can be improved. Also, by using larger dimensions, the influence of these deviations on the accuracy of the circuit is reduced.

In literature, KHN biquads were designed with opamps [11], current conveyors [12]. The proposed filter in square root domain has compact structure, larger dynamic range and greater linearity. As a companding circuit, a KHN biquad was introduced by Tola et al [13]. The main advantage of the square root domain biquad presented is integrability.

2. Proposed Square Root Domain Lossless Integrator

The presented lossless integrator was designed by using state space method. This method relates internally nonlinear filters to equivalent linear systems [14]. A state equation consists of a set of first-order differential equation. The state variables are equal to simple functions of square root of currents in the square root domain circuits. General transfer function of the lossless integrator is

$$H(s)=\frac{Y(s)}{U(s)}=\frac{k}{s} \tag{1}$$

where k is a scaling factor of integrator. The state space representation of the integrator is expressed as

$$\dot{x}=ku \tag{2}$$

$$y=x \tag{3}$$

If the node voltage V_1 and voltage signal U are assumed the state variable x and u, state equations (2) and (3) are rewritten as

$$C\dot{V}_1=kCU \tag{4}$$

$$y=V_1 \tag{5}$$

where C is a scaling constant. In the square root domain circuits state equations represent the branch currents. If C symbolized a capacitor connected between V_1 voltage and ground, left side of the equation (4) is the current of this capacitor. When U is the gate-source voltage of a MOS transistor operating in saturation region, and I_u is the drain current of the MOS transistor, so equation (4) is arranged as

$$C\dot{V}_1 = kC(\sqrt{\frac{I_u}{\beta}} + V_{TH}) \tag{6}$$

where $I_u = \beta(U - V_{TH})^2$, β and V_{TH} are transconductance parameter and threshold voltage of the MOS transistor, respectively. Hence, the state equation in (6) is transformed into

$$I_C = \sqrt{I_o I_u} + I_{TH} \tag{7}$$

where capacitor's current $I_C = C\dot{V}_1$, the bias current $I_o = k^2C^2/\beta$, and threshold voltage compensation current $I_{TH} = kCV_{TH}$. By changing the bias current, the scaling factor of the lossless integrator can be tuneable. According to the state and output equations, the schematic of the lossless integrator is shown in the Figure 1.

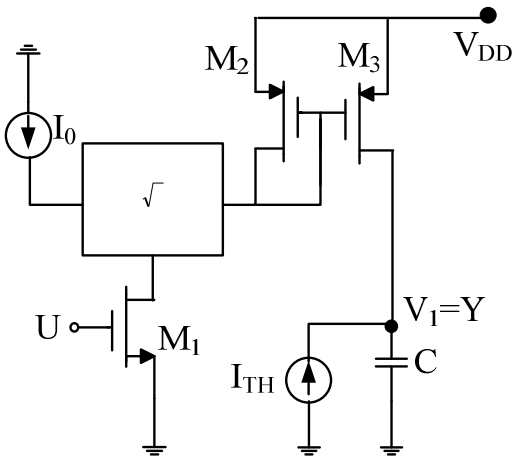

Fig. 1. The proposed square root domain lossless integrator

3. Design of KHN Biquad using Proposed Lossless Integrator

KHN biquad filter consists of two integrators and a summer block, as shown in Figure 2 [15]. To realize the biquad in square root domain, KHN biquad block is modified as shown in Figure 3. With the nodal analysis, the transfer functions of highpass, bandpass, and lowpass are respectively;

$$H_{hp}(s) = \frac{s^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{7}$$

$$H_{bp}(s) = H_{hp}(s).\frac{\omega_0/Q}{s} = \frac{(\omega_0/Q)s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{8}$$

$$H_{lp}(s) = H_{hp}(s).\frac{\omega_0^2}{s^2} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{9}$$

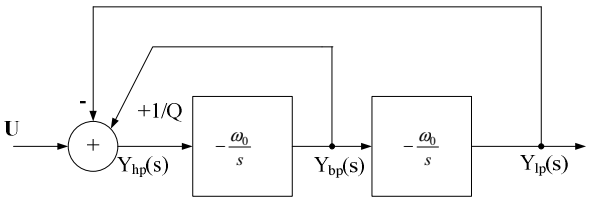

Fig. 2. Block diagram realization of KHN biquad filter

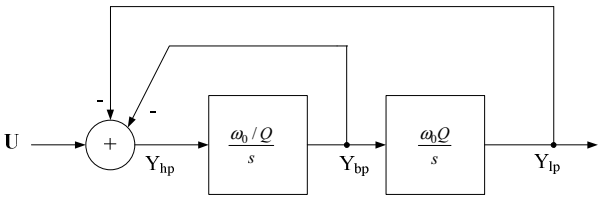

Fig. 3. Modified KHN biquad filter block diagram

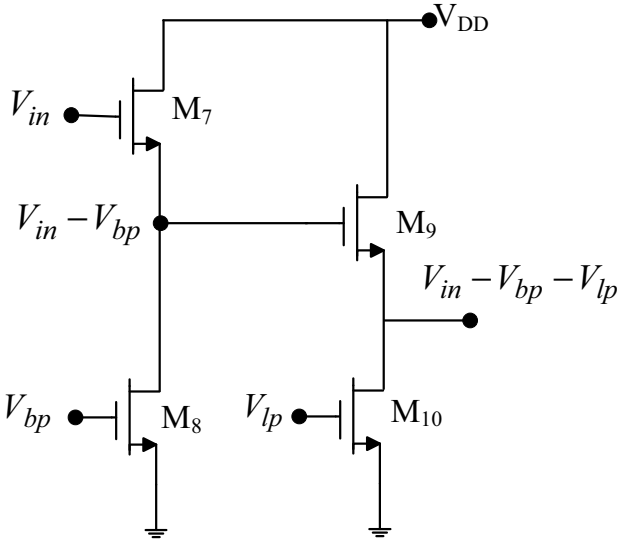

Fig. 4. The summer circuit with linear transconductor based on the MOS transistor square law characteristic

In this work , highpass, bandpass, and lowpass responses of the biquad were simulated. Additionally, notch and allpass responses can be obtained by summing highpass and lowpass, and by subtracting the bandpass from notch response, respectively.

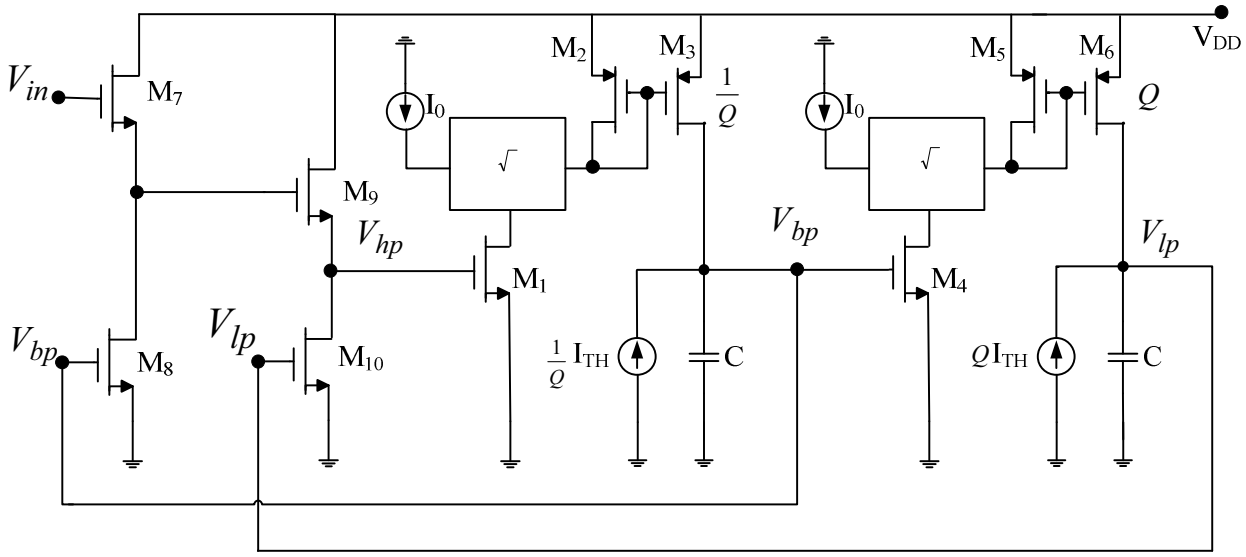

Fig. 5. The schematic of square root domain KHN biquad filter

The newly introduced lossless integrator was used for integrator blocks in KHN biquad. For summer block, a circuit that performs $V_{in} - V_{bp} - V_{lp}$ was designed by using linear transconductor based on MOS transistors square law [16]. The summer circuit is shown in the Figure 4.

The schematic of the square root domain KHN biquad filter constructed with two lossless integrators and a summer block is shown in Figure 5. In KHN biquad the bias current is $I_o = \omega_0^2 C^2 / \beta$ and the threshold voltage compensation current $I_{TH} = \omega_0 C V_{TH}$. The cut off frequency of the filter responses can be adjustable by the bias current and the quality factor Q is tunable with W/L parameters of the MOS transistors in the current mirrors.

4. Simulation Results

To verify the theoretical study, KHN biquad filter was simulated by using SPICE simulation program using TSMC 0.25µm CMOS model parameters. The circuit supply voltage was 2.5V. The geometric mean circuit in [17] was used for the simulation. The values of capacitance of the lossless integrators were chosen 15pF. Figure 6 shows the gain characteristics with ideal responses of highpass, bandpass, and lowpass with the values of the bias currents were 100µA, the transconductance parameter β was 95.02µA/V^2, and the quality factor was 1. Under these conditions the theoretical cut off frequency of the filter was 1.04 MHz, while the simulation result was 1MHz. The power dissipation was 2.05mW. Under the same conditions Figure 7 shows the simulated and ideal gain responses of the highpass filter, while the bias current I_0 was changed from 40µA to 100µA, simultaneously indicates tuning of the cut off frequency from 647 KHz to 1MHz.

For different quality factor from 0.2 to 5, while the bias current was 60µA, bandpass filter response is demonstrated in Figure 8. In the direction of the simulation results, the heoretical and simulation results are in good agreement.

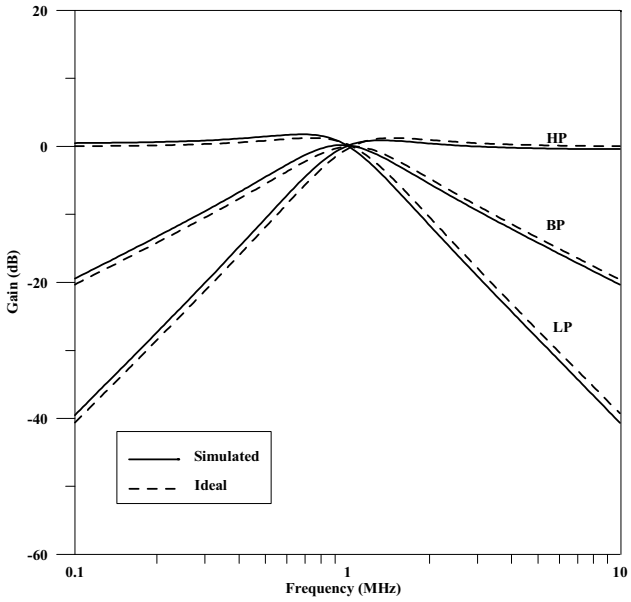

Fig. 6. Simulated gain responses of the proposed KHN biquad for the fundamental filter functions

5. Conclusion

In this paper, a square root domain lossless integrator was presented. This is the first square root domain lossless integrator that is designed by using state space synthesis method in the literature. It has a simple structure and can be electronically tuneable. As an application of lossless integrator a KHN biquad was also proposed in square root domain. KHN biquad has properties as tuning of quality factor and cut off frequency. Simulation results are confirmed the theoretical results. Because of the compatibility of square root domain circuits to CMOS VLSI technology, both presented lossless integrator and KHN biquad filter are appropriate to implement as an integrated circuit.

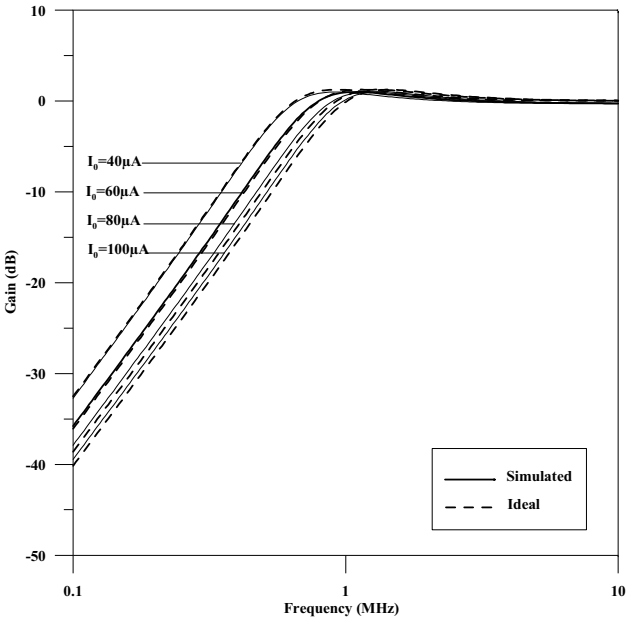

Fig. 7. Simulated gain response of the highpass filter, while I_0 was changed from 40µA to 100µA.

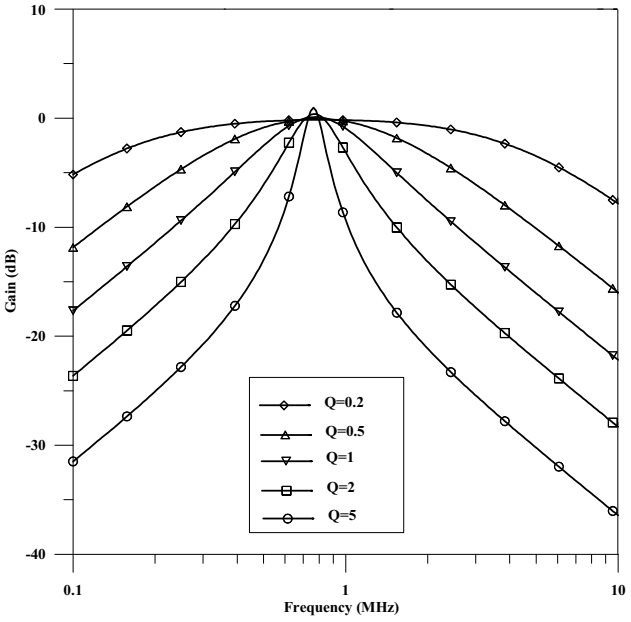

Fig. 8. The quality factor tuning for bandpass filter

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