# AN IMPROVED ZERO-VOLTAGE-TRANSITION INTERLEAVED BOOST CONVERTER WITH HIGH POWER FACTOR

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## Abstract

**In this paper, an improved Zero-Voltage-Transition (ZVT) two-cell interleaved boost Power Factor Correction (PFC) converter is proposed and investigated. A new auxiliary circuit is designed and added to two-cell interleaved boost converter to reduce the switching losses. Only one auxiliary switch is used in the active soft switching auxiliary circuit. The main advantage of this auxiliary circuit is that it not only provides ZVT in the boost switches but also provides soft switching in the auxiliary switch and passive diodes. Therefore, the switching losses of the converter can be reduced. Compared to the previous published soft switching interleaved boost converters, only one auxiliary switch is needed in the auxiliary unit, so the auxiliary unit and control circuit are simple. A 1kW, 50 kHz two-cell interleaved boost PFC converter with an improved ZVT auxiliary circuit has been simulated using average current control method and the results are presented. Simulation results show that the main switches, the auxiliary switch and passive diodes are operating under soft switching mode.**

## 1. Introduction

Boost converters are widely used as power-factor-corrected pre-regulators. In high power applications, interleaved operation (the parallel connection of switching converters) of two or more boost converters has been proposed to increase the output power and to reduce the output ripple [1-5]. This technique consists of a phase shifting of the control signals of several cells in parallel operating at the same switching frequency. As a result, the input and output current waveforms exhibit lower ripple amplitude and smaller harmonics content than in synchronous operation modes. The resulting cancellation of low-frequency harmonics allows the reduction of size and losses of the filtering stages.

However, hard switched PWM converters have low conduction losses and high switching losses. The switching losses of the boost switches create a significant amount of power dissipation in high power application. Since high power density requires high-frequency (HF) operation and high efficiency, the switching losses have to be minimized. In order to minimize switching losses, various kinds of soft switching techniques have been proposed in the literature [6-14]. The soft switching boost converter proposed in [6] achieved soft switching while maintaining its PWM characteristics. The main switch undergoes ZVT, while the auxiliary diodes used are hard switched. The reverse recovery of the auxiliary diodes causes parasitic oscillations increasing the stresses. The most preferred scheme proposed in [7] provides zero voltage switching condition for the main switch without increasing the voltage stress of the switching devices. However, it has drawback such as the hard switching of the auxiliary switch, which deteriorates the overall efficiency and increase the EMI noise. There have been many attempts to solve these problems.

In this study, after discussed the basic soft switching topologies proposed in the literature, the proposed ZVT interleaved boost topology is introduced. The operation modes of the proposed topology for Continuous Conduction Mode (CCM) are analyzed in Section 2. Then, the proposed topology is simulated via Spice and Simplorer simulation programs. Since the Spice program includes the models of real components, this program is used to prove the contribution of this study. For the same conditions, the interleaved hard-switched boost converter and proposed ZVT interleaved boost converter are simulated via Spice program and the results are recorded. Also, the proposed topology (Fig.1) is simulated via Simplorer using average current control method to observe the power factor (pf) and Total Harmonic Distortion (THD) of the topology. The results are discussed in Section 3.

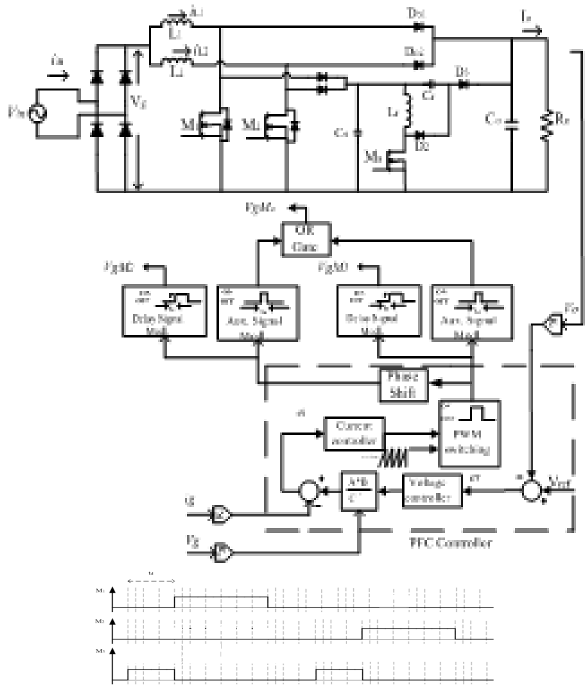


**Fig. 1.** The proposed ZVT two-cell interleaved boost PFC converter and its switching pattern

## 2. Analysis of Operation

The typical waveforms and the equivalent circuits of the operating modes of the proposed converter for D>0.5 (in one switching cycle) are shown in Fig. 2 and 3 respectively. The related waveforms and the equivalent circuits of the converter for D<0.5 can be derived in the same manner. Two current sources are considered for the input stage of the equivalent circuits because of the inductors. Also, the output stage of the equivalent circuits is considered as a voltage source due to the large output capacitor. To simplify the analysis, all the components are assumed ideal and the input boost inductors are assumed large enough to neglect the input current ripple. Also, the resonant circuit is assumed as ideal. As shown in Fig. 2, sixteen operation modes exist within one switching cycle;

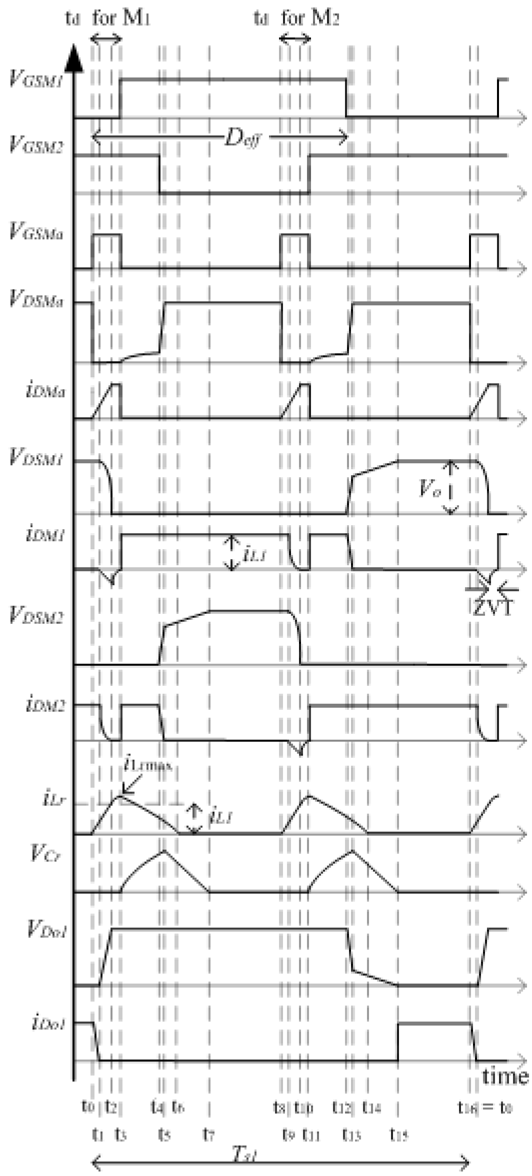
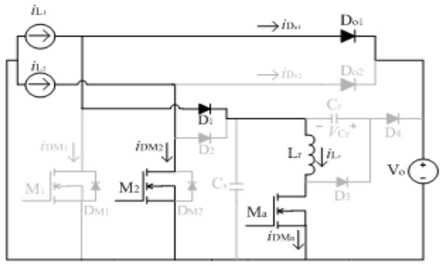
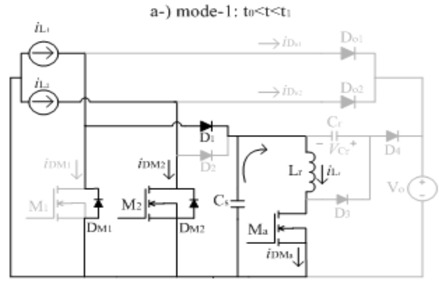


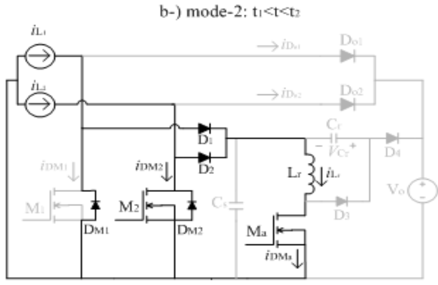

**Fig. 2.** Operating waveforms of the proposed converter for one switching cycle (for D>0.5)



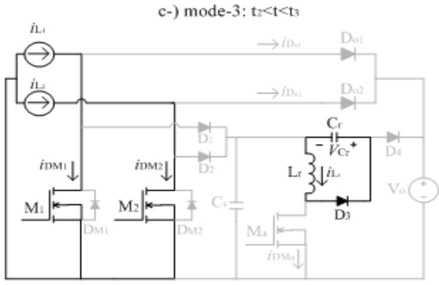
a-) mode-1: $t_0<t<t_1$



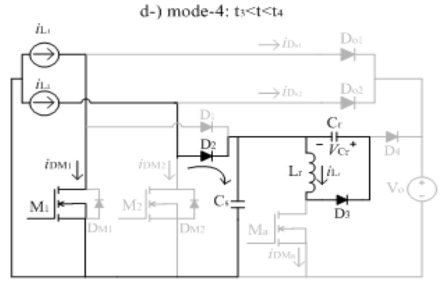
b-) mode-2: $t_1<t<t_2$



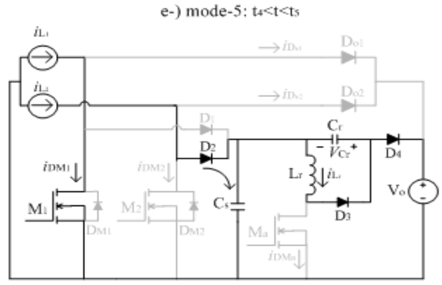
c-) mode-3: $t_2<t<t_3$



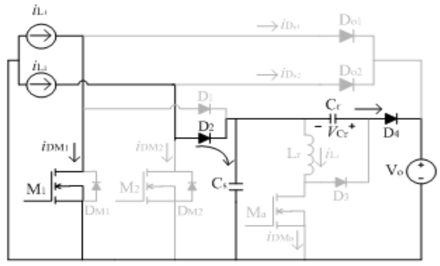
d-) mode-4: $t_3<t<t_4$



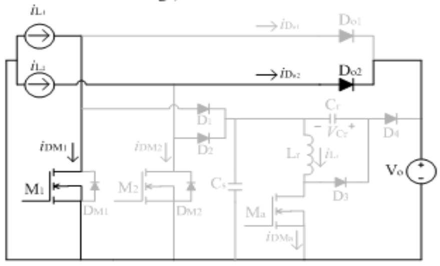
e-) mode-5: $t_4<t<t_5$



f-) mode-6: $t_5<t<t_6$



g-) mode-7: $t_6<t<t_7$



h-) mode-8: $t_7<t<t_8$

**Fig. 3.** The equivalent circuits of the operating modes (for D>0.5) in one switching cycle

_Mode-1;_ ($t_0$-$t_1$) [Fig.3.(a)]. Before $t_0$, the main switch $M_1$ and the auxiliary switch $M_a$ are off, and the output diode of the firs stage is on state. At $t_0$, $M_a$ is turned on. The resonant inductor ($L_r$) current starts to rise through the path of Vin-$L_1$-$L_r$-$M_a$-Vin. In this interval the output diode is turned off with soft-switching. Therefore, the reverse recovery loss of *Do* is greatly reduced. Since the voltage across the $C_s$ is equal output voltage (*Vo*) in this interval, this time interval and current of $L_r$ can be expressed;

$$i_{L_r}(t)=\frac{V_{Cs}}{L_r}(t_1-t_0)=\frac{V_o}{L_r}(t-t_0) \tag{1}$$

$$V_{C_r}(t)=0 \tag{2}$$

$$(t_1-t_0)=\Delta t_1=\frac{I_{L1}L_r}{V_o} \tag{3}$$

_Mode-2;_ ($t_1$-$t_2$) [Fig.3.(b)]. $C_s$ begins to discharge and $L_r$ current increases because of the resonance between $L_r$ and $C_s$. $C_s$ is discharged until its voltage reaches zero at $t_2$. The resonant time period of this interval, $L_r$ current and voltage across $C_s$ are given by;

$$i_{L_r}(t)=I_{L1}+\frac{V_o}{Z_1}\sin w_1(t-t_1) \tag{4}$$

$$V_{C_s}(t)=V_o\cos w_1(t-t_1) \tag{5}$$

$$(t_2-t_1)=\Delta t_2=\frac{\pi}{2}\sqrt{L_rC_s} \tag{6}$$

where, $\omega_1=1/\sqrt{L_rC_s}$ and $Z_1=\sqrt{L_rC_s}$

_Mode-3_; ($t_2$-$t_3$) [Fig.3.(c)]. At $t_2$ snubber capacitor $C_s$ is fully discharged and $L_r$ current reaches its maximum value. In this interval, $L_r$ current flows in $L_r$-$M_a$-Body diodes of the main switches. Maximum $L_r$ current can be expressed as;

$$i_{L_r}(t)=I_{L_r\max}=I_{L1}+V_o/Z_1 \tag{7}$$

$$V_{C_r}(t)=0 \tag{8}$$

In this interval, the main switch should be switched to satisfy the ZVT condition. The delay time, $t_d$ can be expressed as;

$$t_d=\Delta t_1+\Delta t_2=\frac{I_{L1}L_r}{V_o}+\frac{\pi}{2}\sqrt{L_rC_s} \tag{9}$$

As seen from equation(9), the worst case occurs at maximum input current. Therefore, the auxiliary circuit parameters must be selected according to the worst case.

_Mode-4_; ($t_3$-$t_4$) [Fig.3.(d)]. At $t_3$, the auxiliary switch is turned off and $M_1$ is turned on at the same time. In this mode two main switches conduct the input current together. Auxiliary capacitor $C_r$ begins to charge up and $L_r$ current begins to fall until the end of this mode.

_Mode-5_; ($t_4$-$t_5$) [Fig.3.(e)]. This mode starts by switching of the main switch, $M_2$. The energy transfer from $L_r$ to $C_r$ is continuing. begins to $M_1$ and $D_{o2}$ are conduct.

_Mode-6_;($t_5$-$t_6$) [Fig.3.(f)]. At $t_5$, $M_2$ current falls to zero. The auxiliary capacitor begins to discharge and $C_s$ begins to charge up.

_Mode-7_;($t_6$-$t_7$) [Fig.3.(g)]. At $t_6$, the current of $L_r$ is zero. In this mode, only the main switch, $M_1$ conducts. $C_s$ continues to charging up to the output voltage.

_Mode-8_; ($t_7$-$t_8$) [Fig.3.(h)]. When the voltage across the $C_r$ falls to zero the output diode of the second stage starts to conduct. In this mode, the input current is shared between $M_1$ and $D_{o2}$.

_Mode-9-16;_ Since the proposed converter is $180^0$ phase shifted with identical frequencies and duty ratios, the last eight modes are the same as the before modes. Only the roles of the main switches and output diodes change.

## 3. Results and Discussion

First, the proposed ZVT interleaved boost topology and hard-switched interleaved boost topology have simulated via Spice simulation program using the same condition (for 1kW output power, 50kHz/cell switching frequency and 0.3 duty cycle). The voltage-current of the switches and switching losses of the converters are recorded and compared. The related results are shown in Fig. 4-5. Then, the proposed ZVT interleaved boost PFC topology is simulated via Simplorer 6.0 simulation program to observe the topology and switches' voltage-current waveforms, power factor and Total Harmonic Distortion (THD) of the topology (Fig. 6-12). The parameters in Table 2 are used for simulation studies.

**Table 2.** Parameters used in the Simulations

| ***Parameters*** | ***Values*** |
|---|---|
| Input voltage, $V_{in}$ | 220 VAC, 50Hz |
| Output voltage, $V_o$ | 400V |
| Switching frequency | 50kHz/cell |
| Output power | 1kW |
| Inductances ($L_1$, $L_2$) | 1mH |
| Output capacitance | 470µF, 450V |
| Auxiliary inductance ($L_r$) | 15µH |
| Auxiliary capacitance ($C_r$) | 250nF |
| Snubber capacitance ($C_s$) | 2nF |
| Power Switches ($M_1$ $M_2$ $M_a$) | IRFP460 |

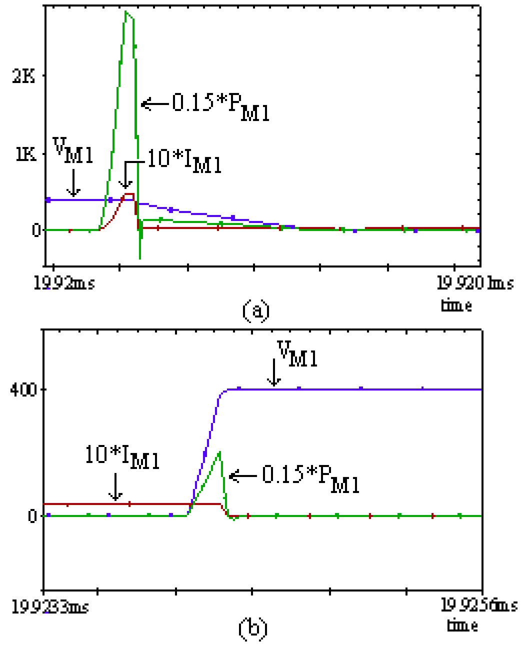
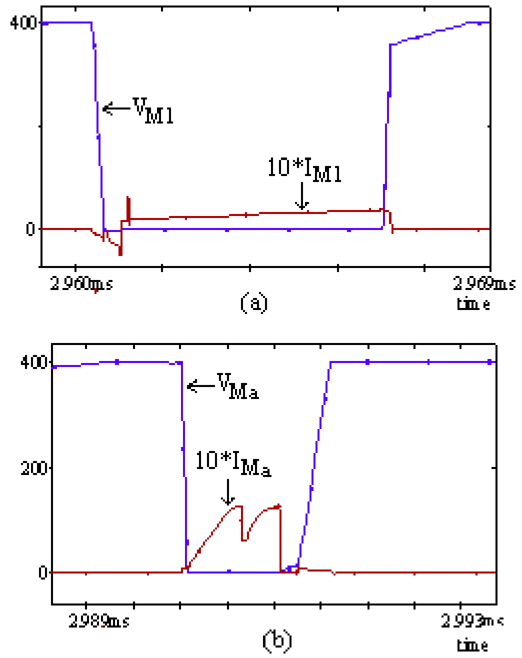



**Fig. 4.** Spice simulation results of the hard-switched two-leg interleaved boost topology, (a) for ON-time (b) for OFF-time (Green is Power loss) [**Avg ($PM_1$+$PM_2$)=32W**]

As seen from Fig. 4 and 5 the total switching loss of the hard switched two-leg interleaved topology is higher than the proposed ZVT interleaved topology. While the total switching loss is 32W for hard switched interleaved boost circuit, the total switching loss of the proposed topology is 16+6=22W (16W for the switches and 6W for the passive components of the auxiliary circuit). The Spice simulation has been done for the worst case (maximum input current and minimum duty cycle for 1kW output power).



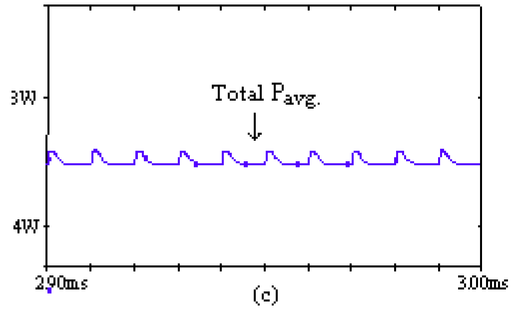




**Fig. 5.** Spice simulation results of the proposed ZVT interleaved boost topology, (a) $VM_1$-10*$IM_1$; (b) $VM_a$-10*$IM_a$; (c) AvgP(Auxiliary circuit) waveforms.
[**Avg ($PM_1$+$PM_2$+$PM_a$)=16W**]; [**Avg ($PL_r$+$PD_{passives}$=6W**]

As shown in Fig. 6, the output voltage of the topology is obtained as 400V with a small ripple. Fig. 7 shows the input voltage and current waveforms without any EMI filter. This result shows that the obtained power factor and THD of the input current are suitable for international standards (European Norm EN61000-3-2.).

The total inductors' current and the current of each inductor of the proposed topology are shown at Fig.8. The input ripple current is significantly reduced compared to the two independent inductors current ripple. Since the two phases of the circuit work with the 180 degree phase shift, the input current ripple minimization is best at duty cycle of 0.5.

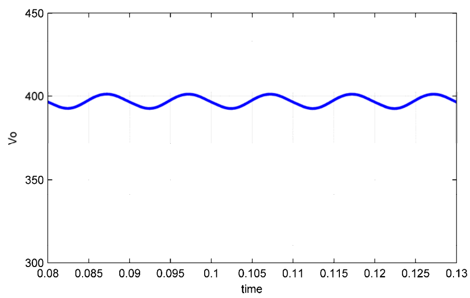



**Fig. 6.** Simplorer simulation result of output voltage (400V)

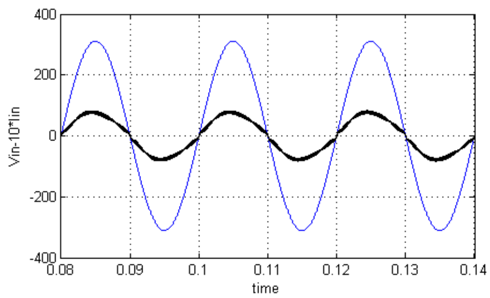



**Fig. 7.** Simplorer simulation result of input voltage-current ($V_{inrms}$=220V; $I_{inrms}$=4.63A) waveforms ; ***(pf=0.989, THD=8%)***

Figure 9 and 10 show the voltage and current waveforms of the main switch (M1) and auxiliary switch (Ma). As seen from the results, the ZVT is achieved for main switch and ZVS is achieved for the auxiliary switch. Also, it is observed that the Simplorer and Spice simulation results are same.

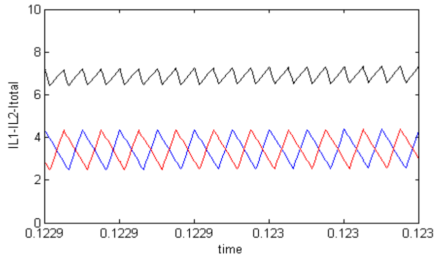



**Fig. 8.** Simplorer simulation result of inductors' current and total current waveforms

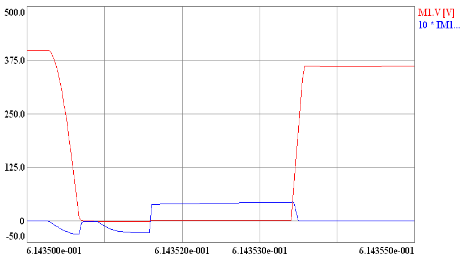



**Fig. 9.** Simplorer simulation result of main switch (M1) voltage-current waveforms

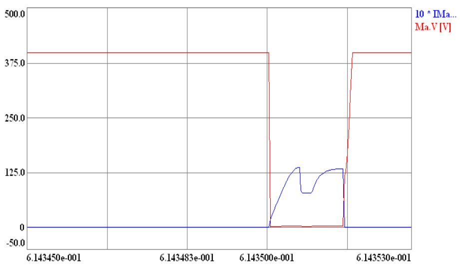



**Fig. 10.** Simplorer simulation result of auxiliary switch (Ma) voltage-current waveforms

## 4. Conclusions

In this paper an improved ZVT interleaved boost PFC converter is presented. A new auxiliary circuit for two-leg interleaved boost PFC converter is designed and analyzed. The proposed ZVT interleaved boost topology and hard-switched interleaved boost topology have been simulated via Spice simulation program using the same condition (for 1kW output power, 50kHz/cell switching frequency). The voltage-current of the switches and switching losses of the converters are recorded and compared. As seen from the results, the main switches are turned on with ZVT and turned off with ZVS. Also, the auxiliary switch and the other diodes used in the auxiliary circuit are turned on and off with ZVS.

This soft switching of the auxiliary switches is the main advantage of the proposed converter. In addition, the soft switching of output diodes reduces switching losses. The simulation results show that the total switching losses of the hard switched interleaved topology is reduced by applying the proposed auxiliary circuit. Using only one resonant inductor and minimum number of components in the auxiliary circuit does not cause a bulky converter. A prototype of the proposed topology has been designed and experimental study is under progress.

## 5. References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