STATE OF THE ART FOR LOW-NOISE AMPLIFIERS IN WIRELESS TRANSCEIVERS; TWO NEW WIDEBAND ALL-ACTIVE LNAS IN SiGe-BiCMOS TECHNOLOGY

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ABSTRACT

The aim of this paper is three-fold. First, it introduces the low-noise amplifier, its relevance in modern wireless communications receivers and the performance expected of it. Then, it presents an exhaustive review of the existing topologies, presenting their advantages and shortcomings. And finally, it introduces a new class of LNAs, based on current conveyors, describing the founding principle and the performances of two new LNAs, one single-ended and the other differential. Both these new LNAs offer the following notable advantages over existent topologies: total absence of passive elements (and the smallest LNAs in their respective classes); wideband performance, with stable frequency responses from 0 to 3GHz; easy gain control over wide ranges (0 to 20dB). Comparisons with other topologies prove that the new class of LNA implementations greatly advances the state of the art. These amplifiers are ideally suited to today's multi-band receivers.

I. INTRODUCTION

In recent years, the domain of wireless communications has undergone an unprecedented evolution, moving rapidly through a series of generations. Traditionally, a receiver is designed according to a set of specifications corresponding to a particular standard and is thus ill-adapted to treat other standards. However, the development of different standards is highly region-specific and to be truly mobile, a receiver must today be able to treat several standards simultaneously. This has led to a rapid development of various multi-standard handsets (and corresponding multi-band receivers). Thus, the development of wideband radio-frequency (RF) front-end topologies is necessary and hinges on the development of circuits whose frequency characteristics are stable over several gigahertz and whose impedances are matched over wide bands [1].

Moreover, multi-band receivers have been increasingly adopting differential topologies. Traditionally used in low frequency analogue circuitry, differential circuits are becoming popular in the RF section. These topologies are today adopted for individual components (low-noise amplifiers, power amplifiers), for entire front-ends and even for complete receivers. This increasing popularity can be attributed to the substantial advantages consequent to differential signal processing, but their use is not always possible because the consumption, area and noise of a differential device are all higher than its single-ended counterpart [2].

PLAN OF THE PAPER

Irrespective of the receiver architecture, the low-noise amplifier (LNA) constitutes one of the essential components. This indispensable element will be the subject of this paper. Section II introduces the LNA and defines the parameters used to characterise it. Different parameters deserve priority for different applications; trade-offs between these parameters will be described.

Section III will elucidate on the major topologies used in LNA design. Three major categories will be discerned: single-transistor, cascode-based and two-stage. Topologies of existent LNAs are similar for single-ended and differential amplifiers: the differential LNA is constructed by duplicating its single-ended counterpart.

In section IV, we will describe the founding principle of a new class of low-noise amplifiers based on current conveyors. The characteristics of the fabrication technology will also be described.

Sections V and VI will respectively present two new LNA solutions, one single-ended and the other differential based on the above principle. We will start with descriptions of the fabricated circuits, the measurement techniques, the measured performances. Although they give different performances, both are wideband (with respect to both the frequency response and wideband input and output impedance matching) and both allow gain control (from 0 to 20dB approximately). Thereafter, we will present comparisons of each of these LNAs with existent solutions taken from recent literature to highlight the advantages of the new class of LNAs. The paper will end with some concluding remarks (section VII).

II. THE LOW-NOISE AMPLIFIER

The principal role of the LNA is to enhance the level of the signal incident on its input, without introducing

significant noise and distortion. As the first real signal processing element after the antenna, the LNA determines the noise and linearity performance of the overall system. It is the most sensitive block in a typical RF receiver [3]-[5].

II.1 LNA PARAMETERS

The five fundamental parameters of the LNA are : gain and bandwidth, noise figure, linearity, impedance matching and power consumption [3], [6]-[8]. The goals in LNA design include minimising its noise figure, providing moderate to high gain with sufficient linearity, and establishing compatibility to other transceiver blocks (impedance matching). The additional constraint of low power consumption is imposed in portable systems.

II.1.1 Gain and bandwidth

The LNA is required to amplify incoming signals and extract them from the noisy environment, thus enabling signal processing by blocks further down the receiver chain. The gain provided by the LNA is generally defined in terms of the voltage gain ($A_V = V_{OUT}/V_{IN}$) or power gain ($S_{21} = P_{OUT}/P_{IN}$). Both are expressed in decibels by, for example, $A_{V,dB} = 20*\log_{10}(A_V)$. The bandwidth is defined as the frequency range where the gain is within 3dB of its peak value. Most LNAs are narrow-band (the ratio of bandwidth to operating frequency is low), but wideband circuits are gaining in importance because transceivers tend increasingly to be multi-mode and multi-standard.

II.1.2 Noise

The noise figure of the LNA is of prime importance. The total noise figure of a cascade of several noise-inducing components is defined as [9]:

$$F_{CASCADE} = F_1 + \frac{(F_2-1)}{G_1} + \frac{(F_3-1)}{G_1*G_2} + \ldots \quad (1)$$

where G_n and F_n correspond respectively to the gain and noise figure of the *n*th stage of the cascade. Since the LNA is the first component in this cascade, its noise figure adds directly to the overall noise. Therefore, in order to reduce the total noise of the receiver, the LNA should present the lowest possible noise.

II.1.3. Linearity

The input power of wireless standards extends over a wide range (in GSM, for example, the signal received at the antenna lies between -110dBm and -20dBm). The LNA should be able to receive and treat this entire range, while providing linear processing. However, because of the saturation of transistors, the gain saturates at high input power, and linearity comes into play. The LNA should be linear upto powers beyond the highest power likely to enter it. The 1dB compression point, generally referred to the input (IP_{1dB}), is the power at which the gain of the LNA drops 1dB below its steady linear value.

Another important indicator of the LNA's linearity is its 3rd-order intermodulation product. Wireless standards consist of several narrow receive channels. A strong blocker may be present in the channel adjacent to the one which has to be treated. This blocker (as strong as -15dBm in GSM) interferes with the main power tone, giving rise to "intermodulation products". This may saturate the LNA and block the receiver. The intermodulation product IP3, also generally referred to the input (IIP3), is an indicator of the linearity of the LNA. In carrying out intermodulation measurements on the LNA, two tones (the first is desired and the second is the blocker) are applied to the input. The spacing between these tones differs according to the communication standard, varying from 1MHz in GSM [10], 2MHz in WCDMA [11], to 200MHz in UWB [12]-[14]. A linear LNA can alleviate the performance requirement of the other blocks and thus lead to low power consumption and less silicon area of the overall receiver [15].

II.1.4. Impedance matching

The ports of the LNA should present impedances matched to desired values. Generally, the standard 50Ω impedance has been adopted because it lies between 77Ω for minimum cable losses and 30Ω for maximum power-handling capability of the transmission line [16]. The LNA is either placed immediately after the antenna, or follows a RF filter [3]. Impedance matching is important to avoid signal reflections on a cable or alterations of the characteristics of the pre-select filter which is sensitive to terminating impedances [17],[18].

Different matching considerations exist for the input and output. Input matching is always required, while output adaptation is necessary when the LNA drives an external image-reject filter. In integrated receivers where the image filter is driven by the antenna, the LNA can be directly connected to the mixer and no output matching is required [3]. As a general rule, input impedance matching determines the noise figure of the LNA. The output match effects linearity if a low output load (i.e., 50Ω) must be driven, as is almost always the case [3],[5],[16].

II.1.5. Trade-offs between LNA parameters

It is impossible to design a LNA which provides peak performance for all the five cardinal parameters. Trade-offs have to be made depending on the standard for which the LNA is destined. To reduce the noise of the receiver, the LNA's NF has to be low and its gain high (to reduce noise contributions from succeeding blocks). Since the noise figure of a transistor (and, by consequence, of the LNA) is inversely proportional to its collector current I_C, I_C can be raised indefinitely to reduce noise figure. However, a raised I_C entails higher consumption and goes

against the trend of low-consumption receivers. Although in some applications linearity and power consumption are perhaps equally important, these should not come at the expense of degradation in NF [19]. Sometimes, the linearity of the receiver is dominated by the stages which follow the LNA; in such cases, the primary goal is to minimize the power consumption for the required noise figure [7]. Moreover, high gain in the gigahertz range deteriorates the intermodulation distortion [3]. A high LNA gain is therefore not always desired. Using high LNA gain helps reduce NF by compensating for the insertion loss of the inter-stage filter and scaling down the noise contribution of the mixer, but at the expense of higher consumption and with the risk of early overloading of both the LNA output stage and the mixer [20].

II.2 LNA SPECIFICATIONS

A review of the specifications of various wireless standards and of the performance of existent LNA solutions allowed us to establish the expected LNA performance for each standard. Conventional narrowband LNAs should provide peak performance at the frequency for which they are designed. Wideband LNAs, on the other hand, are required to give stable performance over frequencies covering several hundreds of megahertz. Thus, LNA specifications are divided into two parts, one treating narrow-band and the other wideband LNAs.

II.2.1. Narrow-band LNAs

The LNA gain in GSM is required to be moderate, to minimise distortion and interference. The emphasis on noise figure is moderate (2dB), but linearity requirements are strict [10],[20]-[23]. In GPS, on the other hand, both the gain and the noise figure have to be extremely good : 20dB and 1dB, respectively, whereas linearity is only a secondary concern [24]. In PCS systems a -20dBm blocker can be expected at the LNA's input, and the LNA should give moderate gain and high linearity [21],[25]. The linearity requirement in WCDMA solutions is even more strict [11],[26]; obtaining IIP3 ~ 0dBm with low consumption (<5mA) is the major challenge here. WLAN LNAs have requirements which are less strict: moderate gain and noise figure, while allowing higher consumptions (~10mA) [25],[27].

II.2.2. Wideband LNAs

In wideband LNAs, the stringency of linearity and noise performance is exchanged for a wide bandwidth and moderate performance. The replacement of three or four narrow-band LNAs by one wideband one allows for enormous economies of power, area and cost. The gains provided by high-bandwidth LNAs are generally high (15 – 20dB), and the noise figure is required to be of the order of 3dB [13],[17].

III. REVIEW OF EXISTING LNAS

As mentioned above, the topologies used are essentially similar for single-ended and differential LNAs. Differential LNAs are generally realised by duplicating the single-ended circuit and can moreover be analysed and explained using their single-ended counterparts as the starting point [4],[28]. We were able to divide existent LNA solutions into three distinct categories: single-transistor, cascode-based and two-stage solutions.

III.1 ONE-TRANSISTOR SOLUTIONS

Members of the first class of LNAs use only one transistor in their signal chain.

III.1.1. Common-emitter/source LNA

The simplest realisation of a voltage amplifier is the common-emitter or common-source amplifier (fig. 1a). It is inherently narrow-band because the input matching circuit (comprising of inductors placed at the base and emitter of the transistor) can only be resonated at one single frequency. The output impedance matching is simply obtained by the load resistor. The biggest shortcoming of this simple solution is the difficulty of simultaneously matching the port impedances for optimum power transfer and minimum noise.

III.1.2. Dual-loop feedback LNA

The deployment of feed-back in the form of a 1:*n* transformer and a degeneration inductor permits easier simultaneous matching for noise and power while maintaining essentially the same gain (fig. 1b). Reverse signal isolation and stability are improved while still functioning at very low supply voltages [10].

III.1.3. Improved matching using resistive feedback

Resistor R_L of fig. 1a can be replaced by a LC-tank. This, combined with the inductive degeneration at the input, allows conjugate noise and power match (fig. 1c). Some of the output signal is fed back to the input (between the base and the collector) to further improve the input match [29].

III.1.4. Programmable multi-LC LNA

The topologies presented above are narrow-band: the input and output impedances are matched at the frequency where the LC circuits resonate. The bandwidth can be increased by adding a bank of capacitors at the output (fig. 1d). The feedback remains essentially similar, and the noise and linearity of the narrow-band version are maintained. The presence of the output L and the capacitors C_1, C_2, etc. gives rise to a circuit whose impedances are matched at various frequencies, depending on which LC combination is turned on. This leads to a programmable configuration which, however, is

not wide-band since it cannot simultaneously treat different standards [30].

III.1.5. Wideband resistive feed-back LNA

The feedback circuits above are combinations of resistors and capacitors. A purely resistive feed-back can be applied to provide a LNA with wideband matching (fig. 1e). The network of resistors senses the output current I_{OUT} and compares it to the input current I_{IN} (I_{IN}/I_{OUT}) in one branch and to the input voltage V_{IN} (V_{IN}/I_{OUT}) in the other. The input impedance Z_{IN} is simply the ratio between the second-loop and the first-loop gains. A differential version of this LNA is presented in [31]. But the improvement in the matching bandwidth comes at the cost of a greatly increased noise figure and high supply voltages.

III.1.6. Transformer-feedback LNA

Feedback through a transformer, shown in fig. 1f, can be used to ease impedance matching and increase the common-mode rejection [28].

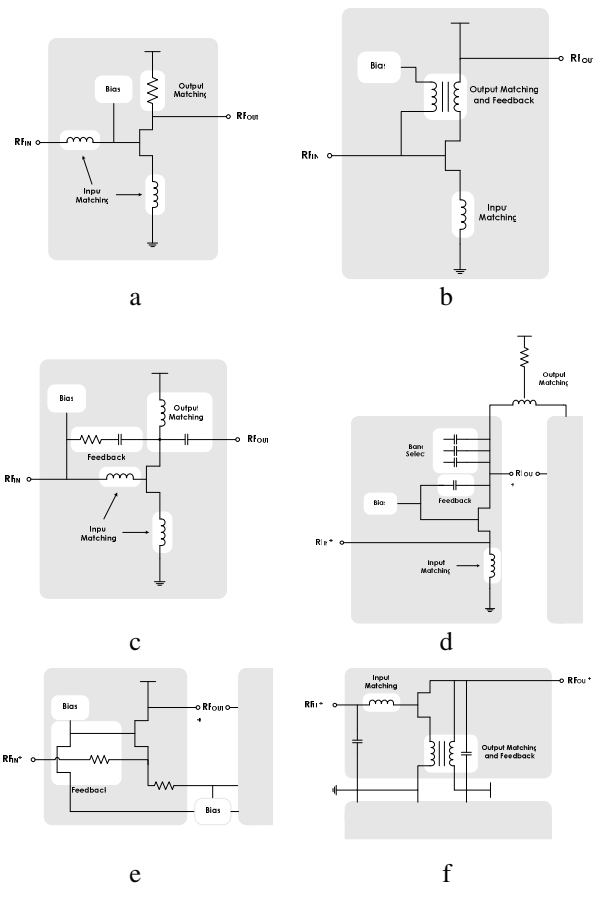


Figure 1 : Single-Transistor LNAs :
a) Common-emitter [21]; (b) Dual-loop-feedback [10]; (c) Tank output matching circuit [29]; (d) Wideband feed-back [30]; (e) Resistive feedback [31]; (f) Transformer-feedback [28]

III.2. CASCODE-BASED LNAS

The single-transistor topologies presented above all benefit from simplicity and a low number of components. The biggest drawback of these topologies is the difficulty of effectively matching the impedances for lowest noise and for best power transfer. Second among the drawbacks is the low isolation to signals traversing the amplifier in the direction opposite to that intended.

The cascode, which uses the common-emitter/source amplifier with another (cascode) transistor, is the most widespread in the realisation of LNAs. The presence of the additional transistor renders the input and output matching networks independent of each other.

III.2.1. Basic cascode

In the basic cascode, input impedance matching is achieved using the degeneration inductor [6],[25],[26], [32],[33].

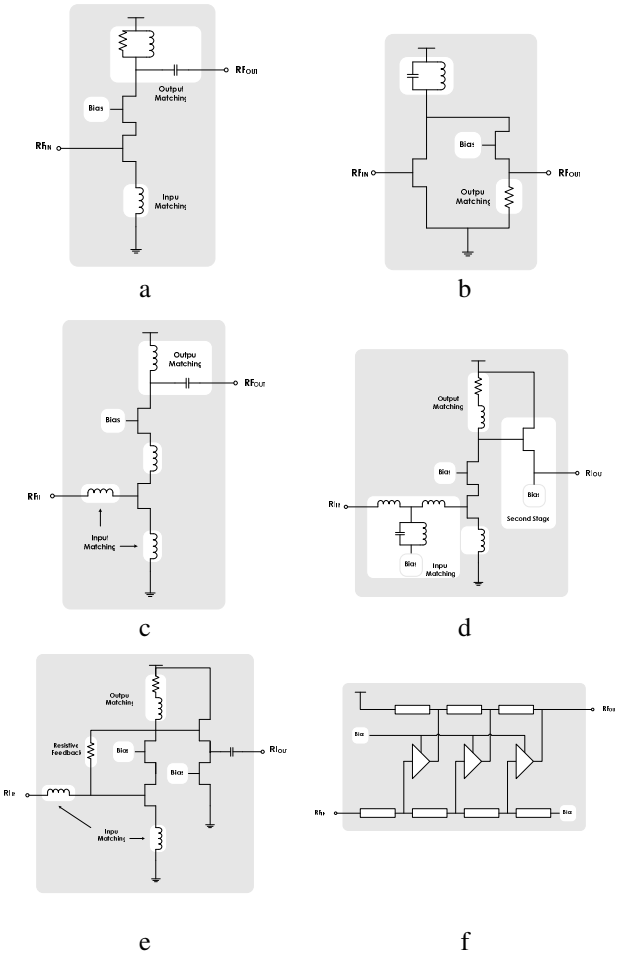


Figure 2 : Cascode-based LNAs
(a) Basic cascode [6]; (b) Folded cascode [21]; (c) Current-reuse cascode [35]; (d) wideband matching [12]; (e) Resistive feedback [14]; (f) Distributed amplifier [36]

The output matching circuit is an LCR-type. The complete combination of this latter is show in fig. 2a, with a parallel combination of inductor and resistor; the capacitor is added in series. One variation of this matching uses a parallel combination of the three elements [34]. Another entirely foregoes the resistor and the capacitor, using only an inductor to match the output impedance [19]. Alternatively, the output capacitor can be replaced by a capacitive divider to increase gain [24],[26]. Active post-distortion can also be used to increase linearity of the LNA [15]. A second common-collector/drain stage is sometimes added to achieve better output match and increase the gain and linearity [13].

III.2.2. Folded cascode

To alleviate the need for a high supply voltage, while preserving the cascode's advantages, a folded-cascode is sometimes used, as shown in fig. 2b. The rail-to-rail voltage needed for the LNA to function is the same as that needed to bias one transistor (and not two, as in the conventional cascode). This allows operation at sub-1V supplies [21]. The LC tank's quality factor determines the characteristics of the LNA. The loss of some amount of current in this tank means that the gain of the folded-cascode is lower than that of the standard cascode. Moreover, the reduction in the supply voltage is somewhat negated by the increase in current dissipation.

III.2.3. Current-reuse cascode

The addition of a load on the first transistor of the classic cascode allows the reuse of the current. This load is realised using an inductor (fig. 2c, [35]), or using a parallel RC combination [4],[16].

III.2.4. Multi-section-input cascode

The matching bandwidth of the classic cascode can be increased by employing a more evolved matching network: combining the cascode configuration with a three-section bandpass-filter based matching (fig. 2d, [12]). This matching network resonates the reactive part of the input impedance over a band covering several gigahertz.

III.2.5. Resistive feed-back cascode

An alternative to the complicated filter matching is to use resistive feedback (fig. 2e, [14]). The result is a wideband input matching with small NF degradation.

III.2.6. Distributed Cascode LNAs

Distributed amplifiers, while not a part of the cascode LNA class, are constructed using a series combination of classical cascode amplifiers (fig. 2f). The stages share a common biasing circuit, and the gain of the LNA can be controlled by digitally switching on the desired number of stages. The transmission lines which connect the stages provide wideband matching. The matching is obtained by adding real transmission lines [36]. Alternatively, the input and output capacitances of the transistors are combined with on-chip inductors to form pseudo transmission lines with properties similar to real lines [8]. Theoretically, the gain of such a LNA can be increased indefinitely by adding more stages while maintaining the bandwidth. However, in practice, area constraints and passive losses in the transmission lines limit the number of stages. The advantages offered by distributed LNAs include good gain control, intrinsically broadband frequency response and good impedance matching. However, the presence of several unitary cascode LNAs means that the noise figure, area and power consumed are increased proportionally to the gain of the LNA.

III.3. TWO-STAGE LNAS

III.3.1. Cascade LNA

The simplest two-stage realisation consists in a common-emitter input cascaded with a similar stage (fig. 3a, [37]).

III.3.2. Feedforward LNA

A feed-forward noise-cancelling technique can be used to increase the bandwidth (fig. 3b). This technique also allows for simultaneous noise and impedance matching, while cancelling the noise and distortion contributions of the matching device [17].

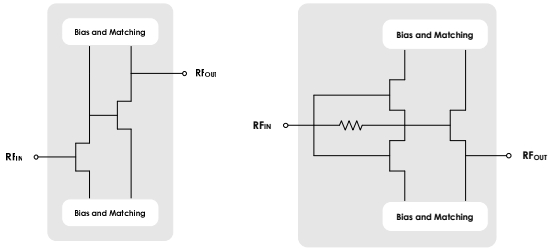


Figure 3 : Two-stage LNAs
(a) Simple [37]; (b) Feed-forward [17]

III.4. SPECIAL TOPICS IN LNA DESIGN

III.4.1. Wideband and Multi-band LNAs

To be considered broadband, a LNA must simultaneously satisfy two criteria: good impedance match and flat gain across a wide bandwidth [8].
From the presentation of various LNA structures above, it can be observed that wideband LNAs are dominated by two topologies: resistive feedback and distributed amplifiers. The feedback LNAs' matching is limited to higher frequencies because of parasitic capacitances [12]. The use of the transmission lines in distributed LNAs allows good matching to be obtained for frequencies all

the way down to DC. Resistive-feedback based amplifiers provide wideband matching and flat gain, but suffer from poor NF and large power. In the resistive shunt-feedback amplifier, input resistance is determined by the feedback resistance divided by the loop-gain of the feedback amplifier. Therefore, feedback resistors tend to be of the order of 100Ω in order to match the low signal source resistance (typically 50Ω), leading to significant NF degradation. Even with moderate gain, it requires large currents due to its strong dependence for voltage gain on the transconductance of the amplifying transistor. Distributed LNAs, too, consume high currents due to multiple amplifying stages, making them unsuitable for low-power applications [14]. The three-section matching LC network of the LNA in [12] provides input matching over a bandwidth extending from 3.1GHz to 10.6GHz because each section of the network is tuned to present a reflection zero at different points along this frequency range. The combination of the three sections leads to a wideband input matching. In all the wideband LNAs encountered, a fundamental trade-off that has to be considered is between bandwidth and noise [17].

Impedance matching networks consist of inductors and capacitors, which can be tuned only at a particular frequency, and the LNA is inherently narrow-band. A "multi-band" LNA designed using these blocks thus has to consist of several narrow-band LNAs in parallel, each treating a separate narrow frequency band. Moreover, there is no possibility of sharing the matching components between different bands. Theoretically, therefore, a *n*-band LNA will occupy *n* times as much chip area as a single-band LNA [16],[33]. LNAs contain on average three to four inductors, and such an architecture used for multi-band operation would take up a lot of space because, firstly, inductor sizes are large compared to transistors, and secondly, additional area has to be left on the chip to include adequate spacing between these inductors [31].

III.4.2. Performance control in LNAs

The suitability of a wide-bandwidth LNA to different standards is not merely dependent on its bandwidth. It should be able to provide variable signal gain depending on the necessity. In instances where linearity requirements are strict, a moderate gain is needed because linearity is generally found to be inversely proportional to the gain. When the transceiver's noise figure is more important than its linearity, the LNA needs to provide high gain in order to attenuate the noise contributions of the succeeding stages. Moreover, the input signals are variable. The LNA's gain should be reconfigurable so that it can highly amplify weak signals and only moderately amplify stronger ones. Moreover, the LNA should be able to reduce its gain in the presence of a strong signal to prevent saturation [38].

Control of the LNA's performance, though increasingly important, is generally neglected in existent LNAs. Among the rare instances where the LNA incorporates gain control, the easiest method is to add a variable-gain stage at the output of the LNA. The performance of the core is fixed [22]. The gain of the ensemble is controlled by varying the biasing current of this second stage. Sometimes, the performance of the LNA is controlled using the biasing conditions of the core amplifier [34]. Besides the gain, the noise figure and the input matching depend on the supply. But the improvement in the performance comes at the cost of higher power consumption. Distributed amplifiers, as mentioned above, provide the easiest solution: the higher the number of stages that are turned 'on' by the biasing current, the higher is the LNA's gain [8]. Various combinations of the biasing of the three cascode stages lead to distinct, equally-spaced gain profiles, without detriment to the bandwidth. In most LNAs the gain provided by the amplifier is only controllable in two steps: peak gain, or zero gain. Such LNAs are equipped with a bypass circuit leading to two modes of operation (in [29], for example, the LNA has a gain of 14dB or -4dB).

III.5. COMPARATIVE ANALYSIS

From the presentations above, the following salient properties can be discerned for single-transistor solutions. They present the evident advantages of small chip area, low consumption and low supply voltages. The noise parameters of LNAs remain the same as those of the transistor itself, thus simplifying the noise analyses. Because the input and output impedance matching circuits are dependent on each other, it is difficult to obtain simultaneous match for optimum power transfer and low noise. Since the circuit contains only one transistor in its signal chain, the isolation to reverse signals is very low. This factor becomes all-important when considering the leakage of the mixer signals to the LNA (since the mixer and the LNA are generally placed end-to-end on the same chip). Broadband matching is difficult due to the capacitive nature of the transistor input.

The popularity of the cascode class is explained by the numerous advantages it offers over the single-transistor topology. First, the presence of the second transistor improves the isolation to the reverse signal. Simultaneous matching of the impedances for optimal noise and power transfer is easier in cascode LNAs because the two impedance matching circuits are independent of one another. The deleterious Miller effect, which limits bandwidth and increases noise in one-transistor amplifiers, is attenuated by the presence of the common-base/gate transistor which avoids amplification of the base-collector capacitance of the common-emitter transistor. This keeps the Miller effect from degrading the power gain, as well as from increasing the input referred

noise. On the flip side, the supply voltage has to be high enough to bias both the transistors in the cascode. The minimum supply voltage is thus of the order of 1.4V. The presence of a second noise contributor increases the noise figure and reduces the output voltage swing.

Having defined the performance that an amplifier must give in order to be a good candidate for low-noise amplifiers in modern wireless systems, we now proceed to describe a new class of LNAs.

IV. A NEW CLASS OF LNA SOLUTIONS

Voltage amplification can be realised using two controlled current conveyors as the starting point. The operation and characteristics of the current conveyors have been presented elsewhere and will not be repeated here [39].

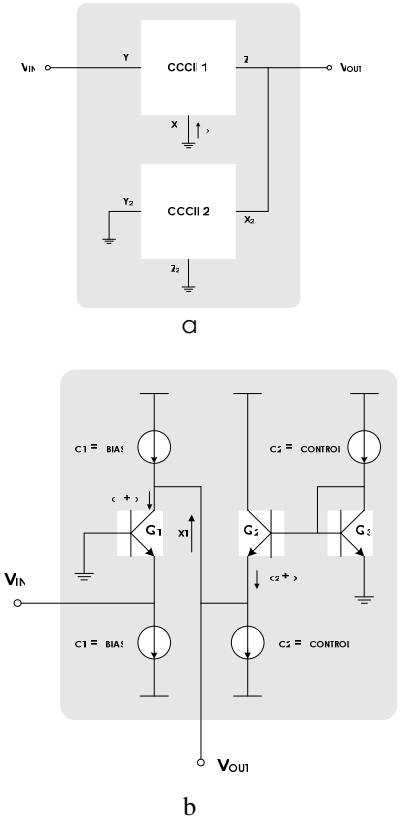


Figure 4 : New CCCII-based Low-Noise amplifiers
(a) Guiding principle; (b) Final transistor-level diagram

IV.1. GUIDING PRINCIPLE

Two conveyors, labelled CCCII 1 and CCCII 2, can provide voltage amplification if connected as shown in fig. 4a. Conveyor CCCII 1 converts the input voltage into a current, the connection of the two conveyors amplifies this current, and conveyor CCCII 2 converts the amplified current into the output voltage.

When voltage V_{IN} is fed at port Y_1, the intrinsic resistance R_{X1} of CCCII 1 converts it into current I_{X1}.

$$I_{X1} = -\frac{V_{IN}}{R_{X1}} \quad (2)$$

Since CCCII 1 is a current follower between its ports X and Z, I_{X1} is copied to Z_1. Because of the connection of the two, this current I_{Z1} enters port X_2 of CCCII 2. Current $I_{X1} = I_{Z1} = I_{X2}$ is converted to a voltage because of resistance R_{X2}. It appears at the output voltage V_{OUT}.

$$V_{OUT} = -R_{X2} * I_{X1} = \frac{R_{X2}}{R_{X1}} * V_{IN} \quad (3)$$

In conveyors, the intrinsic resistance R_X is inversely proportional to the biasing current I_O. This is the basis of controlled conveyors: the properties of the conveyor (especially its R_X) can be controlled using I_O. In classic trans-linear loop conveyors, for example, $R_X = V_T/2*I_O$ where V_T is the thermal voltage (26mV at 27°C) [39]. The gain of the amplifier is thus given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_{X2}}{R_{X1}} = \frac{I_{O1}}{I_{O2}} \quad (4)$$

IV.2. CIRCUIT DESIGN

IV.2.1. Choice of conveyor

Various conveyors were connected to realise the voltage amplifier. The class-A current conveyors presented in [40] were finally decided upon. The absence of PNP transistors (whose transition frequency f_T is typically only a tenth of that of the NPN transistors for a given technology) potentially allows high bandwidths to be attained, compared to NPN-PNP conveyors. Because of the low number of transistors in the signal chain, the noise and distortion introduced to the signal are lower than those for other conveyors. The low number of transistors allows for low supply voltages (as low as ±1.5V) and reduces the consumption of the final LNA. The gain profiles obtained using these CCCIIs are stable and flat upto the gigahertz range, and present no rebounds. Although the linearity of the conveyors is limited by the class of operation, the linearity of the final LNA realised using these was found to be sufficient with respect to the levels of input signals to be treated by the LNA. Therefore, the use of the simple all-NPN class-A conveyors allows for the optimisation of the four major parameters that define the LNA: gain and bandwidth, linearity, noise and power consumption.

IV.2.2. Simplification of architecture

One of the fundamental demands on the LNA is to have 50Ω impedance matching at the input. According to the schema presented, the input signal is fed at port Y whose intrinsic impedance is of the order of some tens or hundreds of kilo-ohms (kΩ). Port X, on the other hand, has impedances R_X lower than some hundreds of ohms;

R_X can be reduced to 50Ω for higher values of I_{O1}. Therefore, the input signal is shifted from port Y_1 to X_1. The subsequent changes and optimisation of the architecture lead to the basic transistor-level schematic of the LNA shown in fig. 4b. Biasing currents I_{O1} and I_{O2} are re-named I_{BIAS} and $I_{CONTROL}$ respectively.

On the transistor level, the operation of the LNA can be explained as follows. The input voltage $V_{IN}(t)$ is applied at the emitter of Q_1, around a DC offset equal to the base-emitter voltage of Q_1, $V_{BE,Q1}$. $V_{IN}(t)$ induces an alternating current $i_{X1}(t)$ at port X of Q_1, hereafter referred to as I_{X1}. The collector current of Q_1, $I_{C,Q1}$ is thus the sum of the DC current I_{O1} and $i_{X1}(t)$. Because of the connection between the collector of Q_1 and the emitter of Q_2, the emitter current of Q_2, $I_{E,Q2}$, is the sum of I_{O2} and $i_{X1}(t)$. Since the collector and emitter currents of a transistor can be considered equal, the collector currents of the two transistors are given by :

$$I_{C,\,Q1} = I_{O1} + I_{X1} = I_{O1}\left[1 + \frac{I_{X1}}{I_{O1}}\right] \quad (5)$$

$$I_{C,\,Q2} = I_{O2} + I_{X1} = I_{O2}\left[1 + \frac{I_{X1}}{I_{O2}}\right] \quad (6)$$

Since the base of Q_1 is on ground level, $V_{IN} = -V_{BE1}$.

Now, V_{BE1} can be expressed in terms of the collector current I_{C1} of Q_1 as

$$V_{BE1} = V_{T*}\log\left[\frac{I_{C1}}{I_{SAT}}\right] = V_{T*}\log\left[\frac{I_{O1}}{I_{SAT}}\left(1 + \frac{I_{X1}}{I_{O1}}\right)\right] \quad (7)$$

where I_{SAT} is a constant. Given that log(AB) = logA + logB and that log (i+a) ~ a when a<<1, this equation changes to

$$V_{IN} \approx -V_{T*}\log\left[\frac{I_{O1}}{I_{SAT}}\right] - V_{T*}\frac{I_{X1}}{I_{O1}} \quad (8)$$

The first term in this equation corresponds to the constant DC component of V_{BE} of Q_1, and the second term is the alternating part induced by the input.

Therefore, $V_{IN} \approx -V_{T*}\frac{I_{X1}}{I_{O1}}$

Applying the same principle to the output voltage,

$$V_{OUT} = V_{E2} = V_{BE3} - V_{BE2} \quad (9)$$

Expressing the base-emitter voltages in terms of collector currents, and these in turn in terms of biasing current I_{O2} and I_{X2} gives :

$$V_{OUT} = V_{T*}\log\left[\frac{I_{O2}}{I_{SAT}}\right] - V_{T*}\log\left[\frac{I_{O2}}{I_{SAT}}\left(1 + \frac{I_{X1}}{I_{O2}}\right)\right]$$

(10)

Simplifying this equation leads to

$$V_{OUT} = -V_{T*}\frac{I_{X1}}{I_{O2}} \quad (11)$$

The voltage gain A_V of the LNA is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-V_{T*}\left[\frac{I_{X1}}{I_{O2}}\right]}{-V_{T*}\left[\frac{I_{X1}}{I_{O1}}\right]} = \frac{I_{O1}}{I_{O2}} \quad (12)$$

Comparison of equations 4 and 12 shows that transistor-level operation of the LNA corresponds to the guiding principle.

IV.2.3. Noise optimisation

The noise of the LNA is dominated by the input transistor Q_1; more specifically, the base resistance r_B and the collector current I_C are the dominant contributors in the overall noise figure. The input transistor's emitter length was increased to 10µm to increase its collector current. Three transistors were placed in parallel, and the base of each was sectioned into five parts, to reduce the base resistance and thereby the noise.

IV.2.4. Impedance matching

Equation 12 shows that in its simplest expression, the gain provided by the amplifier is the ratio of the biasing currents of the two conveyors. The input signal V_{IN} is fed at port X_1 of CCCII 1. The impedances of the two ports of the LNA are required to be 50Ω. The input impedance Z_{IN} of the LNA is thus simply the intrinsic impedance Z_{X1} of the first conveyor. Since this latter can be controlled using the conveyor's biasing current I_{O1}, the value of this current is fixed to a value which gives $|Z_{X1}| = |Z_{IN}| = 50\Omega$. The LNA's input impedance is thus easily matched to standard 50Ω. Since the value of I_{O1} is fixed, it will henceforth be called I_{BIAS}. The output impedance Z_{OUT} of the LNA is a combination of the Z port impedance Z_{Z1} of CCCII 1 and the X port impedance Z_{X2} of CCCII 2. Z_{OUT} can be fixed to 50Ω using the two biasing currents. I_{O1} (= I_{BIAS}) is already fixed to give $|Z_{IN}| = 50\Omega$. Fixing I_{O2} also will take away the biggest advantage of this LNA: the easy control of its performance using the biasing currents. Therefore, I_{O2} is kept free of the impedance constraint, and another way of matching the LNA's output impedance has to be investigated. A new method of matching the (arbitrary) output impedance of a RF circuit to a desired value using a current conveyor in the voltage follower mode was used [1]. This makes the output impedance of the LNA independent of its gain.

IV.2.5. Performance control

The gain of the LNA is the ratio of its biasing currents. Current I_{O1} (= I_{BIAS}) is fixed by the need for impedance matching of the LNA input. Output matching is obtained using a novel approach. This renders I_{O2} independent of the impedance-matching. I_{O2} This current will be used to control the performance of the LNA, and will henceforth be called $I_{CONTROL}$. The inverse proportionality between the gain and $I_{CONTROL}$ presents some notable advantages.

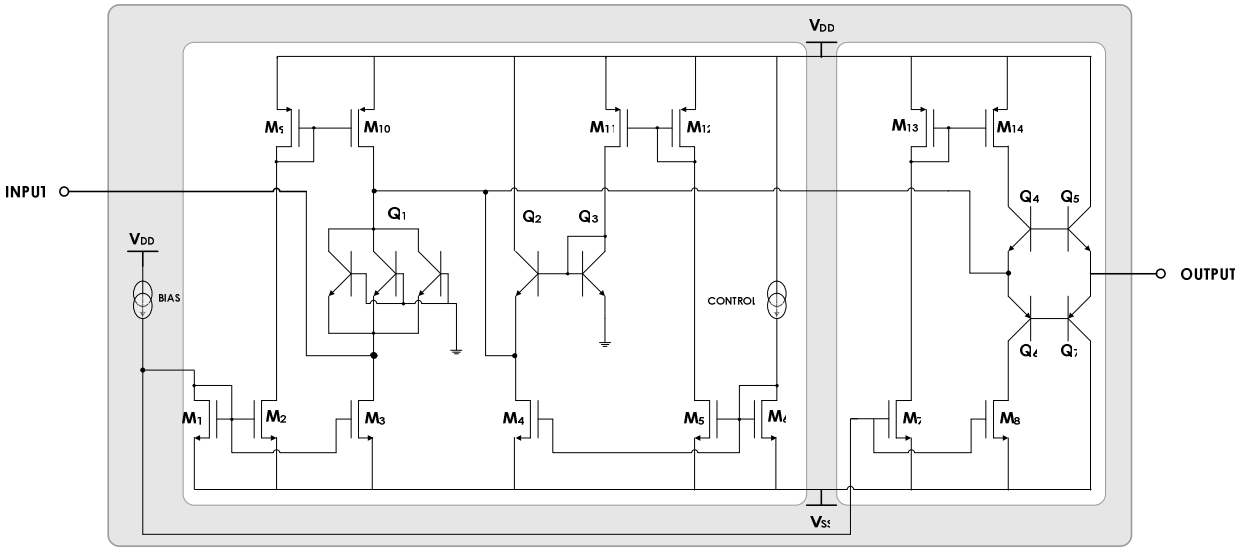


Figure 5 : Complete transistor-level description of a single-ended LNA based on the new principle

Chief among these is the possibility of obtaining high gains for low currents.

IV.2.6. Biasing the LNA using current mirrors

And finally, the current sources were replaced by CMOS mirrors. The sizes and models of the transistors were monitored to make the mirrors efficiently copy a wide range of currents: whereas I_{BIAS} is fixed, $I_{CONTROL}$ will be varied from 25µA to 525µA to obtain gains from 0dB to 25dB; and the mirrors must be able to correctly copy this entire range into the two branches. Moreover, the DC current sources in the impedance matching circuit were also replaced by mirrors. These mirrors were dimensioned in such a way that the current I_{BIAS} that sets the input impedance Z_{IN} can also be supplied to power the output matching circuit.

IV.2.7. Complete transistor-level description

The core of the new LNA contains a very low number of transistors in its signal path (three NPN devices), and will therefore benefit from low consumption and noise. The matching circuit contains 2 NPN and 2 PNP transistors. It introduces negligible distortion to the signal. Moreover, the LNA's noise figure is dominated by the input transistor of the core amplifier; the addition of the matching circuit engenders a very low deterioration in the noise figure. The necessity of copying the biasing current into the different branches adds current mirrors consisting of a total of 14 CMOS devices. The complete single-ended LNA architecture is shown in fig. 5.

IV.2.8. Choice of biasing conditions

The most transistor-laden branch of the LNA consists of 4 transistors between the supply rails. In order for the circuit to function, a ground-referred voltage supply of at least 2.8V is required. It was found that the new LNA provides good operation for supplies as low as ±1.5V. Increasing the supply voltage to ±2.5V was found to greatly improve the performance, especially its bandwidths; the power consumption at this supply is still low enough to justify it.

IV.3. FABRICATION TECHNOLOGY

IV.3.1. SiGe Processes

In 2002, silicon-based devices accounted for more than 98% of sales in the global semiconductor market, owing mainly to their low costs [41]. The trend continues to this day, although silicon has gradually been supplanted by a new composite : silicon-germanium (SiGe). Thanks to the boost in the performance by this doping, SiGe has become the material of choice for wireless ICs and low-power radio-frequency components [41]-[44]. SiGe offers a bridge between low-cost, low-power, low-frequency silicon chips and high-cost, high-power, high-frequency chips made from materials such as Gallium-Arsenide (GaAs) and Indium-Phosphate (InP). They entirely maintain the key advantages of silicon processing [41]. In SiGe processes, peak transition frequencies are obtained for lower collector current and noise figures are reduced upto frequencies of 10GHz [43]-[45]. Besides the improvement in the bipolar transistor's performance, SiGe processes offer very easy integration of CMOS devices to create BiCMOS technologies with improvements in the properties of both the bipolar and the MOS devices. The advantages of BiCMOS technologies is their lower cost

(consequent to a reduction in the number of manufacturing steps) and the possibility of mixed-signal integration using one single technology [44],[45].

IV.3.2. 0.35µm SiGe BiCMOS

Based on the excellent performance-cost combination of the 0.35µm SiGe BiCMOS process from STMicroelectronics, it was decided to fabricate the circuits in this technology. This process is optimised for low-power radio-frequency system-on-chip applications, but also enables high density/high performance digital and analog applications in the same chip. 'bicmos6g' proposes a parameterised vertical NPN transistor optimised for 3.6V operation [46]. The process also proposes scaleable vertical PNP transistors. The transition frequencies of the NPN transistors have peak values of around 45GHz at 3.3V and that of the PNP devices has values upto 4 – 5 GHz. The noise figure of the NPN transistor, at 2GHz, is around 0.8dB [47]. Besides the core bipolar transistors, the technology contains complementary MOS transistors designed specifically for RF applications (models : nrfmos and prfmos). Both the channel width and the length can be scaled according to choice, subject to the minimum length limit of 0.35µm. The technology contains 1 poly layer and five metal layers. Metal M1 is in tungsten and metals M2 to M5 are in aluminium.

IV.4. MEASUREMENT TECHNIQUES

The aim behind the fabrication of circuits and the measurement of their performance is to validate the efficient operation of the circuit in a real environment. Comparisons between the simulated and experimental performances determine the effect of non-idealities (parasitics, temperature variations, substrate leakage, device failure, effects of interferers and noise sources in the environs, etc.).

The imperfections in the measurement apparatus render it difficult to estimate what part of the performance deterioration comes from the circuit itself and what part from the apparatus. Generally, integrated circuits are encapsulated in packages and then soldered on a printed circuit board. The measurements thus carried out are highly dependent on the properties of the cables that link the IC to the apparatus and on the type of packaging itself. Moreover, these are measurements 'at a distance'.

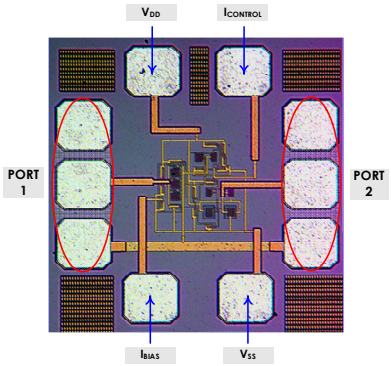
The principle which guides measurements using micro-probes is the evaluation of the circuit's performance directly on the silicon wafer, giving a better idea of the 'intrinsic' performance. The Karl Süss PA200 measurement bench is one such ensemble [48]. It allows direct on-wafer measurements of circuits. The temperature of the thermo-chuck can be regulated from -65°C to +220°C, thus allowing the measurement of the temperature stability of circuits. An air-evacuation mechanism prevents the formation of ice crystals on the wafer for analyses at temperature below 0°C. A Faraday cage offers high immunity to electrical noise as well as light. On-wafer measurements allow the characterisation of a circuit's performance as close to a real environment as possible, by minimising cable parasitics and eliminating packaging faults.

Micro-probes are placed on the circuit's pads. The DC micro-probes, used for biasing the circuits and carrying out static measurements, terminate in fine needles of diameter smaller than 1µm. For the frequency-domain analyses of the circuits, single-ended AC probes of the Ground-Signal-Ground (GSG) type are used at either port of the circuit. Since the signals supplied and tapped are of necessity defined with the ground plane as reference, the set-up allows only single-ended characterisation of circuits. The GSG configuration minimises contact losses and parasitics at high frequencies. The AC probes that were used have a fixed distance of 100µm between any two adjacent points (ground-signal, or signal-ground). The RF pads of the circuits have thus to be placed such that the distance between their centres corresponds to this 100µm.

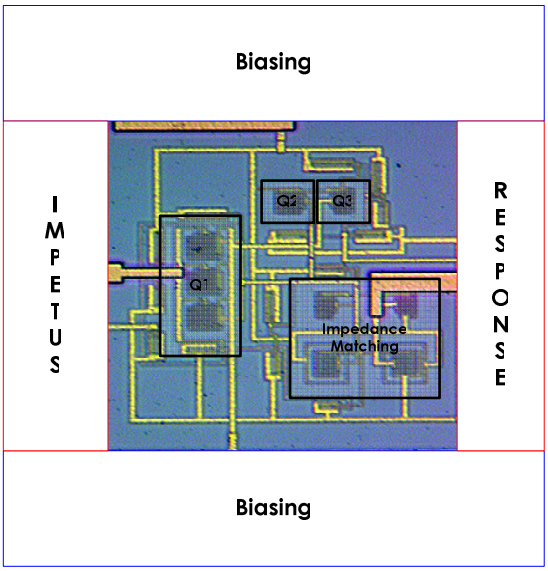
The placement of the probes on the circuit's pads is a delicate exercise. Once the probes are placed on the pads, small pressures are applied to create the contact between probe and measurement pad. Measurement pads on the circuit are generally made of aluminium, and have a thin (of the order of a 100 Angströms) oxide film on them. The probe must crack this film to access the real aluminium within. It is the breaking of this thin oxide film which creates small depressions in the pads. But the pressure on the probes must not be so high that it pierces the fine pad.

In some of the preliminary analyses, it was observed that the results were erroneous. This was explained by the insufficient pressure on the probes, which led to unstable contacts and incomplete breaking of the oxide layer. Moreover, small fragments of the broken oxide film remained stuck to the probes, and destabilised later analyses; the probes were thus periodically cleansed of these remnants.

Similar precautions are to be observed for the AC probes.



a



b

Figure 6 : The Single-Ended LNA
(a) Photograph of the new impedance matched single-ended LNA, with measurement pads; (b) Close-up of the single-ended LNA, showing the three transistors in the signal chain and the output impedance matching circuit

V. NEW SINGLE-ENDED LNA

V.1. DESCRIPTION OF THE CIRCUIT

Fig. 6a presents a photograph of the 50Ω single-ended LNA. The RF pads (GSG, to correspond with the micro-probes) are placed opposite one another, and the DC biasing pads are distributed on the other two sides of the circuit. The total area occupied by the LNA is 0.022mm² without the pads (with pads, it is 0.206mm²).

The LNA is biased under a dual voltage supply (nominally, ±1.5V) at pads marked V_{DD} and V_{SS}. The bias current I_{BIAS} is used to bias the core LNA as well as the matching circuit, and its value sets the values of both Z_{IN} and Z_{OUT} of the LNA. Current $I_{CONTROL}$ is the means of controlling the gain of the LNA.

Since the number of DC probes is limited to four, the biasing currents and voltages are placed on each of the pads. The Ground path is provided by the AC probes: the lower ground pads of the GSG pad combinations are linked to each other and determine the ground of the circuit. This connection ensures that the ground of the circuit is established even if one of the AC probes' grounds provides a bad contact.

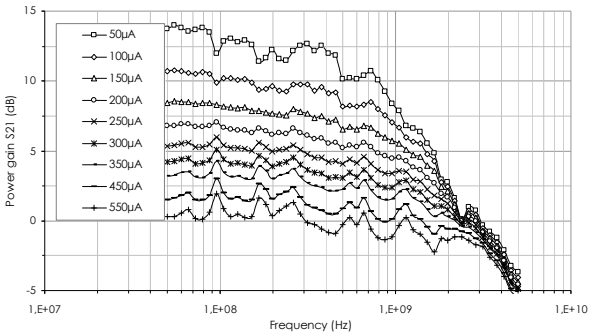
Fig. 6b shows a close-up of the LNA. Transistor Q_1, at whose emitter the input is applied, is the major contributor of the noise. Therefore, to reduce its base resistance and collector current, three devices are placed in parallel. The rest of the signal processing is done by transistors Q_2 and Q_3. The output is matched to 50Ω using the new impedance matching circuit, which is also shown on the photograph. The major RF signal wires are realised on the least resistive metal layer, M5.

V.2. MEASURED PERFORMANCE OF THE NEW SINGLE-ENDED LNA

V.2.1. Power consumption

The transistor dimensions of the LNA are optimised for operation at V_{DC} = ±1.5V. Preliminary analyses showed that the I_{BIAS} required for best impedance at both the input and the output is around 450µA.

Gains between 0dB and 14dB are obtained for $I_{CONTROL}$ varying between 50µA and 550µA. This variation in $I_{CONTROL}$ has the effect of changing not only the gain of the LNA, but also other parameters. This latter, an undesired secondary affect, will be shown to be minor, in comparison with the range of gain control. The LNA consumes between 3 and 4.5mA for the entire range of $I_{CONTROL}$. These values are essentially similar to those obtained from simulations. As expected, the consumption changes linearly with $I_{CONTROL}$.



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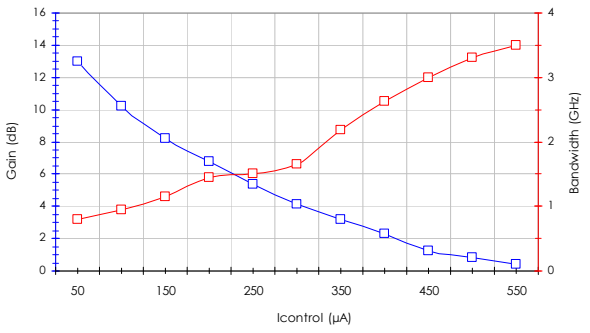


b

Figure 7 : Gain and bandwidth of the single-ended LNA for different $I_{CONTROL}$; at V_{DC} = ±1.5V and I_{BIAS} = 450µA
a) Gain profiles; b) gain control

V.2.2. Gain control

Fig. 7a shows some representative gain profiles of the LNA. Barring the renegade points (especially at low frequencies for lower gains), the gain profiles are flat and stable over large bands. It can be observed that for high values of gain, the bandwidth is the lowest.

Fig. 7b depicts the gain and the bandwidth of the single-ended LNA. For gains higher than about 10dB, the bandwidth is lower than 0.9GHz, but it improves at moderate and low gains. The gain control of the LNA is smooth, and intermediate gains can be obtained by fine-tuning $I_{CONTROL}$. Peak bandwidths of 3.5GHz were attained.

V.2.3. S-parameter response

The scattering parameter matrix of the single-ended LNA is given by the matrix:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

Here, transmission parameter S_{21} is the gain of the LNA, presented above.

The other three S parameters are shown in fig. 8 below. S_{11} and S_{22} stand, respectively, for the reflection coefficient the input and the output, and are indications of the quality of impedance matching at each port. S_{12} is the strength of the reverse signal.

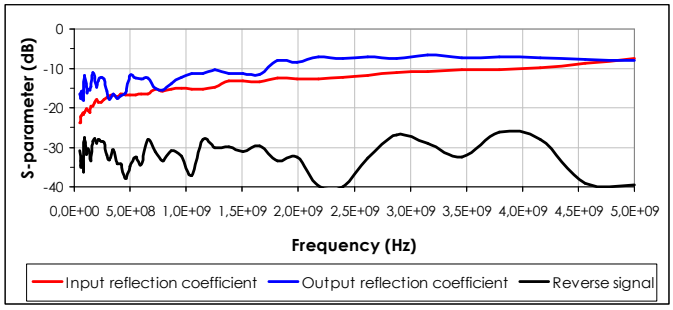


Figure 8 : S-parameters of the single-ended LNA, for gain = 6dB; at V_{DC} = ±1.5V and I_{BIAS} = 450µA

The input impedance is excellently matched over a multi-GHz band: S_{11} is lower than -10dB for all frequencies upto 4GHz, and for all values of $I_{CONTROL}$. Below 1GHz, S_{11} < -15dB and upto 2GHz, S_{11} < -13dB.

The impedance matching at the output is excellent upto 1.8GHz (S_{22} < -10dB). S_{22} is more dependent on $I_{CONTROL}$ than is S_{11}. This is in keeping with the simulations, where it was observed that for the entire range of $I_{CONTROL}$, the input impedance was essentially the same, whereas the output impedance of the LNA showed variations of 10% around 50Ω.

The strength of the reverse signal is extremely low : for all frequencies upto 5GHz, S_{12} is lower than -26dB for all values of the LNA gain.

V.2.4. Noise performance

In this new LNA, the gain is dependent on $I_{CONTROL}$. This same current also changes the operating point of the transistors, notably their base resistances and collector currents, the two parameters which have the highest effect on the noise figure of the LNA. Therefore, the noise of the LNA is dependent on $I_{CONTROL}$.

The LNA's simulated noise is lower for higher gains (at 15dB of gain, for example, the LNA's NF is around 1dB, and it goes upto 6dB for 0dB of gain). Therefore, in terms of the trade-off between gain and noise figure, the LNA works best at moderate and high gains. Noise figure profiles for different gains are depicted in figure 9.

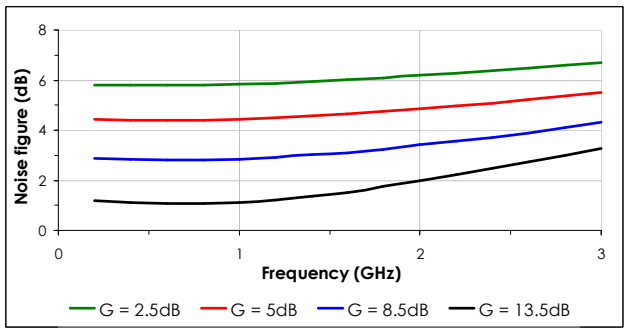


Figure 9 : Noise figure profiles for the single-ended LNA

V.2.5. Transient performance

A sinusoidal signal of 80mV peak-to-peak amplitude and 200MHz frequency was applied at the LNA's input, and the response was observed on an oscilloscope. The variation of the output (and, consequently, the gain) was found to be inversely proportional to the gain control current, in keeping with the AC gain control.

V.2.6. 1dB Compression point

For a fixed $I_{CONTROL}$ of 200µA (corresponding to a gain of 6dB), the input signal power was varied in fixed steps, thus enabling the determination of the 1dB compression point and consequently, the linearity of the new single-ended LNA. The frequency of the input signal was 1GHz. The input-referred P_{1dB} was found to be -12.5dBm.

V.2.7. Intermodulation products

Another important indicator of the linearity of the LNA is its third-order intermodulation product. The analysis consists in applying two separate equal-intensity tones, at the desired frequency f_1 and at a neighbouring frequency f_2. The frequencies and the distance between them, $f_1 - f_2$, are dependent on the standard for which the LNA is

destined. Unwanted intermodulation products, due to the interaction between the two tones, occur at all frequencies $mf_1 \pm nf_2$. To determine the intermodulation performance of the new LNA, two tones of -30dBm intensity were applied at 1GHz and 1.02GHz.
At the output of the LNA, the two fundamental tones were present and the levels of the higher-order terms (with respect to the fundamental) were: 3rd-order terms 30.28dBm, 5th-order terms 48dBm, and 7th-order terms 72dBm lower than the fundamental. The input-referred third-order intermodulation point was determined to be -12.04dBm.

V.2.8. Temperature stability

The temperature of the thermo-chuck on which the wafer is mounted was changed from -25°C to +75°C, and the LNA's performance was measured to determine its temperature stability.
Fig. 10 depicts the temperature stability of the four critical LNA parameters: gain, impedance matching and reverse signal isolation. A representative case is taken: LNA gain of 10dB. The values of the S-parameters are those at a frequency of 1GHz, the centre of the destined applications of the LNA. The impedance matching at both the input and the output remains good (S_{11} and S_{22} are both lower than -10dB). The reverse signal isolation remains better than -30dB over the same range of temperatures. The gain of the LNA shows variations of ±0.6dB around the ambient temperature value of 12dB.

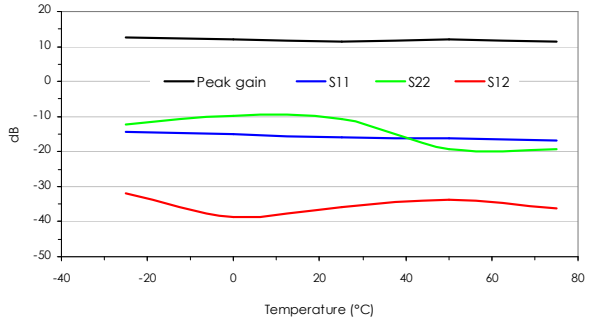


Figure 10 : S-parameters of the single-ended LNA, versus temperature, for gain = 10dB; at V_{DC} = ±1.5V and I_{BIAS} = 450µA

V.3. RESUME AND COMPARISONS WITH SIMULATIONS

The new single-ended 50Ω gain-controllable low-noise amplifier was fabricated in a 45GHz 0.35µm SiGe BiCMOS process. It takes up 140µm x 160µm of area. The sub-sections above have presented the results obtained from different analyses carried out on this structure.
Table I presents an overview of the results described above. For comparison, it also presents the results obtained from simulations. Gains ranging from 0 to 13dB can be obtained by varying the biasing current $I_{CONTROL}$. Working under a ±1.5V supply, the LNA consumes less than 4.5mA of current (the same as the simulated values). For gains greater than 5dB, the LNA consumes lower than 3.6mA. For the entire range of gains, the 3dB bandwidth is greater than 800MHz; the lower cut-off frequency is always 0Hz (because of the limitations of the network analyser, the response of the LNA could not be measured below 50MHz). For gains between 0 and 10dB, the 3dB bandwidth of the LNA extends from DC to greater than 1GHz. Peak bandwidths of 3.5GHz were attained.

Table I : Synopsis of the single-ended LNA's measured and simulated performances, at V_{DC} = ±1.5V

Impedance-matched Wideband Single-ended LNA			
Parameter	Conditions	**Simulations**	**Measurement**
Gain control		0 – 18dB	0 – 13 dB
Bandwidth :			
f_L		0Hz	0Hz
f_H		> 1.0GHz	>0.8GHz (3.5GHz)
Consumption		2.8– 4.5 mA	3 – 4.5 mA
S_{11}	0 – 2GHz	< -14dB	< -12.5dB
S_{22}	0 – 2GHz	< -11dB	< -8dB
S_{12}	0 – 2GHz	< -64dB	< -27dB
Noise figure		1dB – 6dB NF α 1/Gain	not measured
IP_{1dB}	1GHz	-12dBm	-12.5dBm

The impedance matching at the input and the output of the LNA is good for frequencies ranging from 0 to 2GHz, and only slightly worse than the simulated performance. The rejection of the reverse signal is better than -26dB for all frequencies upto 5GHz. This performance is stable for all the values of gain. The LNA is highly linear, with an input-referred P_{1dB} of -12.5dBm.
The LNA works well for temperatures between -25°C and +75°C, a 100°C range around the ambient temperature.

V.4. COMPARISONS WITH EXISTENT LNAS

The relevance of the new LNA for present-day wireless transceivers can be determined on comparison with solutions that exist in published literature. Table II presents some recent single-ended LNAs, along with the new conveyor-based solution. This table contains LNAs that we deemed most representative in terms of applications (standards from CDMA to UWB are covered) and in terms of performances. The performance of the new LNA given is that obtained at gains of 3dB and 13dB, the two extremes of the gain control range.
Existent low-noise amplifiers inevitably make use of passive elements, thus increasing their area, and often ruling out single-chip solutions (the passives often have to be placed off-chip).

Table II : Comparison between the new single-ended LNA and some other recent solutions

Reference **Year**	**[15]** **2006**	**[24]** **2002**	**[21]** **2001**	**[17]** **2004**	**[14]** **2005**	**This work**	
Frequency **Applications**	0.88GHz CDMA	1.23GHz GPS	1.9GHz PCS1900	0 – 2GHz Wideband	3 – 5GHz UWB	**0 – 2GHz** **Wideband**	
Technology **Passives** **Area**	.25µmCMOS 8 - n.a. -	.25µmCMOS 8 0.66mm²	.5µmCMOS 3 1.3mm²	.25µmCMOS 8 0.08mm²	0.18µmCMOS 9 0.9mm²	**0.35µmBiCMOS** **0** **0.022mm²**	
Peak gain **Bandwidth : f_L** **f_H**	16.2dB - n.a. -	20dB 1.0GHz 1.4GHz	15dB 1.7GHz 2.1GHz	13.7dB 0Hz 1.6GHz	9.8dB 2.0GHz 4.6GHz	**0dB** **0Hz** **3.5GHz**	**10dB** **0Hz** **0.95GHz**
Consumption **Dissipation**	12mA 31.2mW	6mA 9mW	25mA 25mW	14mA 35mW	- n.a. - 12.6mW	**4.2mA** **12.6mW**	**3.2mA** **9.6mW**
S_{11} **S_{22}**	-10dB -10dB	-11dB -11dB	-22dB -10dB	< -10dB < -8dB	< -9dB < -10dB	**< -13dB** **< -10dB**	
S_{12}	- n.a. -	< -31dB	- n.a. -	< -36dB	< -20dB	**< -28dB**	
IP_{1dB}	- n.a. -	-24dBm	-11dBm	- n.a. -	- n.a. -	**-12.5dBm**	
Noise figure	1.2dB	0.8dB	1.8dB	2.4dB	2.3dB	**6.8dB***	**1dB***

The new single-ended LNA is an all-active circuit, and its size is 40-50 times smaller than most other LNAs - and at least four times smaller than the smallest LNA observed in existent literature [17].

The current consumption of existent LNAs varies widely, depending on the gain of the LNA, but is almost always greater than 5mA (barring the 2.5mA consumption of the LNA in [10]). In contrast, the new LNA consumes less than 4.5mA for the entire range of gains it provides. This figure is better than the best consumption noted in existent LNAs.

The impedance matching circuitry is the most area-consuming part of most LNAs. Successful matching is achieved in very narrow bands (over which the passive network resonates). The new LNA attains good matching for all frequencies between 0 and 4GHz. Moreover, matching is independent of the gain of the LNA, contrarily to, for example, the LNA in [34].

Each communication standard has its specific exigencies with respect to the linearity. The IP_{1dB} of the new LNA is much higher than the GPS LNA in [24], comparable to the PCS1900 LNA in [21] and the WCDMA LNA in [11]), and only slightly worse than the highest observed IP_{1dB} [10].

Gain control is a rare feature in existent low-noise amplifiers. When it is included, the gain control range is rather limited and power consumption increases with the gain (for example, the LNA in [34] provides gains ranging from 10 to 14dB, with power dissipations of 5mW and 15mW respectively). By contrast, the gain of the new single-ended LNA can be varied between 0 and 13dB. The inverse relation between the gain and the control current means that best gains are obtained at lowest power dissipation.

VI. NEW DIFFERENTIAL LNA

VI.1. DESCRIPTION OF THE CIRCUIT

The general technique of obtaining a fully differential circuit by mirror-duplicating its single-ended version was used [25],[31]. The transistor-level description of the LNA is similar to the one presented in section IV.3. The block-level description of the differential LNA is given by fig. 11. Two similar LNA architectures are included on the same schematic. The two 'channels' are totally independent of each other, except the biasing circuit. Each branch is a single-ended LNA with an integrated input matching and the new matching circuit added to match the output impedance. Biasing current I_{BIAS} alone decides both the input and the output impedances of all the ports. Current $I_{CONTROL}$ controls the gain of both the channels.

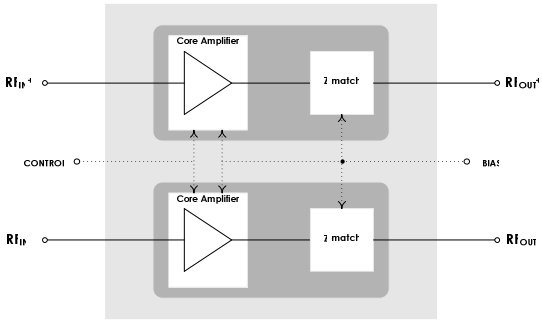


Figure 11 : Block-level description of the new differential LNA

Like the single-ended LNA, the lowest supply voltage at which the new differential LNA functions competitively is ±1.5V. The performance of the LNA (especially its bandwidth and noise figure) improves as the supply

voltage is increased. But these improvements come at the cost of increased power dissipation. It was adjudged that the most optimal performance is obtained at $V_{DC} = \pm 2.5V$: the performance is excellent, and the consumption still remains within acceptable limits.

VI.1.1. Impedance matching

As was observed in the design of the single-ended LNA, current I_{BIAS} is fed to both the (inherent) input matching network, and the output matching circuit added to the core LNA. In the LNA branch which determines the input impedance (the branch of the transistor Q_1 in fig. 5), a bias current of around 530µA is needed for the input impedance to be close to 50Ω. On the other hand, the current required in output matching network is around 325µA at ±1.5V and 440µA at ±2.5V. These values give rise to impedances R_X which are around 50Ω. In *each branch* of the LNA, the mirrors were dimensioned such that they provided, for example, 530µA in the input impedance branch and 440µA in the output matching network, at $V_{DC} = \pm 2.5V$. Thus, a current I_{BIAS} of around 1mA to 1.1mA needs to be fed into the *entire* differential LNA, for it to be split into two, one going into *each 'channel'* of the LNA. In reality, it was found that 1.14mA was needed at $V_{DC} = \pm 1.5V$, and 1.08mA at $V_{DC} = \pm 2.5V$. This decision of splitting I_{BIAS} into two halves was taken supposing that the two channels of the LNA are exactly identical. Care had to be taken to ensure that the corresponding transistors in the two channels were the same. It was observed that I_{BIAS} was exactly split into two halves, thus giving a perfect similarity between the performances of the two single-ended channels. On the level of measurements on the fabricated LNA, it will be observed that despite the uncertainties introduced by the layout process, the measured performance of the two single-ended halves of the LNA was exactly identical.

VI.1.2. Performance control

A single current source provides $I_{CONTROL}$ to change the performance of the two channels. The dimensions of the CMOS mirrors which copy $I_{CONTROL}$ into the required branches of the LNA (the Q_2 and Q_3 branches in figure 5) were monitored and fixed such that $I_{CONTROL}$ from the source was *duplicated* in the two channels of the LNA, and not *divided* into two, as was the case with I_{BIAS}. Duplicating $I_{CONTROL}$ allows wide gain variations using currents between 25µA and 550µA (as opposed to the need to vary $I_{CONTROL}$ between 50µA and 1.1mA, were $I_{CONTROL}$ to be divided into two halves).

VI.1.3. Optimisation of the differential structure

Ideally, since the differential LNA is simply designed by duplicating the single-ended version, it would have the following characteristics, consequent to the doubling of the number of transistors: the consumption of the differential LNA would be two times that of the single-ended counterpart; the noise figure of the differential LNA would be exactly 3dB higher than that of the single-ended version (because the number of noise contributors is doubled). But this consumption and noise are both unacceptable. Therefore, additional optimisation was carried out on the sizes and models of the signal-processing transistors, to achieve the following: consumption lower than 7 – 8mA, and noise figures comparable to the single-ended LNA. The bandwidth of the LNA was greatly increased following these optimisations. However, this improvement came at the cost of decreased linearity, higher transient offsets, and lower temperature stability.

VI.1.4. Description of the fabricated circuit

The differential LNA was also fabricated as a stand-alone circuit in the 0.35µm SiGe BiCMOS process. The LNA is a 4-port device with two input ports (denoted P_1 and P_2) and two output ports (P_3 and P_4). The two amplification channels are thus P_1P_3 and P_2P_4. A complete characterisation of such a circuit would take into account its response to differential and common-mode stimuli besides the single-ended analyses of each pair of ports. However, since the measurement apparatus were all two-port, only single-ended analyses could be carried out. These provide an excellent approximation of the performance of each of the amplifying channels of the differential device. A close correspondence between the simulated and measured single-ended analyses would enable us to draw conclusions on the subsequent differential-mode performance of the LNA.

Single-ended analyses on multi-port devices are carried out by testing each combination of two ports while terminating all the unused ports with 50Ω resistors. Since the chip was fabricated and un-packaged, these resistors could not be placed externally but had to be included on the chip itself. This gave rise to several circuits, one for each combination of two ports of the differential LNA.

The two forward transmission amplification channels are the P_1P_3 and P_2P_4 combinations. The P_1P_2 combination determines the isolation between the two inputs, the P_3P_4 combination determines the isolation between the two outputs, and the P_1P_4 combination determines the inter-channel performance.

To minimise the errors resulting from possible differences between the layouts of the circuits, a single circuit was first laid out and then duplicated to give the other four combinations.

Fig. 12 shows a close-up of the LNA, without the pads. The layout of one of the channels (the transmission channel from IN+ to OUT+, in our case) was first created and then duplicated to give rise to the differential structure, around a plane of symmetry.

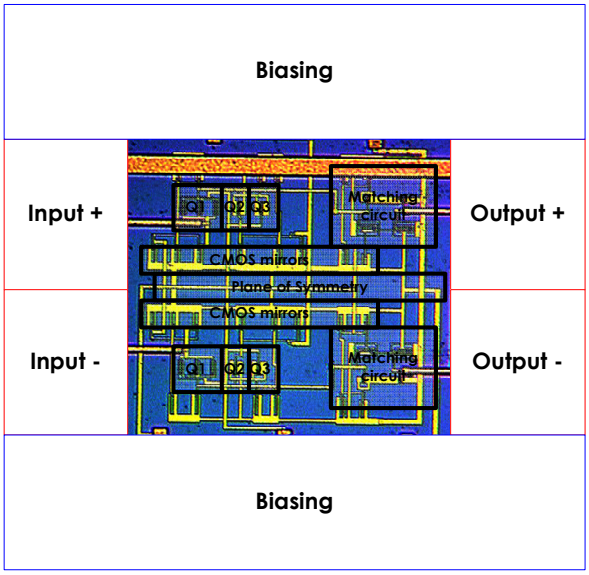


Figure 12: Close-up of the differential LNA showing the signal-chain transistors Q_1 to Q_3, the output matching circuit and the CMOS mirrors; the two halves are laid out around a symmetry plane

Special care was taken to make sure that the dimensions of the wires were exactly similar in the two halves of the LNA. The active area of each half of the LNA is divided into two major parts: the core LNA consisting of the transistors Q_1 – Q_3, and the matching circuit.

The total size of the differential LNA, without the measurement pads, is 0.083mm² (with pads, it is 0.253mm²).

VI.2. MEASURED PERFORMANCE OF THE DIFFERENTIAL LNA

VI.2.1. Power consumption

The transistor dimensions of the LNA circuit were optimised for operation at ±2.5V. The results presented in the remainder of this section are those obtained at this operating voltage. The biasing current I_{BIAS} determines the matching of the LNA's ports to 50Ω. The best match was obtained at I_{BIAS} = 1mA to 1.1mA (compared to 1.08mA required during simulations).

A wide range of gain control was obtained by varying the other biasing current, $I_{CONTROL}$, in the range of 25µA to 525µA. For all the values required for gain control over a maximum range, the total current consumption of the LNA remains lower than 7.5mA.

VI.2.2. Gain control

The value of I_{BIAS} needed to match the input and output impedances of the LNA is around 1.1mA. It was observed that an increase in I_{BIAS} to 1.4mA led to large improvements in the LNA's bandwidths without sensibly degrading the impedance match. Therefore, two separate gains 'systems' are enabled: one LNA working at I_{BIAS} = 1mA and the other at 1.4mA. Fig. 13 presents the gain and bandwidth profiles for these two conditions. The range of achievable gains is limited by the lowest possible value of $I_{CONTROL}$. Moreover, since the gain of the LNA is ideally $A_V = V_{OUT}/V_{IN} = I_{BIAS}/I_{CONTROL}$, lower values of $I_{CONTROL}$ are needed to achieve the same LNA gain at I_{BIAS} = 1.4mA than at I_{BIAS} = 1mA.

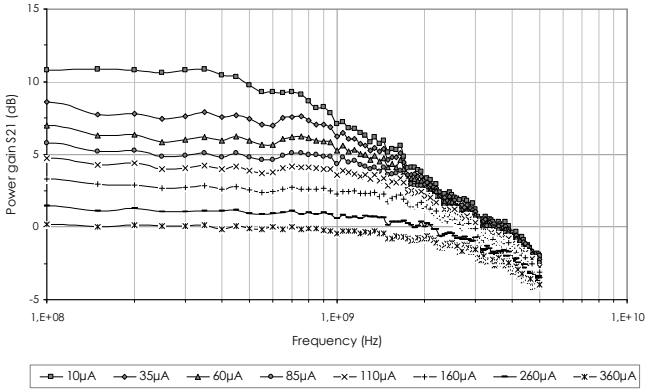
The rise in power consumption consequent to the rise in I_{BIAS} is neutralised by the lower values of $I_{CONTROL}$ needed for higher gains, and the overall current consumption of the LNA is similar for the two cases: I_{BIAS} = 1mA and I_{BIAS} = 1.4mA.

It can be observed that for an equivalent gain (for example, 10dB), the improvement in the bandwidth is of the order of 700MHz. Inversely, the bandwidth of the LNA biased under 1mA is greater than 1GHz only for gains lower than 8dB, whereas the 1GHz point is attained by the 1.4mA system for gains as high as 12dB.

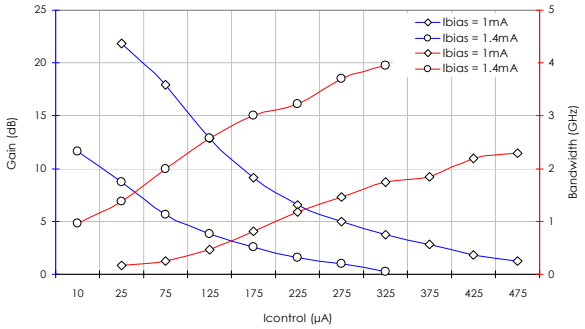
The figure above shows that a trade-off has to be made in the LNA's operation. If gain is privileged, the 1mA system is better, whereas the 1.4mA operation is better adapted when moderate gains *and* high bandwidths are required (as is the case in multi-standard transceivers).

Fig. 13 also depicts a representative case of the frequency-stability of the power gain profiles. It can be observed that the gain profiles are flat and stable upto the GHz range. Intermediate gains can be obtained by tuning $I_{CONTROL}$ to the desired value.

It must be noted that the highest bandwidths of the differential LNA are of the order of 4GHz, and the best bandwidth to transition frequency (BW_{3dB}/f_T) ratio of around 0.1 is achieved. The significance of this performance will be highlighted below in the section comparing the new solution with existing ones.



a

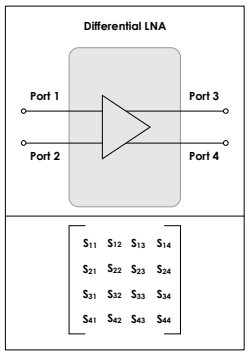


b

Figure 13 : Gain and bandwidth of the differential LNA for different $I_{CONTROL}$; at V_{DC} = ±2.5V and I_{BIAS} = 1.4mA
a) Gain profiles; b) gain control

VI.2.3. Scattering parameter performance

Since the differential LNA is a 4-port device, the corresponding scattering parameter matrix contains 16 single-ended elements, as shown below.



S_{31} and S_{42} are, respectively, the gains P_{OUT}^{+}/P_{IN}^{+} and P_{OUT}^{-}/P_{IN}^{-}. Since the LNA is supposed to be perfectly symmetrical, the two gains should be similar. Figures V.28 above presented representative gain-frequency profiles. Fig. 14 presents the control of the two gains, versus $I_{CONTROL}$. It can be observed that the two profiles are similar, and the difference between them never exceeds 0.5dB. The values are given for the 1mA system.
Fig. 15 presents the other important S-parameters of the differential LNA. These parameters remain similar for the entire range of values of $I_{CONTROL}$ required for the gain control. A representative case, for gain = 10dB, is thus presented.
S_{11} and S_{22} are the reflection parameters at the two inputs ports; while S_{33} and S_{44} are those at the outputs. As can be seen in fig. 15, the frequency range of the port matching excellent: all S_{ii} parameters are lower than -10dB upto 5GHz. This limit is well beyond the desired applications of the differential LNA (wireless communications standards upto about 2.5GHz).

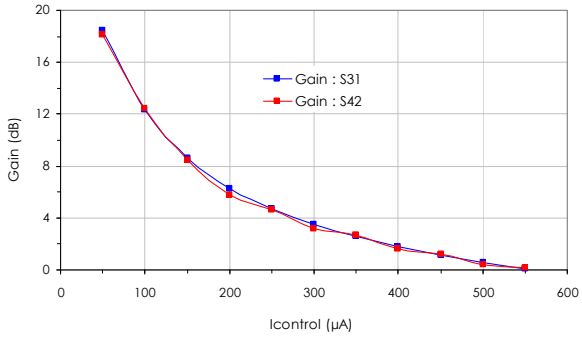


Figure 14 : Symmetry between the two amplification channels of the differential LNA : gain versus $I_{CONTROL}$; at V_{DC} = ±2.5V and I_{BIAS} = 1.1mA

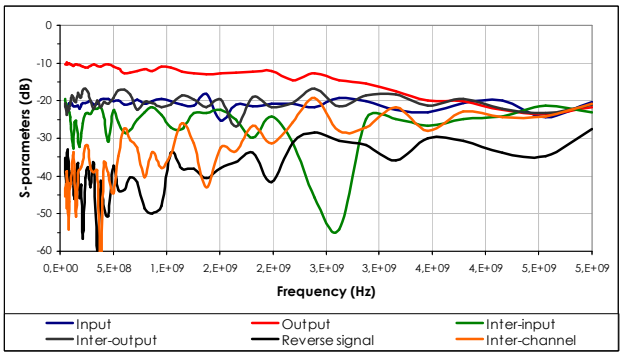


Figure 15 : S-parameters of the differential LNA, for gain = 10dB; at V_{DC} = ±2.5V and I_{BIAS} = 1mA

S_{13} and S_{24} represent the strength of the reverse signal. They are both lower than -20dB upto 5GHz. Moreover, this performance is independent of the LNA's gain.
Since the differential LNA is made of two amplifier channels in parallel, no amount of signal incident at the input of either of these channels (ports 1 and 2, respectively) must be amplified at the output of the other channel (ports 4 and 3 respectively). Similarly, no reverse signal from ports 3 or 4 must leak to the other channel's input. In other words, the terms S_{14}, S_{41}, S_{23} and S_{32} should be as close to zero as possible. Both S_{14} and S_{41} are lower than -20dB for a major part of the frequency range, signifying that less than 10% of the signal crosses over from one channel to the other.
The two amplification channels of the LNA are ideally isolated from one another. The two input ports and the two output ports must be entirely independent of one another. Terms S_{12} and S_{21} stand for the isolation between the two inputs and S_{34} and S_{43}, between the two output ports. The amount of signal leakage between the two input ports is lower than -20dB for a majority of the gain control range; the isolation between the output ports 3 and 4 is lower than -15dB.

VI.2.4. Noise performance

The noise introduced by the differential LNA is a preponderant parameter, especially given the high number of noise sources (transistors). All other conditions being invariable, the noise of the differential LNA will be 3dB higher than its single-ended counterpart, because the differential structure has twice the number of components. It was found during simulations that the collector current I_C and the base resistance r_B are the major noise contributors in the input transistor of the LNA; and that the input transistor itself is the major contributor to the overall noise of the LNA. The gain of the new differential LNA is a function of $I_{CONTROL}$; however, an increase in $I_{CONTROL}$ leads to a rise in I_C; this rising I_C should manifest itself in the form of a rise in the noise figure of the LNA. This was found to be the case (fig. 16).

One of the biggest advantages of the new LNAs is the inverse proportionality between the gain and $I_{CONTROL}$. Besides the apparent advantage of low power dissipation at high gains, the highest gains are obtained for the lowest noise figures. This, for example, the simulated noise figure of the differential LNA is only 1.04dB for a gain of 23dB; it rises to 4.16dB as the gain decreases to around 10dB.

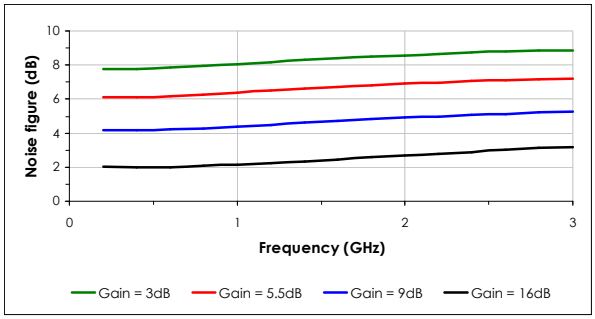


Figure 16 : Noise figure profiles for the differential LNA

Additional analyses determined the major noise contributors of noise in the new LNA. Despite the increase in transistor emitter area and partitioning of the base (to reduce I_C and r_B, respectively), the input transistor (Q_1) was found to be the biggest contributor of noise in the LNA. It accounted for 22.5% of the noise (19.25% from I_C and 3.25% from r_B). Transistors Q2 and Q3 of the core LNA gave 10.2% and 9.4% of the total noise, respectively, and were the next highest contributors. The NPN transistors in the impedance matching network contributed about 8.5% each.

VI.2.5. Transient performance

The P_1P_3 and P_2P_4 combinations, which are the forward amplification channels of the differential LNA, were tested for their response to a sinusoidal wave (of 25mV peak-to-peak amplitude and 100MHz frequency). The variation of the output voltage (and thus the gain) is inversely proportional to $I_{CONTROL}$, with peak gains of around 10 times (or 20dB) being attained, thus showing a good correspondence with the AC and S-parameter gain performance. The transient response is similar for the P_1P_3 and $P2P_4$ combinations.

VI.2.6. Gain compression and linearity

The input signal's power was varied in equal steps over a wide range, to determine the LNA's linearity. The input-referred 1dB compression point IP_{1dB} of the LNA was determined to be -24.8dBm. It must be remembered that this is the linearity performance of the differential LNA in single-ended operation, that is, the input power was provided at the positive input port and the output observed at the positive output port. The linearity was observed to be approximately similar for different values of LNA gain; and for the two channels.

VI.2.7. Intermodulation products

To study the deleterious effect of a strong blocker in a channel adjacent to the desired one, two tones of equal intensity (-30dBm) were applied at the desired frequency (1 or 2GHz) and at a neighbouring frequency (the separation between the two tones was alternately fixed at 200kHz, 2MHz and 20MHz). The smallest channel separation of 200kHz models a GSM system, whereas 2MHz and 20MHz can be used alternately for WCDMA and wideband standards like UWB (section II.1.3 above).

The response of the LNA to such a stimulus, studied on a network analyser, led to the determination of the third-order intermodulation product (IP3) under various conditions (variable fundamental frequencies, channel separation and LNA gains).

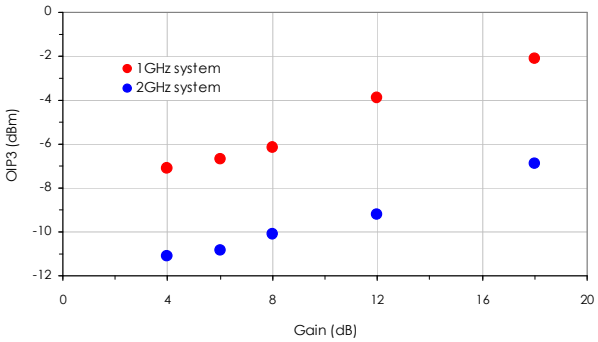


Figure 17 : OIP3 between P_1 and P_3 of the differential LNA as a function of the LNA's gain; at V_{DC} = ±2.5V and I_{BIAS} = 1.1mA

Fig. 17 presents, for a tone separation of 20MHz, the output-referred IP3 of the LNA, versus its gain. For the 1GHz system (the two tones are placed at 1GHz and 1.02GHz), the output-referred intermodulation point varies between -7dBm and -2dBm. When the two tones are placed at 2 and 2.02GHz, OIP3 varies from -11dBm to

-7dBm. It is noteworthy that the best OIP3 is obtained for higher gains (and lower consumption), thus easing the fundamental trade-off in LNA design.
Placement the blocker tone closer to the fundamental (200kHz or 2MHz instead of 20MHz) modified the intermodulation performance of the LNA. When the fundamental tone is placed at 1GHz and the blocker at 1.0002, 1.002 and 1.02GHz, the OIP3 of the LNA is, respectively, -3.3dBm, -4.35dBm and -3.91dBm. For the 2GHz fundamental tone, with blockers at 2.0002, 2.002 and 2.02GHz, OIP3 is, respectively, -7.3dBm, -2.2dBm and -8.9dBm. These are the values obtained at a LNA gain of 10dB.
The performance of the LNA in terms of intermodulation products is best when the tones are separated by 2MHz.

VI.2.8. Temperature stability

The temperature of the wafer was varied using the temperature regulator, and the performance control was studied for a temperature range of -25°C to +75°C. Fig. 18 depicts the gains and bandwidths of the LNA at different temperatures. The gain profiles are quite similar to one another: the highest achievable gain varies from 16.4dB at -25°C to 18.8dB and +75°C (the highest gain at ambient temperature was around 18dB); the lowest is always around 0dB. This is the performance at I_{BIAS} = 1mA. For the entire range of temperatures, the maximum difference in the gain profiles is 2dB.
The variation of the bandwidth with $I_{CONTROL}$ is much wider. However, when considering the gain-bandwidth variation with respect to one another, it becomes clear that the variations are less worrying than those indicated by the figure. For example, at a gain of around 4dB, the bandwidth varies from 2.1GHz at -25°C to 1.7GHz at +75°C, through 2GHz and 1.75GHz at 0°C and +50°C respectively. For a corresponding gain, the bandwidth at ambient temperature was 1.8GHz.
Both the gain and the bandwidth of the LNA improve at temperatures lower than 27°C; and the deterioration at temperatures higher than 27°C is very small (less than 1dB in gain, and less than 0.2GHz in bandwidth, for the entire range of gain control). Therefore, the LNA's performance is deemed temperature-stable over a 100°C temperature range around the ambient temperature.

VI.2.9. Statistical analyses

LNAs situated on five different chips were tested under the same biasing conditions to determine the stability and reproducibility of the LNA's performance. Fig. 19 depicts the gain control of each of the chips, as well as the 3dB bandwidth. This is the performance of the five chips at I_{BIAS} = 1.4mA. The difference between the gains of the five LNAs, for the entire range of biasing currents, is less than 1dB; the 3dB bandwidths of all five specimens are greater than 1GHz for the entire range of gains and show a maximum variation of about 0.4GHz between them.
For the five LNA prototypes, the S-parameters were also measured for frequencies ranging from 50MHz to 5GHz. The worst-case parameter variations over this multi-GHz range are : input matching S_{11} between -13.09dB and -13.89dB; output matching S_{33} between -9.52dB and -9.97dB; reverse signal isolation S_{13} between -22.5dB and -23.9dB for the five chips.
The sub-dB variations in the LNA's scattering parameters show the excellent reproducibility of its performance.

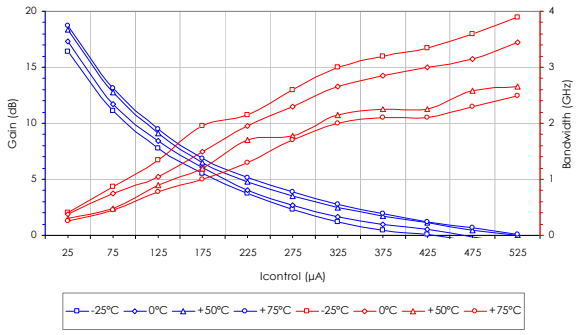


Figure 18 : Gain control of the differential LNA, for different temperatures; V_{DC} = ±2.5V I_{BIAS} = 1.1mA

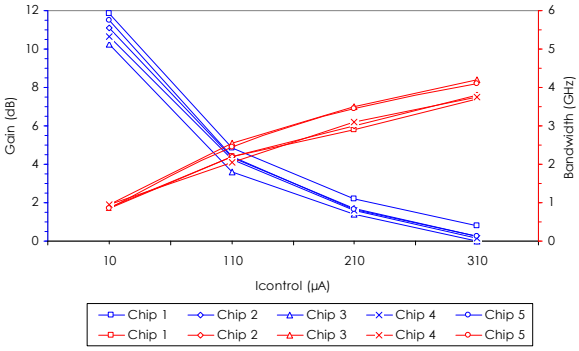


Figure 19 : Gain control and bandwidth of the five LNA prototypes; at V_{DC} = ±2.5V and I_{BIAS} = 1.4Ma

VI.3. RESUME AND COMPARISONS WITH SIMULATIONS

The new differential LNA was fabricated with the intention of validating it as a viable block for wireless communications receivers which use differential signal processing. Implemented in the same 0.35µm SiGe BiCMOS technology as the single-ended version above, the LNA occupies 0.08mm² of space (without pads). This remarkably small size is even more significant in view of the differential architecture.
The extreme care taken to ensure symmetry between the two amplification channels during the layout design of the LNA bore fruit in the good correspondence between the performances of the two channels. This symmetry was

observed in the gain control of the two channels and in the S-parameters.

Table III : Synopsis of the differential LNA's measured and simulated performances, at V_{DC} = ±2.5V

Impedance-matched Wideband Differential LNA			
Parameter	Conditions	**Simulations**	**Measurement**
Gain ; Bandwidth	I_{BIAS} = 1.4mA	0 – 24dB; BW> 1GHz	0 – 13dB; BW > 1GHz
Consumption		6.5mA to 8mA	5.5mA to 7mA
Input reflection	0 – 3GHz	< -22dB	< -11dB
Output reflection	0 – 3GHz	< -15dB	< -11dB
Reverse rejection	0 – 3GHz	< -60dB	< -20dB
Inter-input isolation	0 – 3GHz	< -70dB	< -20dB
Inter-output isolation	0 – 3GHz	< -70dB	< -15dB
Inter-channel isolation	0 – 3GHz	< -80dB	< -20dB
Single-ended IP_{1dB}	1GHz	-22.5dBm	-24.8dBm
Single-ended OIP3	2MHz	-5.94dBm	-3.91dBm
Noise figure		1dB – 9dB NF α 1/Gain	- not measured -

Working at V_{DC} = ±2.5V, the gain of the LNA could be controlled using two separate profiles. In the first of the profiles, obtained using I_{BIAS} = 1mA, gains varying form 0 to 22dB were obtained (similar to the simulated range), but the bandwidths were lower than 2.5GHz. In the second, at I_{BIAS} = 1.4mA, the range was limited to 0 to 13dB, but bandwidths upto 4GHz were obtained; 3dB bandwidths from DC to at least 1GHz were evinced for all the values of the gain. Under both these conditions, the total current consumed by the LNA was lower than 7.5mA, and inversely proportional to the gain.

In terms of the scattering parameters of the LNA, the reflection coefficients S_{11} through S_{44}, indicators of the impedance matching at the four ports, were excellent: lower than -10dB for all frequencies upto around 3.7GHz. The reverse signal rejection (S_{13}, S_{24}), the inter-channel isolations (S_{14}, S_{41}) and the isolation between the two input ports (S_{12}, S_{21}) were all better than 20dB for all gains of the LNA, and for all frequencies upto 5GHz. The isolation between the two output ports (S_{34}, S_{43}) was only slightly unfavourable: better than 15dB, for the same frequency range. The linearity of the LNA in the single-ended mode was found to be around -25dBm, a slight deterioration when compared to simulations. The measured third-order intermodulation product is 2dBm better than the simulated value.

The differential LNA gave good results under different temperature conditions : at temperatures lower than the ambient value of 27°C, both the gain and the bandwidth improved; and for temperatures between +27°C and +75°C, the deterioration in the performance was small. The performance of the differential LNA is reproducible, as was shown by the similarity of the performances of five different prototypes.

VI.4. COMPARISONS WITH EXISTENT LNAS

Table IV shows the performance of the new LNA with respect to other differential LNAs taken from recent publications. The performance of the new LNA is given for two gains, 0dB and 13dB, which form the two ends of the gain control range. The new LNA is the smallest differential LNA presented so far, being at least 7 times smaller than its nearest contender. The consumption of the new differential LNA, lower than 7mA for most of the gain control range, is better than a large majority of existent differential LNAs (between 4.5mA [26] and 20mA [38], the average being situated around 10mA [22],[31]).

Gain control in differential LNAs is a rare feature: the only other differential LNA which includes control (using an additional stage added to the core amplifier) has gains varying between 20 and 28dB, consuming 5 and 25mA for the two extremes respectively [22]. In comparison, the new differential LNA can provide easy control from 0 to 13dB, and its consumption is inversely proportional to the gain.

Most differential LNAs are narrow-band structures, with 3dB cut-off within some hundreds of MHz around the centre frequency. The new LNA allows bandwidths upto 4GHz, and its bandwidth is always greater than 1GHz for all values of gain. At 6dB of gain, the bandwidth extends from 0Hz to 2GHz.

Bandwidths of upto 4GHz are obtained for the new differential LNA, signifying bandwidth to transition frequency (BW_{3dB}/f_T) ratios of upto 0.1, or 10%. In no other LNA does the 3dB bandwidth exceed 3% of the constituent transistor's f_T: the RF LNAs in [35],[11],[34],[6],[16] have ratios of 0.01, 0.013, 0.027, 0.007 and 0.005 respectively.

Besides the gain profiles, the new LNA is wideband in terms of port impedance matching. Excellent matches are achieved at all the four ports for frequencies varying from 0Hz to at least 4GHz.

The measured IP_{1dB} is -24.8dBm. This is the single-ended IP_{1dB}. Simulations gave a corresponding value of -22.5dBm. The real linearity of the differential LNA is determined by the differential-mode operation. Unfortunately, this parameter could not be measured because of the single-ended apparatus. However, the close resemblance between the simulated and measured single-ended IP_{1dB} permits us to conclude that the measured differential IP_{1dB} of the LNA will be around the simulated value of -11.8dBm. This is 8dBm better than the linearity of the GSM900/PCS1900 dual-band LNA in [31], and 8dBm lower than the highly linear WCDMA LNA in [26].

Table IV : Comparison between the new differential LNA and some recent solutions

Reference **Year**	**[22]** **2001**	**[31]** **2002**	**[26]** **2003**	**[38]** **2006**	**[25]** **2006**	**This work**	
Frequency **Applications**	0.9GHz GSM	0.9/1.9GHz GSM/PCS	2.14GHz WCDMA	1.8/2.1/2.4GHz DCS/UMTS/LAN	2.4/5.0GHz WLAN/802.11a	**0 – 3GHz** **Wideband**	
Technology **Passives** **Area**	0.35µmCMOS 12 -	Bipolar 8 0.54mm²	- n.a. - 8 -	0.13µm CMOS 10 0.75mm²	.25µm BiCMOS 8 -	**.35µmBiCMOS** **0** **0.08mm²**	
Peak gain **BW_{3dB} : f_L** **f_H**	17.5dB 0.75GHz 1.05GHz	20dB 0Hz 3GHz	10.8dB -	13.5 – 28.5dB 1.6/1.7/2.15GHz 2.0/2.5/2.65GHz	24/24dB -	**0dB** **0** **4GHz**	**13dB** **0** **1GHz**
Consumption **Dissipation**	8mA 21.4mW	13mA 65mW	4.5mA - na -	20mA 24mW	- na -	**7.5mA** **37.5mW**	**5.5mA** **27.5mW**
Z_{IN} match **Z_{OUT} match**	< -10dB -8dB	< -10dB -	< -20dB < -10dB	< -10dB -	- -	**< -12dB** **< -11dB**	
IIP3 **IP_{1Db}**	-6dBm -	-3dBm -20dBm	+10dBm -3dBm	-7.5dBm -	- -	**-9.9dBm** **-24.8dBm***	
Noise figure	2.1dB	3.8dB	4dB	5.2/5.6/5.8dB	1.8/2.1dB	**7dB****	**1dB****

* : single-ended measurements. The real differential-mode performance could not be measured, but is expected to be much better. For example, the simulated differential-mode performance IP_{1dB} is 11dBm better than the single-ended value.
** : simulated values

VII. CONCLUDING REMARKS

The aim of this article has been to update the state of the art in low-noise amplifiers for wireless communications receivers.

An exhaustive review of existent LNA solutions (narrow-band and wideband; single-ended and differential) led to the conclusion that today's LNAs are based on three distinct topologies: single-transistor, cascode and two-stage. Cascode-based LNAs are the most widespread. Most LNAs are narrow-band structures. Wideband LNAs provide bandwidths of the order of gigahertz, but at the expense of increased consumption and noise, and moderate gains. It was also observed that gain control in low-noise amplifiers is a rare phenomenon, even though it is deemed indispensable in today's mobile environments.

These introductory sections helped establish the specifications that would be required of a LNA for it to be suitable for transceivers treating different standards. The ultimate aim was to design a LNA that exhibits the following properties: competitive performance (in terms of gain, noise, consumption, linearity, etc.); small size (by reducing the number of passive elements); high bandwidths (enabling the new LNA to replace several parallel-connected narrow-band devices found in today's multi-standard receivers); and easy gain control over wide ranges (without overly effecting the other parameters of the LNA).

Two novel low-noise amplifiers were then developed. The first of these was a single-ended configuration, and the second a differential topology. The guiding principle is the same: the connection of two second-generation current controlled conveyors to provide signal amplification. A new category of LNAs was thus developed: conveyor-based amplifiers. Transistor parameters of a 0.35µm SiGe BiCMOS technology were used to design them, and both structures were subjected to various analyses at the simulation level.

Both the new low-noise amplifiers satisfied, at the simulation level, the targets set for them. In order to verify operation in a real environment, they were both fabricated in a f_T = 45GHz 0.35µm SiGe BiCMOS technology. This technology provides an excellent performance-cost-form factor trade-off.

Simplification during the circuit design stage enabled final configurations that use only three NPN transistors in their core signal chain. These topologies are entirely active. This absence of passives results in LNAs with very small form factors (0.02mm² and 0.08mm², respectively, for the single-ended and the differential versions). These are the smallest LNA noted so far.

Gain control over wide ranges (0 – 20dB) is obtained by simply varying the bias current. This is the widest range of gain control encountered for LNAs.

Both the LNAs present wideband matching (the reflection coefficients at all the ports of both LNAs is lower than -10dB for frequencies extending from 0 to over 4GHz).

Since the highest gains are obtained at lowest control currents, the LNA dissipates the lowest power when providing moderate to high gains. The total consumption of the single-ended and the differential LNA is lower than 4.5mA and 8mA, respectively, for the entire range of gains between 0 and 20dB.

The inverse proportionality between the gain and control current translates to another significant advantage of in the new topologies: best noise performance at high gains. The noise figures of the single-ended and differential amplifiers vary between 1dB at 20dB of gain, to about

4dB at gains of 5dB for the single-ended version and 10dB for the differential version.
The single-ended and differential LNAs have input-referred P_{1dB} comparable to the best linearity performances evinced by existent LNAs.
Moreover, the performances of these circuits are stable to variations in ambient temperatures throughout a 100°C range between -25°C and +75°C.
And finally, the performances of all the circuits are reproducible, as was shown by statistical analyses carried out on each of them.

More complete characterisation, using multi-port measurement apparatus, would further highlight the advantages of the differential low-noise amplifier.
The noise of the two low-noise amplifiers could not be characterised at the measurement level because of faults in the measurement apparatus which were, unfortunately, outside our control. Given the close correspondence between the measured and simulated performances (gain profiles, consumption, linearity, intermodulation products, port impedance matching, etc.) we expect the noise figure of the two LNAs to resemble the values obtained from simulations, that is, as low as 1dB at high gains, and upto 4dB at low gains.

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