Design and Comparison of High Bandwidth Limiting Amplifier Topologies

Umut Yilmazer, Caglar Yilmazer, Ali Toker

Electronics and Communication Engineering Department, Istanbul Technical University,Istanbul, Turkey
yilmazerumut@gmail.com caglaryilmazer@hotmail.com ali.toker@itu.edu.tr

Abstract

This paper describes and compares many of inductorless limiting amplifier topologies that have been introduced in the technical literature so far. We start with resistor loaded NMOS differential amplifier as a reference to our work. Then we investigate bandwidth enhancement techniques such as negative Miller capacitance, active shunt peaking, active feedback and negative impedance conversion. We also propose an improvement for active shunt peaking topology to reduce ISI jitter especially for large input signals. Maximum input loading of amplifiers is specified as 250fF and output loading can be as high as 50fF. Therefore, inverse scaling technique is applied in all amplifiers to further increase the bandwidth. All topologies are designed in 0.18µm CMOS technology and were simulated in Cadence Design Environment. They are designed for a voltage gain of 32dB and 1.2Vpp output voltage swing. Each of them consumes 54mW to make a fair comparison.

1. Introduction

The demand for high speed communication systems has increased due to the rapid growth in the multimedia and internet communication systems. Today, modern high speed data link systems use multi-gigabit data rates. As data rates increase, attenuation of the transmission medium increases and the receiver side of the communication channel suffers from the small signal levels. For reliable operation of the following stages, attenuated signal must be amplified to a sufficient voltage level. In front-end circuits, limiting amplifier (LA) has the responsibility of satisfying the requirements of the subsequent clock and data recovery (CDR) circuits. Some of these requirements are having enough gain and wide bandwidth to provide high voltage swings to CDR and to introduce low intersymbol interference (ISI). They should also have low input referred noise and offset not to limit the overall RX sensitivity [1]. Design of such high voltage gain and wide bandwidth amplifiers is more challenging in CMOS technologies than the other technologies such as SiGe, GaAs. Due to the lower cost and higher integration capability of CMOS technology, the researches on the implementation of high speed ICs become very important in the last years.

In this paper, we describe the design of 5 different LAs topologies in 0.18µm CMOS technology. The design procedure and comparison of the topologies are given with simulation results.

2. Limiting Amplifiers

LAs are usually used between transimpedance amplifier (TIA) and CDR in optical links [1]. The output of TIA usually suffers from very small signal amplitudes. For this reason, TIA is followed by additional gain stages to boost the signal to logical levels [2]. For small input levels, LA operates in linear regime. However, it goes into the limiting region for larger input levels and its output amplitude gets constant. LAs are also used directly at the chip input to amplify the signals attenuated by the link or a continuous time linear equalizer. The link can be a coaxial or twisted pair cable or PCB trace. Attenuation of the link can be very high for long cable lengths and high data rates. Therefore, LAs should have high gain, wide bandwidth and low input referred noise as discussed before.

There are many techniques that have been introduced so far in order to increase the gain bandwidth product of amplifiers. Overall gain can be increased by cascading the stages. However, overall bandwidth of the system will be lower than the bandwidth per stage. Assuming that the gain bandwidth product of a stage is fixed for a given power consumption, there should be an optimum number of stages that makes the overall bandwidth maximum for a given gain [2]. It is mathematically shown in [1] that for n identical cascaded gain stages and first order systems as shown in Fig. 1, the required gain bandwidth product per stage can be given as

$$GBW_c = \frac{GBW_{tot}}{A_{tot}^{\,1-1/n}.\sqrt{2^{1/n}-1}} \quad (1)$$

where GBW_{tot} is the total gain bandwidth product of the system and A_{tot} is the overall gain of the system. It can be shown that for a constant A_{tot}, increasing the number of stages beyond a number does not increase the bandwidth much. However, it makes the input referred noise worse. Therefore, use of very large number of stages is avoided in limiting amplifier design.

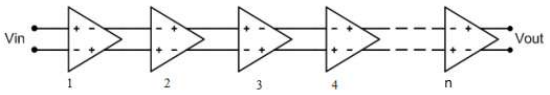

Fig. 1. Cascaded limiting amplifier stages

There are many topologies in the literature to enhance the bandwidth of amplifiers. If the bandwidth per stage is maximized for a fixed gain, then the overall GBW is maximized. Therefore, we will discuss the most popular inductorless bandwidth increasing topologies in the literature. For comparison purposes, overall gain, power consumption, input and output loading of the LAs are kept constant for all topologies. In all designs, input capacitance of LA is 250fF and the load capacitance that is the input of CDR circuit is assumed 50fF. Since the input capacitance is bigger than the loading capacitance, inverse scaling [3] technique is used in our design. This technique makes the driven stage smaller than the driving stage and a significant bandwidth extension is achieved without

changing the gain per stage. This method is mostly useful for the amplifiers which receive the input signal from off-chip source due to their large input capacitance. However, all other techniques discussed in the next sections can be used in wide bandwidth amplifier design.

2.1. Resistor Loaded Amplifier

The simplest gain stage available in high speed circuits is resistor loaded differential amplifier shown in Fig. 2. Resistor is generally implemented with poly layer without salicide. Its GBW is $g_{m1,2}/C_L$. It can be optimized by maximizing g_m and minimizing C_L. If a signal with a high voltage level, V_{DD}, is applied to one side of the differential pair, the tail current is steered to that side and a voltage drop, $R.I_{tail}$, is created across the load resistor. If the threshold voltage of M1-2 is higher than this voltage drop, M1 or M2 stays in the saturation region. Gain of a single stage can be written as

$$A_{vi} = \frac{g_{m1,2}}{I_{tail}} I_{tail} R \qquad (2)$$

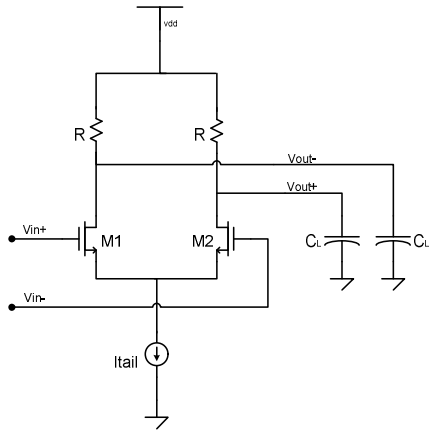

Fig. 2. Resistive Loaded Differential Amplifier Gain Stage

$R.I_{tail}$ value which guarantees either M1 or M2 works in saturation region should be maximized to obtain the optimum bandwidth. In order to picture this, assume that the amplifier stage drives a replica of it, which means that the output capacitance of the amplifier is its input capacitance. For a constant tail current; if load resistor values are divided by a constant value x, widths of differential pair transistors must be multiplied by x^2 in order to obtain the same gain. For x>1, widths of differential pair transistors increase which boosts the value of loading capacitance by x^2. Therefore, bandwidth of the circuit decreases. However, if x<1, capacitance of the driven stage decreases and hence bandwidth increases. Since $R.I_{tail}$ is limited by the threshold value of M1-2, maximizing $R.I_{tail}$ optimizes the bandwidth. It is obvious from the equation (2) that for a constant gain, if the tail current of the gain stage is chosen then the load resistor, g_m and width of all transistors can be determined.

2.2. Negative Miller Capacitance

Bandwidth of the previous circuit can be improved using negative Miller capacitance method. In this method, two capacitors are connected across the noninverting nodes of the amplifier to cancel the some part of the amplifier's input capacitance. If a capacitance C_i is connected across the noninverting nodes of an amplifier, effective miller capacitance at the input of the amplifier becomes $-C_i.(1-A)$, where A is the gain between these noninverting nodes. The gain, A, must be greater than 1 to apply this method. A resistive loaded gain stage that incorporates negative Miller capacitance is shown in Fig. 3. Efficiency of this method depends on the cutoff frequency of capacitors and their series resistances. We used MimCap in this design. Negative miller capacitance compensation method is not used in the first stage due to relatively high input loading specification (250fF). This even increases the bandwidth because Miller capacitance does not load its output.

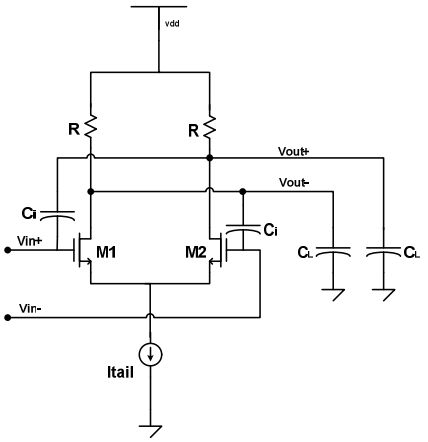

Fig. 3. Negative Miller Capacitance

It should be also noted that increasing the Miller capacitance too much can cause peaking in AC gain response. Therefore, suitable capacitance value should be chosen carefully.

2.3. Active Shunt Peaking

Gain of a resistor loaded single stage is proportional to $g_m.R_L$. As the frequency increases, equivalent load impedance and g_m decrease due to the capacitive effects. It is known that impedance of an inductance increases as the frequency increases. If an inductance is added in series with the load resistor, it introduces a zero and the equivalent load impedance can be held constant within a wider frequency range [4]. Thus, the bandwidth of an amplifier can be increased with this method which is also known as shunt peaking.

On chip implementation of the inductors requires a large silicon area and a good modelling that brings extra cost. Instead of using passive inductors, we can implement active inductors with transistors. An active inductor can be implemented using an NMOS and resistor as shown in Fig. 4. Neglecting C_{gd} and r_o, the impedance seen from the source can be written as in the equation (3).

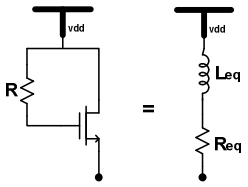

Fig. 4. Active Inductor

$$Z_{eq} = \frac{1 + sC_{gs}R}{g_m sC_{gs}} \quad (3)$$

It is seen in equation (3) that if $R>1/g_m$, the circuit behaves like an inductor.

The drawbacks of active inductors are their noise and their large voltage drop that is caused by NMOS threshold voltage. The voltage drop across the active inductor limits its operating range. If the gate voltage is biased one threshold above V_{DD}, the voltage drop across the active inductor is reduced. This configuration is depicted in Fig. 5 [3]. In this configuration, load transistor is in saturation region and its small signal behavior does not change. The current drawn from V_{DD} also does not change significantly so that power consumption does not change. This technique does not cause any reliability problem because drain-source voltages remain below 1.8 V [3].

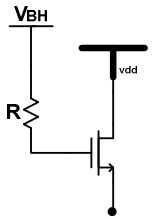

Fig. 5. Low voltage drop active inductor

Differential amplifier configuration with active inductors is given in Fig 6. DC gain of this amplifier is less sensitive to process, temperature and biasing, since the gain is the ratio of widths of two NMOS transistor for $L_1=L_2$ and neglecting the body effect [3].

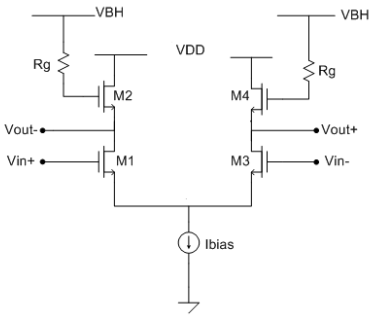

Fig. 6. Active inductor loaded differential pair

DC gain of the amplifier in Fig. 6 is determined according to the ratio of the differential pair and load transistors. For $R_g=0$, bandwidth of the stage equals to g_m/C_{out}. According to this equation, it is understood that decreasing the width of the transistors increases the bandwidth. This is because C_{tot} is proportional to the widths of transistors, but g_m is proportional to the square root of the width. However, there is a limit for this because if widths are reduced, overdrive voltages of active loads also increase. That causes differential NMOS transistors to gointo the triode region. Since the overdrive voltage of the input transistors also increases, this may cause the tail current source enter the triode region. Increasing overdrive voltage of input transistors may cause the tail current source go into triode region. Tail current value should be high in order to increase cutoff frequency of transistors. Moreover, output of a stage is the input of next stage. Therefore, voltage difference between output nodes should not be higher than one threshold voltage to keep input transistors in saturation region. During the design, after choosing aspect ratios of transistors, R_g value is determined. It is clear from equation (3) that increasing R_g increases the equivalent inductor value. For this reason, R_g values are increased until a peaking in the frequency response is observed.

The circuit in Fig. 6 has an issue that is not disscused in the original paper [3]. If long consecutive bits occur at the input, one side of differential pair enters the cut-off region and source node of active load transistor increases towards V_{DD}. Load resistance is high in this situatuion, which causes long output settling time. If a single reverse bit comes after long consecutive bits, it tries to pull down the output from a high value, which in turn causes ISI jitter.

The problem mentioned above can be solved if a small amount of current leakes over the load transistor even when differential pair transistor current is zero. One solution to this problem is connecting a PMOS transistor with a low aspect ratio between two output nodes. Gate of this PMOS is connected to ground so that it is kept in the triode region and it is used as a resistor. A little current flows through this PMOS so that active loads do not go into cut off region. Resistance of this PMOS transistor must be much higher than the differential resistance of the active loads not to affect the voltage gain. Resistance of differential active load is 2/gm. Resistance value of PMOS on resistor is chosen as 80/gm. Proposed improved amplifier stage is given in Fig. 7.

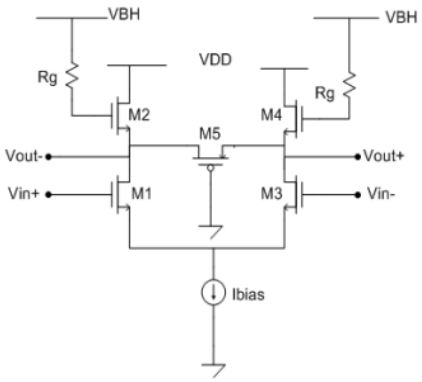

Fig. 7. Active inductor loaded stage with improved scheme

We designed two 6 stage amplifiers without and with the PMOS resistor shown in Figure 7. We simulated these two amplifiers at 5Gbps random data with 200mV input signal amplitude. The eye diagrams are shown in Fig. 8 that demonstrates the improvement. The ISI jitter is 9.4ps and 0.5ps for amplifiers without and with the PMOS resistor respectively.

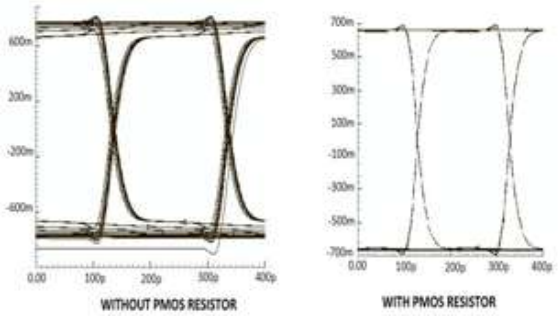

Fig. 8. Eye diagrams of active inductor loaded differential pair without and with PMOS resistor @5Gbps

2.4. Active Feedback

In limiting amplifiers, cascading technique is widely used in order to obtain both high gain and wide bandwidth at the same time. If n identical second order gain stages are cascaded to each other, overall bandwidth is given as [1]

$$BW_{tot} = BW_c.\sqrt[4]{2^{1/n} - 1} \tag{4}$$

where BW_c is required bandwidth per stage. It is understood that for the same overall bandwidth, required bandwidth per stages smaller for the second order gain stages with respect to the first order gain stages. Second order active negative gain stages can be used in order to obtain wide bandwidth. In Fig. 9, active negative feedback architecture is shown.

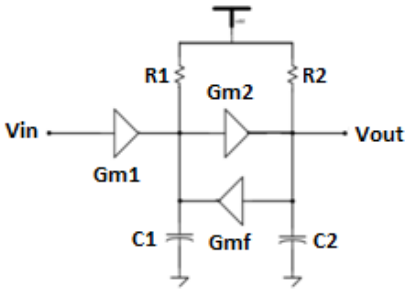

Fig. 9. Active feedback architecture [1]

For this architecture, overall transfer function can be written as

$$\frac{V_{out}}{V_{in}} = A_{vo}\frac{{\omega_n}^2}{s^2 + 2\zeta s\omega_n + {\omega_n}^2} \tag{5}$$

where

$$A_{vo} = \frac{G_{m1}.G_{m2}.R_1.R_2}{1 + G_{mf}.G_{m2}.R_1.R_2} \tag{6}$$

$$\zeta = \frac{1}{2}.\frac{R_1.C_1 + R_2.C_2}{\sqrt{R_1.R_2.C_1.C_2(1 + G_{mf}.G_{m2}.R_1.R_2)}} \tag{7}$$

$${\omega_n}^2 = \frac{1 + G_{mf}.G_{m2}.R_1.R_2}{R_1.R_2.C_1.C_2} \tag{8}$$

Since there are two poles in the transfer function, magnitude of the gain decreases after some frequency. Output of the G_{m1} stage is the input of G_{m2} stage. As the frequency increases, voltage gain of G_{m2} stage starts to decrease. However, the equivalent impedance at the output of Gm1 stage has a peak for suitable circuit parameters because it is a second order function. If the impedance has a peak, G_{m1} stage also has a peak in gain response. If this peaking is realized in a frequency range in which the voltage gain of G_{m2} stage starts to decrease, it compensates the frequency behavior of G_{m2} stage and the output response becomes flatter. Therefore, bandwidth of the system increases. It is demonstrated in [5] that GBW of this system can be increased beyond f_T.

Transistor level implementation of the active feedback topology is shown in Fig. 10. In this circuit, M1-M2 realizes G_{m1}, M5-M6 realizes G_{mf} and M3-M5 realizes G_{m2}. It is also shown in [5] that if transistor widths and their currents are multiplied by a scaling factor and resistor values are divided by the same factor, the transfer function does not change. This is the basic approach used in the inverse scaling.

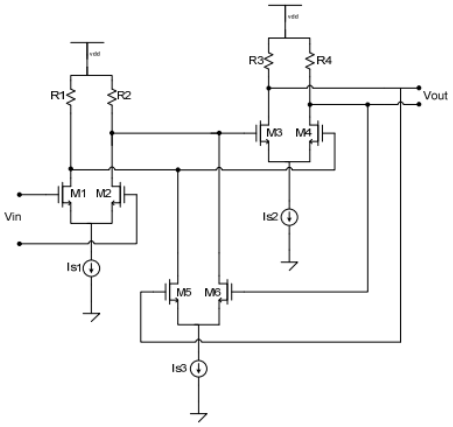

Fig. 10. Active feedback gain stage implementation [1]

2.5. Negative Impedance Conversion (NIC)

A negative capacitance can be used to cancel the total parasitic capacitance at the output port of the amplifier. This reduces the equivalent capacitance of the output port and helps to achieve a significant bandwidth extension. Cross coupled pair shown in Fig. 11 can be used as a negative capacitance. In [6], it is shown that for C_{gs}<<2C and sC_{gs}<< g_m, the equivalent impedance of this circuit can be approximated to

$$Z_{eq} \cong -2/g_m - 1/(sC) \tag{9}$$

This equation shows that a negative resistance is connected in series with a negative capacitance. If this impedance is connected to the output of the amplifier, the negative capacitance increases the bandwidth of the amplifier. Total output resistance of the amplifier can be increased more if a resistor, R_C, is connected parallel to the capacitor shown in Fig. 11. The gain stage with NIC is shown in Fig. 12.

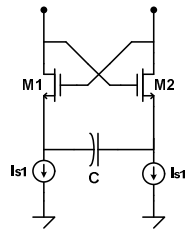

Fig. 11. Negative capacitance generation

In this circuit, $-2/g_m$-R_C comes parallel to the impedance in equation (9) so that the gain of the amplifier increases more without using a high load resistance. Thus, a high GBW is obtained. We implemented the capacitor with 2 NMOS transistors using intrinsic capacitance between gate and shorted source-drain terminals.

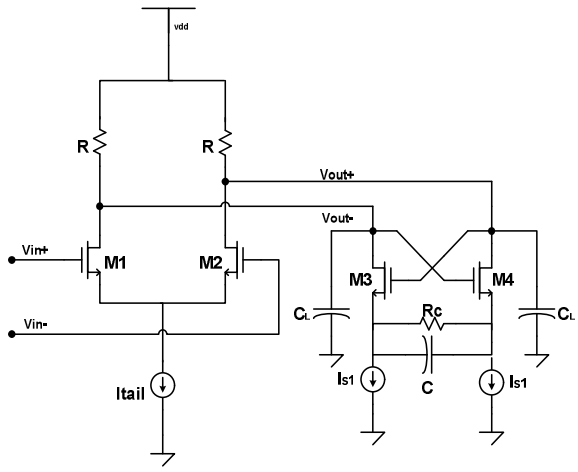

Fig. 12. The gain stage with NIC

3. Simulation Results and Comparison of the Topologies

We designed all of the amplifiers discussed in previous sections. We used six gain stages in all LA topologies except the 4 gain stage in active feedback amplifier due to its large area. We compared the bandwidth and the input referred noise of all amplifiers. Results are summarized in Table 1. Frequency response of all amplifiers is plotted in Fig. 13. According to the results, active shunt peaking has the highest bandwidth. Its bandwidth is 85% higher than the resistor loaded amplifier. The resistor loaded amplifier has the minimum bandwidth. However, the input referred noise performance of the resistor loaded amplifier is the best among all topologies. Active shunt peaking has the worst noise performance due to the noise of the resistors in its active loads. Taking into consideration both bandwidth and input referred noise; negative impedance conversion technique looks like the optimum choice.

Table 1. Comparison of -3dB bandwidth and input referred noise of the amplifiers

Amplifier topology	-3dB bandwidth	Input referred noise @1GHz
Resistor Loaded Amplifier	3.16GHz	44.5µV [rms]
Miller Capacitance	4.47GHz	48µV [rms]
Active shunt peaking	5.9GHz	66µV [rms]
Active feedback	5.2GHz	50µV [rms]
Negative impedance conversion	5.4GHz	54µV [rms]

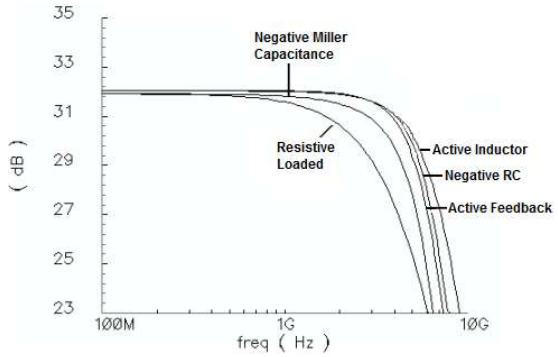

Fig. 13. Simulated **F**requency response of 5 different amplifiers

4. Conclusions

In this work, 5 different wideband limiting amplifier topologies have been discussed and designed in 0.18µm CMOS technology. These topologies incorporate resistive loading, miller capacitance, active shunt peaking, active feedback and negative impedance conversion. None of these topologies include physical bulky inductors. DC gain and power consumption of all amplifiers are chosen the same for comparison purposes. Simulation results show that active shunt peaking has the highest bandwidth. However, it also has the highest input referred noise. Taking bandwidth and input referred noise into account, active feedback and negative impedance conversion techniques look like best choices. Authors believe that this work will be a useful guide for the researchers who are trying to choose a wideband amplifier topology for their application.

5. References

[1] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18-µm CMOS technology", IEEE J. Solid-State Circuits, vol. 38, pp. 2138-2146, Dec. 2003.

[2] B. Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, New York, 2003.

[3] E. Sackinger,and W. Fisher, A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receivers, IEEE Journal of Solid State Circuits, vol. 35, no.12, pp. 1884-1888, 2000.

[4] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd edition, Cambridge University Press, Cambridge, 2004.

[5] S. Galal, "Broadband Devices and Circuits for Data Communication Systems", PhD Thesis, University of California, Los Angeles, 2003.

[6] D. Lee, J. Han, G. Han, and S. M. Park, “An 8.5-Gb/s fully integrated cmos optoelectronic receiver using slope-detection adaptive equalizer,” IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2861–2873, Dec. 2010.