Fault Current Limitation and Contraction of Voltage Dips Thanks to D-FACTS and FACTS Cooperation

J. Khazaie[1], D. Nazarpour, M. Farsadi, M. Mokhtari[1], M. Khalilian[1], and S.Badkubi[1]

[1]Department of electrical engineering, Urmia University, Iran
javad_khazaie@yahoo.com, d.nazarpour@Urmia.ac.ir, *m_farsadi@yahoo.com,* Maghsood.mokhtari@yahoo.com, m.khalilyan@yahoo.com and salman.badkubi@yahoo.com

Abstract

This paper presents the instantaneous response of Distributed Static Series Compensator (DSSC) in fault current limitation of disturbed lines. DSSC has the ability to adjust the impedance of the power line in order to increase the power transfer capacity. The injected voltage is implemented here for limiting the fault currents. The STATCOM which is renowned FACTS device is also implemented for fault current limiting. The fault current will greatly reduce, if the STATCOM make the bus voltage adjacent to fault bus decrease its voltage. Furthermore, it is also revealed that, operation of both DSSC and STATCOM will greatly reduce the fault currents. The effectiveness of the DSSC in reduction of instantaneous voltage dip range during fault current limiting mode, also investigated. PSCAD/EMTC is used to validate the claims.

Key Words: Distributed Static Sereis Compensator (DSSC), Fault Current Limitation (FCL), STATCOM, Voltage Dip

1. Introduction

The increasing power demand and major environmental constraints require a solution for transmission systems. Increasing generation is one of the solutions in high load density networks. This solution on one hand and interconnections between systems on the other hand, increases the fault current in power system. If the fault current rating of the equipment in the system is exceeded, the equipment must be either upgraded or replaced. The both of those solutions for equipment are either very cost or time intensive procedures [1].

So, fault current limiters could be implemented [2]-[4]. Presently investigations are being carried out to study the coordination of the distance protection and the line's apparent impedance variation of these lines used with FACTS (Flexible AC Transmission Systems) devices, mainly those connected in series with the line [5]. These devices increase power handling capacity of the line and improve transient stability as well as limiting fault currents. Many papers have studied the FACTS for fault current limiting (FCL) mode. These papers have applied different methods for this purpose [6], [7]. But FACTS devices have some constraints for applying in fault current limiting (FCL) mode, which include:

- High cost resulting from device complexity and component requirements [8];
- High magnitudes of fault currents passing through their converters make the FACTS devices bypass themselves for protecting.

Recently a new concept from the family of distributed FACTS, (D-FACTS) has been introduced as a way to remove these barriers. Distributed nature of the suggested systems makes it possible to have fine granularity in the system rating [9].

The distributed static series compensator (DSSC) uses a low-power single-phase inverter which attaches to the transmission conductor and dynamically controls the impedance of the transmission line, allowing control of active power flow on the line [10]. Also the DSSC concept overcomes limitations of the FACTS devices mentioned above. Small rated (10KVA) single phase inverter and a single turn transformer (SST), suggests that the DSSC would be possible to realize extremely low cost [11]. Single turn transformer is the key factor for DSSC in tolerating high fault currents. It uses the transmission line conductor as a secondary winding and is designed with a high turn ratio that reduces the current handled by the inverter. This means that, there is no need to bypassing for protecting itself from high fault currents in inverter side. In this paper, DSSC is utilized for fault current limiting based on impedance control. In disturbances, the DSSC injects voltage in series with the line which can be emulated as a reactance, increases the line reactance and fault current limitation is achieved.

Static synchronous compensator (STATCOM) is a well-known member of FACTS family, which is connected in shunt with the system, resembles in many respects, a rotating synchronous condenser used for voltage control and reactive power compensation. From the power system dynamic stability view point, the STATCOM provides good damping characteristics as it is able to transiently exchange active power with the system. While the primary purpose of STATCOM is to support the bus voltage by injecting (or absorbing) reactive power, an additional strategy can be used with the STATCOM to limit the fault current. It consists of utilizing the STATCOM in such a way to force the voltage at the point where its converter connected, to reduce its magnitude. It is observed that, with this implementation, the total reduction of the short circuit current can be improved.

This paper consists of four sections. First the DSSC concept and its operation in power systems for power flow control, is investigated in part 2. In the third part, the principle of fault current limitation based on voltage at the fault point is presented. Principle of the STATCOM and its application for fault current limitation is included in part 4. Simulation results investigated in the section five consists of the DSSC and the STATCOM fault current limiting mode. Contraction of voltage

dip caused by fault is investigated in simulation results. Also it is verified that, with DSSC in action, the voltage dip is contracted. Conclusion covered at the last section.

2. Distributed Static Series Compensator (DSSC)

2.a DSSC Structure

DSSC is in fact a single-phase model of a SSSC, but in a smaller size, that lies on transmission lines in a distributed manner mainly for power flow control. Each DSSC device is a single-phase, but is deployed on all three phases of a transmission line to preserve symmetry of the power flow. Each module is suspended from the line conductor or is configured as a replacement for the conductor support clamp on an insulator. So, there is no need for phase-ground insulation in contrast to Static Synchronous Series Compensator (SSSC) [12]. The low-power intrinsic of DSSC necessitates installation of hundreds or thousands DSSC modules in a single transmission line.

Fig.1 illustrates DSSC module components in a circuit schematic representation [10]. It mainly consists of a current transformer (CT) to provide the feedback signal required, a processing unit serving as the controller, a small-rated (1-20 kVA) single-phase inverter to generate the compensating sinusoidal voltage, a single-turn transformer (STT) to insert the voltage in the transmission line, a power supply feeding the processor, and a built-in communication hardware to send/receive signals to/from other modules or a centralized controller [13]. DC capacitor holds the voltage level at the DC bus of inverter and power losses of the inverter are compensated through the active power absorbed from the line. Harmonic content of the generated voltage are cleansing by an LC filter connected to output of the inverter. The module is bypassed during the sleep mode of DSSC, or in the event of any failure. The required system commands for responding to gradual changes are received from a central control center via a wireless link or power line communication (PLC) technique [14]. An autonomous operating mode could also be considered in which each module works based on a predetermined set points. The STT utilizes the transmission line conductor as the secondary winding and is designed with a high turn ratio (100:1). Hence, the current which is handled by the inverter is reduced and commercial IGBTs can readily be employed for low cost implementations [11]. As depicted in Fig. 1, the transformer core consists of two parts that are clamped around the line conductor in order to form a complete magnetic circuit [15].

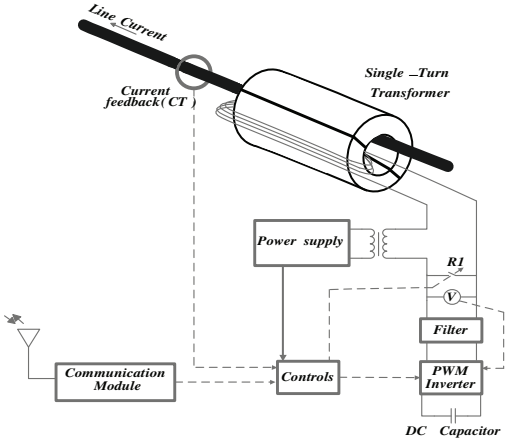

Fig. 1. Circuit schematic of a DSSC module.

2.b Control System

The main task of the DSSC is to control the power flow in a transmission line. This objective can be achieved either by direct control in which both the angular position and the magnitude of the output voltage are controlled, or by indirect control in which only the angular position of the output voltage is controlled and the magnitude remains proportional to the dc terminal voltage [16].

The inverters which are controlled in a direct mode encounter with more difficulty and higher cost to implement in comparison with indirectly controlled inverters. Also in a direct control mode the inverter function is usually associated with some drawbacks in terms of increased losses, greater circuit complexity and increased harmonic content in the output, hence the control structure used for the DSSC in this model is based on indirect control. Fig.2 shows an indirect control schematic of a DSSC module [17].

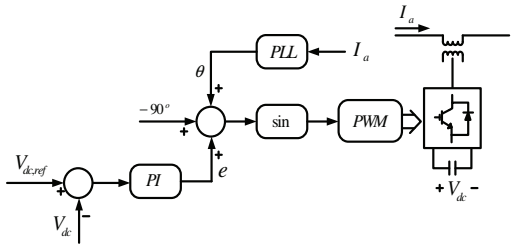

Fig.2 indirect control of DSSC

Here, the controller is used to retain the charge on the dc bus capacitor and to inject a synchronous voltage that is orthogonal to the line current. In order to control the dc capacitor voltage a small displacement 'e' beyond the required 90 degree between the injected voltage and the line current is required as a control signal. The phase-locked-loop (PLL) is used to provide the basic synchronization signal 'θ', which is the phase angle of the line current. The error signal that is obtained by comparing V_{dc} with $V_{dc\,ref}$ is passed through a PI controller and the resultant will be the required phase angle displacement 'e' [10].

3. Fault current limitation analysis

Fig.3 shows a power system where lots of DSSCs are established on transmission line. This power system is implemented for current limitation analysis.

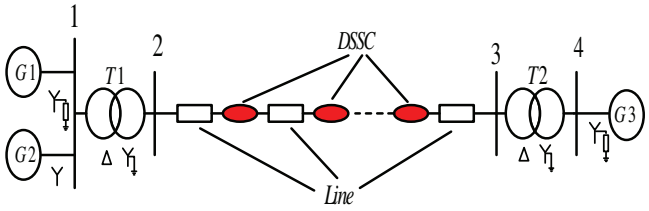

Fig.3 simple power system for fault current limitation analysis

Fig.4 shows the single line diagram of Fig.3. In this figure, ZR is the equivalent impedance of transformer T1 and ZL is the equivalent impedance of line and transformer T2 and V_{se} is the equivalent injected voltage of DSSCs.

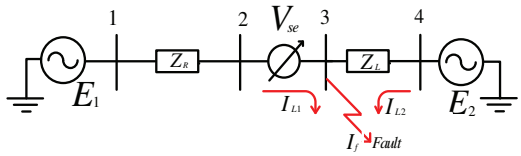

Fig.4 single line diagram of proposed power system

Regarding the fault point considered in Fig.4, which can be located at any point along transmission line, the first equation can be expressed as:

$$[E'_1] = [E_1] + [V_{se}] \quad (1)$$

The line current before the fault is given by:

$$[I_L] = [Z_L + Z_R]^{-1} [E'_1 - E_2] \quad (2)$$

So, the voltage at bus 3 before the fault can be expressed as:

$$[V_3] = [E_2] + [Z_R] [I_L] \quad (3)$$

By substituting (2) in (3) and calling M the matrix that represents the voltage divider, yields:

$$[V_3] = ([I] - [M]) [E_2] + [E_1] [M] + [V_{se}] [M] \quad (4)$$

Where, [I] represent the identity matrix, and [M] is expressed as:

$$[M] = [Z_L + Z_R]^{-1} [Z_R] \quad (5)$$

For subtracting the effect of DSSC on fault current, from E_1 , E_2, these two terms will be named as V_{uf}. Whereas V_{uf} is uncompensated fault voltage and V_{se} is the DSSCs compensating voltage at the fault point (bus 3). So the compensated voltage V_3 becomes V_f :

$$[V_f] = [V_{uf}] + [M] [V_{se}] \quad (6)$$

The compensation term [M] [V_{se}] should be in opposition to V_{uf} for diminishing V_3 , and also V_{se} should be at maximum amplitude during the fault period.

The equations above are applicable on three-phase faults, but for phase-to-ground faults another limitation should be considered. The effect of healthy phases should be clarified to observe whether the coupling effect of unaffected phases can contribute or not to the fault current limitation. For simplification the analysis the resulting impedance matrix in (5) is expressed as:

$$[M] = \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \quad (7)$$

Which factors α, β are dependent on the impedances Z_L, Z_R, and zero and positive sequence values that describe coupling effect between phases. By substituting (7) in (6), yields:

$$\begin{bmatrix} \bar{V}_{fa} \\ \bar{V}_{fb} \\ \bar{V}_{fc} \end{bmatrix} = \begin{bmatrix} \bar{V}_{ufa} \\ \bar{V}_{ufb} \\ \bar{V}_{ufc} \end{bmatrix} + \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \begin{bmatrix} \bar{V}_{sea} \\ \bar{V}_{seb} \\ \bar{V}_{sec} \end{bmatrix} \quad (8)$$

And from (8) it is observed that:

$$\bar{V}_{fa} = \bar{V}_{ufa} + \alpha \bar{V}_{sea} + \beta (\bar{V}_{seb} + \bar{V}_{sec}) \quad (9)$$

The best condition for voltage compensation is attained when $\bar{V}_{sea} = \bar{V}_{seb} = \bar{V}_{sec}$ and $\bar{V}_{fa} = \bar{V}_{ufa} + (\alpha+2\beta)\bar{V}_{sea}$. By choosing $\bar{V}_{sea}$ in opposite position with $\bar{V}_{ufa}$, the $\bar{V}_{fa}$ would be minimum. So the fault current will be greatly diminished.

4. Description of STATCOM structure

The basic STATCOM's structure is presented in Fig.5. The STATCOM is a power electronic based synchronous voltage generator (SVG), that generates a three-phase voltage in synchronism with the transmission line voltage from a DC capacitor. It is connected to the transmission line by a coupling transformer. By controlling the output voltage magnitude of the STATCOM, the reactive power exchanges between STATCOM and the transmission system. The STATCOM is based on the principle that regulates voltage at its terminal with handling the amount of reactive power injected to or absorbed from the power system. When system voltage is low, it generates reactive power (capacitive mode) and in a similar way, if the system voltage is high, it absorbs reactive power (inductive mode). The voltage source converter (VSC) which is connected on secondary side of a coupling transformer contributes to perform the variations of the reactive power. The VSC uses forced-commutated power electronic devices (GTOs, IGBTs or IGCTs) to synthesize a voltage from a DC voltage source.

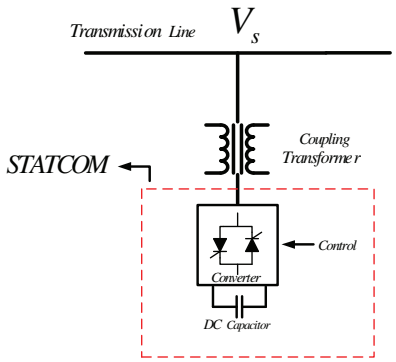

Fig.5 Basic diagram of STATCOM

4.a STATCOM Control

In order to control the power electronic switches, sinusoidal pulse width modulation (SPWM) is utilized. This strategy is used to synthesize a sinusoidal wave form proportional in magnitude to the modulation gain (k) and shifted bye the phase angle α. The advantage of pulse width modulation is that, both parameters k and α can be independently controlled. As the phase angle of the voltage on converter side is changed with respect to the phase angle of AC system voltage, the STATCOM will attempt to generate or absorb active power form the AC system. The exchanged active power will charge or discharge the internal DC capacitors.

The primary control targets of a STATCOM are to control the AC line voltage (Vs) and the DC capacitor voltage (V_{dc}). The AC voltage control is achieved by filtering out the second harmonic and the low frequencies of the AC voltage and then a lead-lag and PI controller are applied to the voltage error in order to attain the modulation phase shift α. The DC capacitor voltage error is put through a PI controller to provide the modulation index gain k. Fig.6 shows the control block of the STATCOM. The STATCOM's data expressed as: Rated Power

= 100MVA, Rated Voltage = 26 KV, Frequency = 60 Hz, XT(sh) = 0.1 p.u

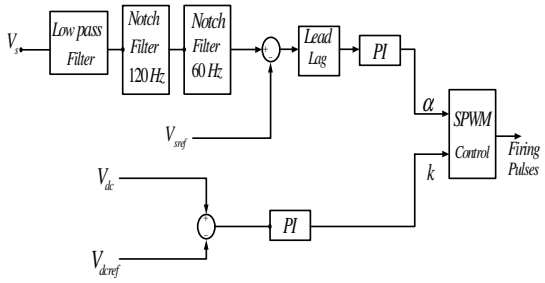

Fig.6 Block control of STATCOM

4.b STATCOM Implementation for Fault Current Limiting

While the primary purpose of STATCOM is to support the bus voltage by injecting (or absorbing) reactive power, an additional strategy can be used with the STATCOM to limit the fault current. It consists of utilizing the STATCOM in such way to force the voltage, at the point where its converter connected, to reduce its magnitude. It is observed that, with this implementation, the total reduction of the short circuit current can be improved. If STATCOM connect to bus 3 in Fig.4 which fault occurs on, with decreasing the bus voltage in fault duration, fault current can be decreased significantly as it is shown in equation (9). The first term of equation (9) can adjusted with STATCOM implementation for fault limiting mode.

5. Simulation Results

The new concept of DSSC in fault current limiting mode mentioned above is applied to 12 bus power system shown in Fig.7. The current limiting effect is evaluated following digital simulation studies in time domain complementary with PSCAD/EMTDC simulations.

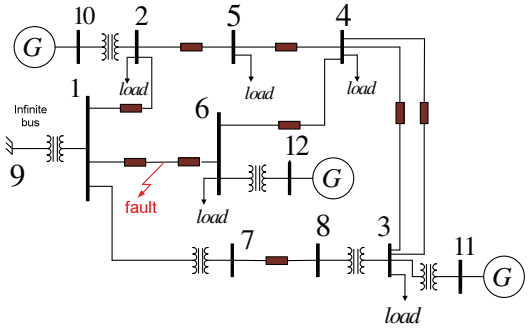

Fig.7. 12 bus system for analyzing fault current limiting

Table I shows the power system constants which are used in time domain simulations. It should be noted that, the PI-sections are used for modeling the transmission lines. Specification of DSSC model is shown in Table II.

Table I. Power system constants

Generators	
H:inertia constant	1.7 s
D:Mechanical damping	0.01 pu
Vbase:Rated RMS phase voltage	22 KV
Ibase:Rated RMS phase current	18.3 KA
VT:Terminal voltage magnitude at t=0	1.01 pu
Pheta:Terminal voltage phase at t=0	0.17 rad
Xd:Direct-Axis Reactance	1.5 pu
X'd: Direct-Axis Transient reactance	0.4 pu
X''d: Direct-Axis sub-transient reactance	0.35 pu
Xq:Quad-Axis reactance	1.2 pu
X''q: Quad-Axis Sub-transient reactance	0.29 pu
Ra=Armature Resistance	0.002 pu
AGFC:Air Gap Factor	1
Transmission lines	
Rated voltage L-L	230 KV
MVA for all phases	250
Line length:(2-5),(4-5),(4-6)	300 Km
Line length:(1-2),(3-4)	100 Km
Line length:(7-8)	600 km
Specification of load	
Load on bus 2	280+j200
Load on bus 3	320+j240
Load on bus 4	320+j80
Load on bus 5	100-j20
Transformers	
1000MVA, 22/230Kv, DY, X_L=0.01p.u ,60Hz, Ideal transformer	Bus10-2 Bus12-6 Bus11-3 Bus 1-9
1000MVA, 230/345Kv, YY, X_L=0.01p.u ,60Hz, Ideal transformer	Bus 9-7 Bus 3-8

Table II.Specification of DSSC

Transformer	1/75
Inverters (single phase PWM inverter)	Power Rating:10 MVA Power devices: IGBT PWM carrier frequency: 12 kHz
Capacity of DC side	2.1 mF
Filter	
Cut-off frequency	375 Hz
L	1.8 mH
C	200 μF

In order to analyze the outcome of current limiting, the DSSC is controlled for compensating reactance of transmission line in normal operation for power flow control. A single-phase to ground fault occurs on phase A of line 1-6 at time 10 sec and lasts for 1 sec. The fault location is 200Km farther than bus 6. It is assumed that, DSSCs are off and they link to power system at 10.05 sec. For simplicity, pre-charged capacitors are considered. This assumption is reasonable, because in real, DSSCs are in operation and they change the mode of operation in faults, so there is no time needed for charge of each DSSC during fault.

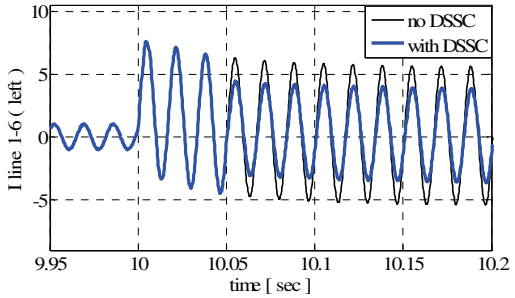

Fig.8 the line 1-6 currents before and after the fault on 10 sec

Fig.8 shows the fault current at the left-hand side of the fault before and after implementation of DSSCs. It is presumed that, during the fault just the left-hand side's DSSCs are in operation, and they are in inductive mode. For better view, the DSSCs begin to operate at time 10.05sec. It is observed from Fig.8 that, the limitation of current is improved up to 1.8p.u. The fault current which has amplitude of 6p.u in 10.05sec decreases to 4.2p.u when DSSC is implemented for limiting the fault current.

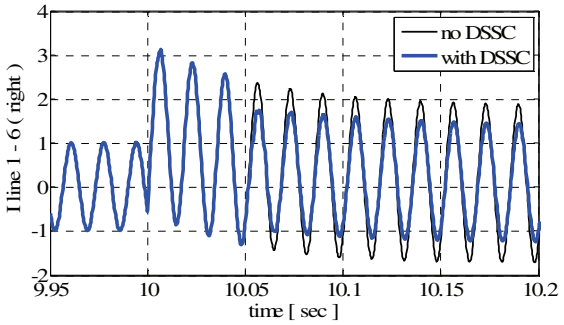

Fig.9 current on line 1-6 during fault with DSSC

Fig.9 exhibits the currents at the right-hand side of the fault occurrence. It is clear that, this current is lower than left-hand side current, because the generator reactance diminishes this current. Also the line reactance of right-hand side is greater than left-hand side because fault occurs on 200km farther on bus 6. So the right-hand side is larger than left-hand side and has more reactance. Fig.9 reveals that, with operation of DSSCs on the right-hand side of the fault, the fault current will be significantly decreased. Now consider a STATCOM is implemented on bus 6 for controlling of its voltage. When fault occurs, its reference voltage decreases from 1p.u to 0.8p.u to limit the fault current. The signal for changing the reference value of STATCOM comes from over current relay, so a little time delay for receiving the signal form relay and dynamic response of STATCOM controller should be taken into account. Fig.10 shows the bus voltage of STATCOM (bus6) during its operation. STATCOM is in operation at time 6.5 sec and fault occurs at time 10 sec. STATCOM operation at 6.5 sec leads to transient state at the bus voltage, but after a short span of time, the STATCOM fixes the bus voltage at 1p.u. when fault occurs, the reference value of STATCOM adjusted to 0.8p.u in order to limit the right-hand side fault current. The right-hand side fault current with implementation of STATCOM is shown in Fig.11. It should be noted that, only DSSCs in the right-hand side of the fault are in operation and they are operating in inductive mode.

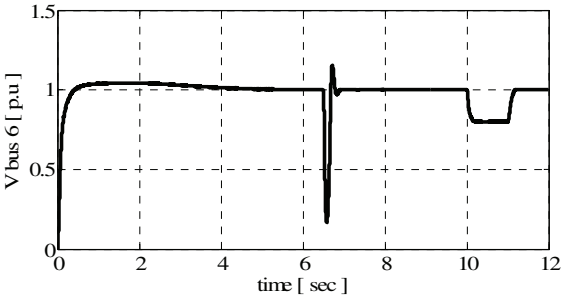

Fig.10 voltage of bus 6 during simulation

. It is observed from Fig.11 that, the fault current decreases significantly from 2p.u to 1.1p.u. It is a go0d characteristic of both DSSC and STATCOM in power system that they can not only do their operation (power flow control by DSSC and voltage control and dynamic stability by STATCOM) in power system, but also with a little change in their operations, they can limit the fault currents. It should be noted that, in this case, DSSCs are in line at time 10.05sec.

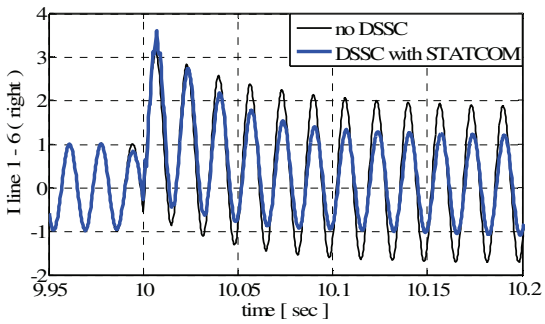

Fig.11 the current limitation with STATCOM and DSSCs

Contraction of range of Instantaneous voltage drop by Fault Current Limiting of DSSC

The main cause for an instantaneous voltage drop is a fault like a stroke of lightning. The fault position is regional and distributed unequally. The possibility of voltage drop caused by a fault in a distance is increases if the power system is integrated. By installing a fault current limiter near the point where the fault rate is high, the instantaneous voltage drops in the entire power system can reduce. This is because of a fault current limit is equivalent to lengthening the electrical distance between faults, making faults remote.

Fig.12 shows the RMS value of generator terminal voltage at bus 12. For simplicity, just phase A is shown. It is observed from Fig.12 that, in a presence of DSSC, the voltage on bus12 improved up to 0.08p.u during fault occurrence.

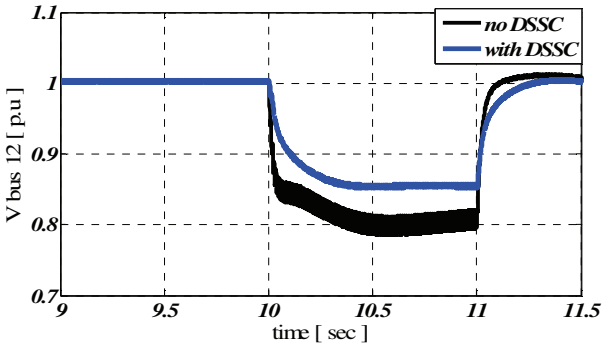

Fig.12 contraction of voltage dips on bus12

Fig.13 shows the voltage dip during fault on bus 11 of power system. In presence of DSSC the voltage dip on terminal voltage of generator on bus 11 is not significantly improved. It is acceptable because the DSSCs are compensating the line 1-6 reactance, and the distance between line1-6 and bus 12 is 600Km. The long line has large reactance that the compensation with DSSC has no significant effect on its voltage.

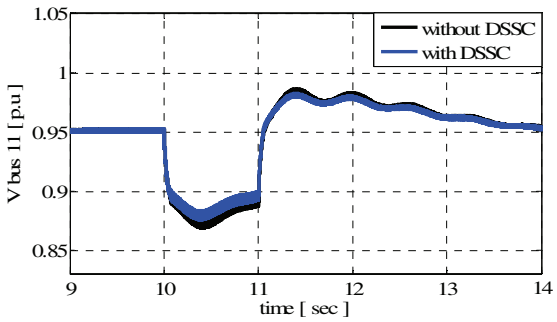

Fig.13 voltage dips during fault on bus 11with DSSC in line1-6

In this case of study because of long distance between different buses, improvements of voltage dips on the other buses like bus 3 or bus 10 in presence of DSSC in line 1-6 is not significant. The long transmission lines have large reactance that the DSSC on line 1-6 cannot alter the reactance of farther lines considerably. But DSSC is a cost-effective device and can distribute along the transmission lines. If the large number of DSSCs connected to the transmission lines, the contraction of voltage dips caused by faults can improve significantly. If the large number of DSSCs connected to the different transmission lines, the contraction of voltage dips caused by faults can improve significantly that is our undergoing investigation that not included in this paper.

6. Conclusion

This paper focuses on a basis of manipulating the series voltage injected by DSSC in order to limit the fault currents drawn by the power system. The analysis was focused on single-phase-to-ground fault on the transmission lines and could be effectively extended to other types of faults. It has been shown that, the STATCOM can also contribute to limit the fault currents by decreasing its reference voltage in fault duration. Implementation of both DSSC and STATCOM results good effect on fault current limitation process. Contraction of voltage dip occurs on system buses during fault period are greatly achieved by inserting DSSCs operate in inductive mode on disturbed lines. Implementation of DSSC in whole system not only improves overall stability and capacity of power system, but also can contracts together voltage dips and fault currents in power system. If DSSCs in the power system are operating in capacitive mode and a fault occurs on the power system, all the DSSCs on the power system should switch to inductive mode. This would limit the fault current and contract the voltage dip on entire system.

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