# New Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources

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## Abstract

**This paper presents a novel topology for cascaded multilevel inverters. The proposed topology employs less number of components. This structure consists of a single DC voltage source, several low-frequency transformers and switching devices. There are two switching devices in each module of the proposed structure and there is only a module with three power switches. However, in conventional cascaded H-bridge multilevel inverters four switches are used in each module. The number of gate drivers are reduced respectively along with the switches which results in smaller size, lower cost, lower power consumption in driving circuits and higher efficiency. To verify the performance of the proposed structure, Simulation results carried out by PSCAD/EMTDC and a low-power experimental setup was used to test the converter in practice.**

## 1. Introduction

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources [1]. The commutation of the power switches aggregates these multiple DC sources in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected. Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations [2].

Multilevel converters can be divided into four remarkable topologies: diode-clamped multilevel converter (DCMC) [3], flying capacitors multilevel converter (FCMC) [4], P2 Multilevel converter (P2MC) [5] and cascaded multilevel converter (CMC) with separate DC sources [6]. Compared to m-level DCMC, FCMC, and P2MC, which use $m$-1 capacitors on the dc bus, the CMC uses only ($m$-1)/2 capacitors for the same $m$-level output voltage. Clamping diodes are not required for FCMC, P2MC and CMC. In overall P2MC undeniably require too many components as compared to other multilevel converters so it is not suitable for higher voltage levels [7]. However, comparing CMC with DCMC, FCMC and P2MC, it requires minimum number of components and its dominant advantage is the circuit layout with flexibility. But a primary disadvantage of the CMC is that it requires a separate DC source for each H-Bridge module, which yields significant cost [8].

Another clear disadvantage of multilevel power conversion is the great number of power semiconductor switches needed. Although low-voltage-rated switches can be utilized in a multilevel converter, each switch requires a related gate driver and protection circuits. This may lead the overall system to be more expensive and complex [9]. Therefore, in practical implementation, reduction of the number of switches and gate driver circuits is very important. Many topologies of multilevel inverters using a reduced number of switches and gate-driver circuits are presented in recent years [10–12].

In this paper a new topology for cascaded transformer H-Bridge multilevel inverter is presented which employs one DC voltage source and several isolated single-phase low-frequency transformers. There are two switches in each module except the last module which consists of three switching devices. Using fewer switching devices respectively, fewer gate drivers result in smaller implementation size and lower cost. To verify the validity of the proposed multilevel inverter, simulation and experimental results are provided.

## 2. Conventional Cascaded Multilevel Inverters

The circuit configuration of a cascaded H-bridge multilevel inverter is depicted in Fig. 1. As it is shown in Fig. 1, there are four H-bridge modules in this structure. Therefore, nine-level output voltage can be synthesized. Each H-bridge module can generate three voltage levels positive, negative and zero according to its different switching states. The outputs of H-bridge modules are series connected in order to generate a stepwise output voltage. The main disadvantage of this structure is that each H-bridge module requires independent DC voltage sources.

Fig. 2 shows the cascaded transformer H-bridge multilevel inverter which only requires a single DC voltage source. Each H-bridge module is connected to a low-frequency transformer. The secondary sides of the transformers are series connected to synthesize the stepwise output voltage.

In both structures shown in Fig. 1, 2, four switches are employed in each H-bridge module. Respectively, four gate driver circuits are required in each H-bridge module. However, the number of components used in these structures could be reduced which result in lower implementation cost, smaller size, higher efficiency and simplicity of the structure.

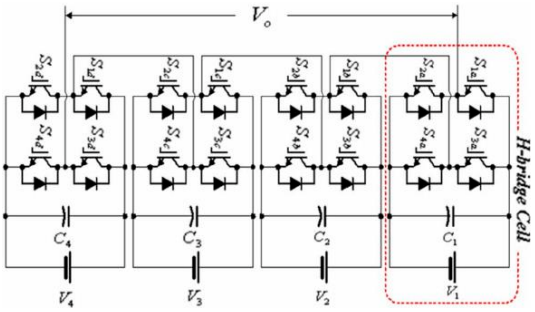


**Fig. 1.** Cascaded H-bridge multilevel inverter

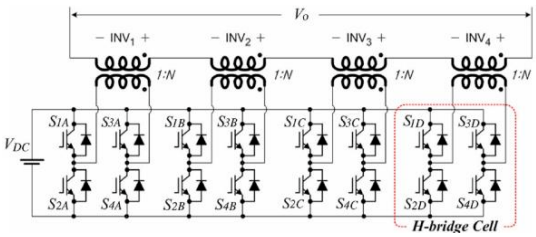


**Fig. 2.** Cascaded transformer H-bridge multilevel inverter

## 3. Proposed Multilevel Inverter

Among multilevel inverter structures, cascaded H-bridge inverters have the advantage of being modular. It is easily expandable for higher output voltage levels. Therefore, the output voltage resembles to sinusoidal waveform as the number of modules increases. Higher number of H-bridge modules requires excessive number of semiconductor switches and other components which increases the size and the cost of the circuit.

The proposed structure is shown in Fig. 3. The proposed structure consists of a single DC voltage source, several low-frequency transformers and fewer number of switching components in comparison to conventional multilevel inverters. As it is shown in Fig. 3, each module comprises of two switching components except the last module which includes two typical switches and one bidirectional switch. Each module is connected to a transformer. Secondary sides of the transformers are series connected to generate the output voltage.

Considering $K$ as the number of transformers in this structure, the number of switching devices can be obtained as follows:

$$SW = 1 + 2K \tag{1}$$

Where $SW$ is the number of switches. Assuming $m$ as the number of output voltage level, the number of switches with respect to the output voltage level is given as follows:

$$SW = m \tag{2}$$

The output voltage can be obtained as follows:

$$V_{output} = V_{o1} + V_{o2} + \cdots + V_{ok} \tag{3}$$

If all turn-ratios of transformers in Fig. 3 are equal then the inverter is known as uniform step symmetric multilevel inverter.

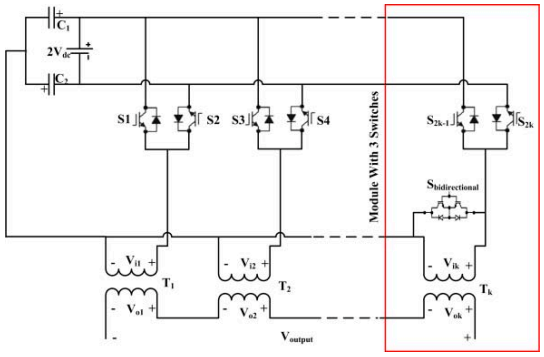


**Fig. 3.** Circuit configuration of the proposed inverter

### 3.1. Operation of Proposed Inverter

To demonstrate the operation of the proposed inverter, a nine-level configuration, which is shown in Fig. 4, is used. As it is shown in Fig. 4, the structure consists of four transformers, eight unidirectional switches and a bidirectional switch. There are also four modules in this structure. Each module can generate two voltage levels positive ($+V_{dc}$) and negative ($-V_{dc}$) except the last module with three switches which can create three voltage levels positive ($+V_{dc}$), zero, negative ($-V_{dc}$). Therefore, the zero voltage level can only be generated by the last module with three switching devices. The maximum output voltage level can be generated from this structure is $+4V_{dc}$.

Table 1 shows the switching pattern of the inverter shown in Fig. 4 for different output voltage levels. It is worth noting that various switching states are possible for the same voltage level. For instance, to generate the output voltage of the $+V_{dc}$, switches $S_1$, $S_3$, $S_6$ and $S_{bidirectional}$ are turned on. It is also possible to obtain the same output voltage by turning on the switches $S_1$, $S_4$, $S_5$ and $S_{bidirectional}$.

There are several modulation strategies for multilevel inverters and operation of them depends on modulation strategies [13 – 15]. The modulation methods used in multilevel inverters can be categorized according to switching frequency. In this paper, the fundamental frequency switching technique has been employed. It is important to note that the calculation of optimal switching angles for different purposes such as elimination of the selected harmonics and minimizing THD are not the objective of this paper.

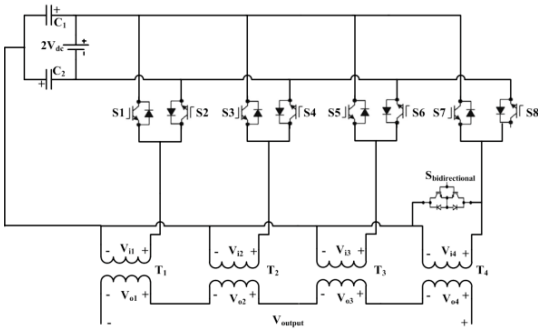


**Fig. 4.** Circuit configuration of nine-level inverter

**Table 1.** Output voltage for various states of switches

| Output Voltage Level | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S bidirectional |
|---|---|---|---|---|---|---|---|---|---|
| +4Vdc | On | Off | On | Off | On | Off | On | Off | Off |
| +3Vdc | On | Off | On | Off | On | Off | Off | Off | On |
| +2Vdc | On | Off | On | Off | On | Off | Off | On | Off |
| +Vdc | On | Off | On | Off | Off | On | Off | Off | On |
| 0 | On | Off | On | Off | Off | On | Off | On | Off |
| -Vdc | Off | On | Off | On | On | Off | Off | Off | On |
| -2Vdc | Off | On | Off | On | Off | On | On | Off | Off |
| -3Vdc | Off | On | Off | On | Off | On | Off | Off | On |
| -4Vdc | Off | On | Off | On | Off | On | Off | On | Off |

### 3.2. Voltage and Current Ratings of the Switches

There are two important criteria for selecting the proper switching devices peak inverse voltage (PIV) and current rating. Considering the input DC voltage 2 per unit (P.u), the PIV of the all switches are 2 P.u except the bidirectional switch which has the PIV of 1 P.u. The PIV of the all switches can be calculated as follows:

$$PIV_{Total} = 2m - 1 \tag{3}$$

Assuming the load current 1 P.u, the current ratings of all the switches are 1 P.u.

In comparison with the conventional cascaded H-bridge inverter, the PIV of the switches in the proposed inverter is higher.

### 3.3. Comparison Study

The present paper aims to reduce the number of components used in multilevel inverter. There is only a single DC source used in this structure. The number of switching devices required to realize an *m*-level output voltage in conventional cascaded H-bridge inverters is as follows:

$$SW = 2m - 2 \tag{4}$$

The numbers of switches in the proposed structure are compared with the cascaded H-bridge multilevel inverter in Fig. 5. As it is shown in Fig. 5, the proposed structure requires fewer switching components. Each switching device requires a gate driver to operate. Therefore, reduction in the number of switching devices also results in fewer number of gate drivers which leads to a smaller size and lower cost of the implementation.

The number of on switches is also an important criterion to compare the structures. There are two on switches in each module of the conventional H-bridge inverter. However, the number of on switches in each module of the proposed inverter is one. More number of on switches means more voltage drop on these switches. The number of on switches for an *m*-level output voltage in conventional cascaded H-bridge inverter can be calculated as follows:

$$N_{on} = m - 1 \tag{5}$$

The number of on switches in the proposed structure can be given as follows:

$$N_{on} = \frac{m-1}{2} \tag{6}$$

Where *m* is the number of output voltage levels.

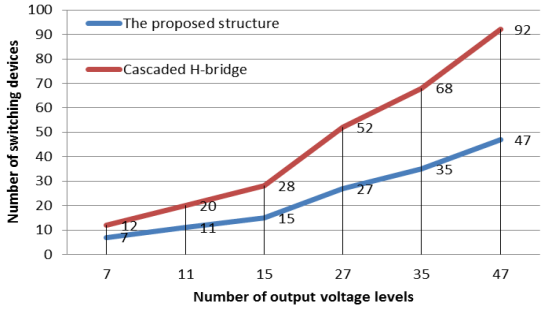


**Fig. 5.** Comparison of switches to realize m-level voltages

## 4. Simulation and Experimental Results

The simulation results are carried out by PSCAD/EMTDC with consideration of an R-L load (R=50 Ω , L=0.5 mH)for a nine-level structure shown in Fig. 4. In this simulation, input voltage is equal ($V_{dc}$=20 V) and the turn-ratios of transformers are chosen as 1:1. Fig. 6 -8 show waveforms of output voltage ($v_{out}$) of the modules 1-3 , respectively and as shown in these figures , the transformer output voltage of each module for all times has negative or positive values. Fig. 9 illustrates , the transformer voltage of fourth module and it has negative, positive or zero values. In this proposed multilevel inverter, fourth module uses bidirectional switch for generating the zero voltage level.

The secondary sides of the transformers are series connected in order to create a stepwise output voltage. Consequently, as shown in Fig. 10, the final output voltage becomes the sum of the terminal voltage of all modules also Fig. 11 shows load current. The output voltage has a waveform close to a sinusoidal waveform, 50 Hz voltage with amplitude 40 V. in Fig. 12 the frequency spectrum of output voltage is illustrated, the THD of the output voltage is found as 10.41%.

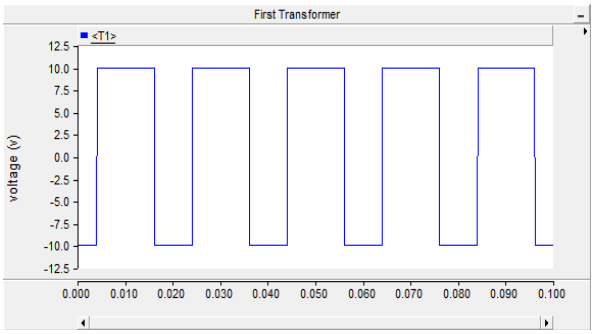


**Fig. 6.** Output voltage of transformer $T_1$

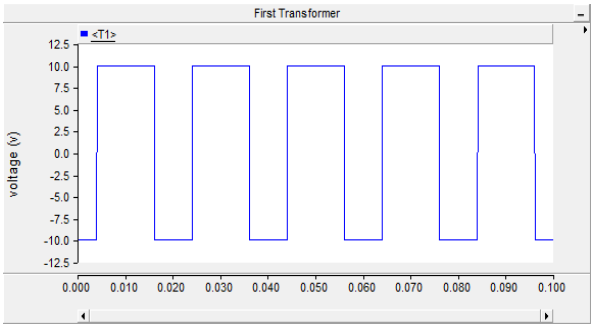


**Fig. 7.** Output voltage of transformer $T_2$

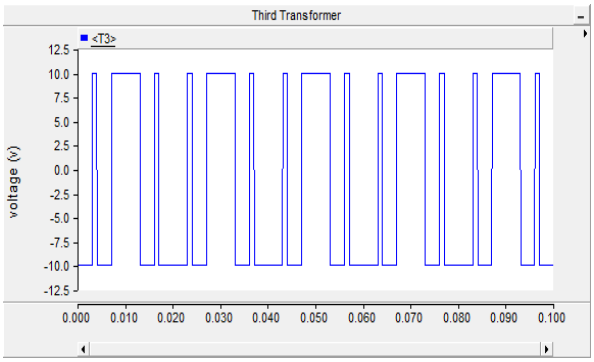


**Fig. 8.** Output voltage of transformer $T_3$

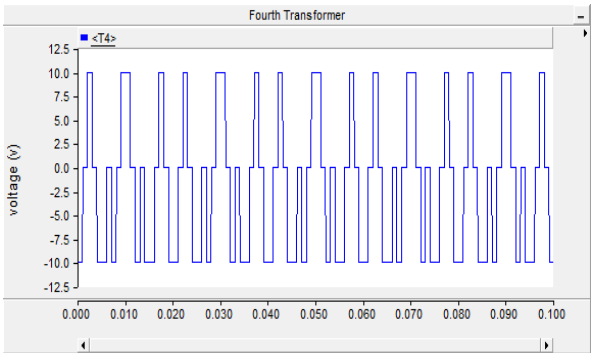


**Fig. 9.** Output voltage of transformer $T_4$

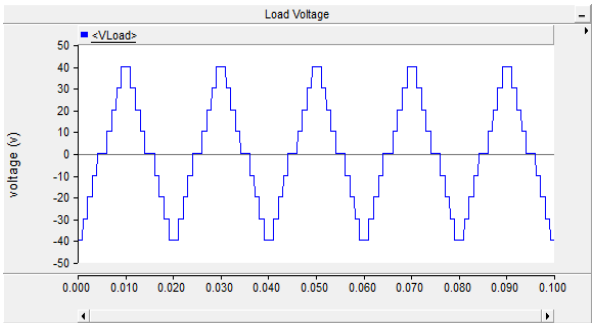


**Fig. 10.** Stepwise output voltage ($V_{dc}$=20 v)

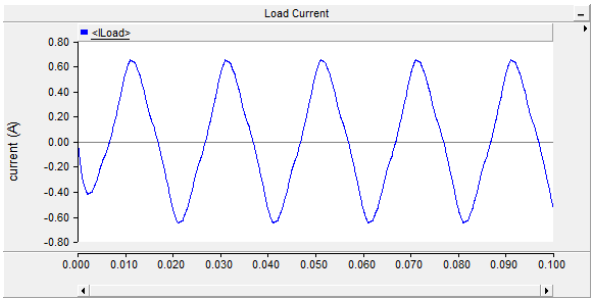


**Fig. 11.** Load current

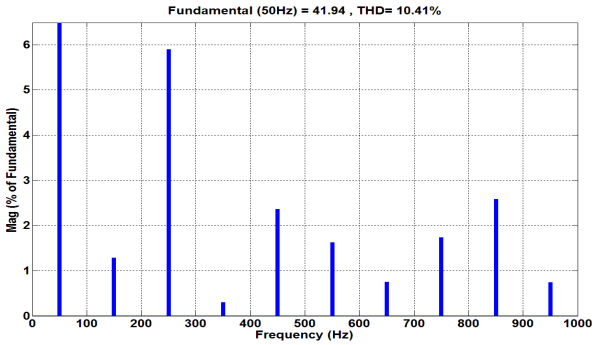


**Fig. 12.** Frequency spectrum of output voltage

To verify the performance of the proposed inverter experimentally, a prototype has been built in the laboratory scale. In order to validate the proposed concept, the inverter of was constructed and tested in the 9-level mode. To get 9 output voltage levels of the inverter, the ratio of transformers are set to 1:1. The DC sources were supplied by a battery sources that has a voltage of 50V. This multilevel generates staircase waveform with maximum 100 V and 50Hz. The common MOSFET with internal anti-parallel diodes has been used in prototype. For every module, only two switches are used with a single-phase transformer. In module 4 a bidirectional switch is applied. The MOSFETs are the types IRFP460 with voltage and current ratings equal to 500V and 10 A, respectively. The ATMEGA32-8PT microcontroller by ATMEL Company has been used to generate the switching patterns and the opt coupler TLP521-1 is used to drive switches.

Fig. 13 shows the output voltage of proposed inverter. As it can be seen, the results verify the ability of proposed inverter in generation of desired output voltage. Consequently, we can say that the proposed topology is more advantageous in switch and DC voltage source cost compared with the conventional cascaded multilevel inverter because the proposed topology can reduce the number of switches and DC voltage sources.

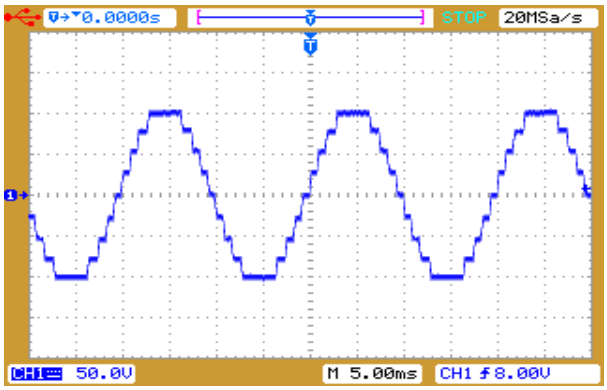


**Fig. 13.** Measured output voltage ($V_{dc}$=50 v)

## 5. Conclusions

In this paper, a novel topology for cascaded multilevel inverters is presented. The proposed structure benefits from the advantage of fewer numbers of components. The number of switching devices as well as the number of gate drivers is reduced in the proposed topology. Therefore, the size and the cost of implementation are decreased. To validate the proper operation of the proposed structure, simulation and experimental results are provided.

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