A Novel High Gain-Bandwidth Product and Low Power Band-Pass Preamplifier using Active Inductor

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Abstract

In this paper, a low power differential preamplifier, which amplifies the input voltage and regenerates the desired output, is presented. The preamplifier can be implemented in 0.18 µm CMOS, with 1.8 V supply voltage. By using a novel structure, a high gain, high bandwidth and low power preamplifier is obtained. To increase the bandwidth, an active inductor is designed. In order to increase the gain, crossover transistors pairs are used. In addition, the parameters of the circuit are tuned to obtain high gain in a high frequency range. Therefore, this circuit is employed as a band-pass preamplifier. By using the results of simulation with HSPICE software, the gain, gain-bandwidth product and power consumption are 41.8 dB, 12 GHz and 1.39 mW, respectively.

1. Introduction

Preamplifier stage reinforces the input signal for the next stage to improve the input sensitivity of the next stage. For example in a comparator, with an increase in the minimum input signal, the comparator can make better decisions. In addition, by using a preamplifier stage, input next stages are insulated from the noise variations which are obtained from feedback stage that is called kickback noise [1]. In general, three types of available amplifier is introduced; two stages, folded cascode and cascode. Among them, cascode structure has less power consumption [2], [3]. However, this structure has low output swing. In addition, it has a limited bandwidth. Some techniques, like adding inductors, can be used in cascode structure to increase the bandwidth [4], [5]. In [6] a cascode differential amplifier is presented. In this circuit, by adding a feedback network, the transconductances of transistors are increased. Therefore, the feedback network is caused to decrease time constant in fundamental output nodes and increase the bandwidth. However, several inductors are used to design the circuit which causes a large chip area. In addition, the obtained dc gain of this circuit is not high enough. Shunt-peaking technique is an excellent method to extension the preamplifiers bandwidth [7]. In this technique, with an inductor in series with a resistor load, the bandwidth of circuit is increased by nearly 80%. Since the inductors occupy large chip area, the active inductors can be employed [8]. In [9] a fully differential preamplifier is designed, take advantage of active inductors to increase the bandwidth. The equivalent inductor and resistance of the active inductor are tuned to obtain high bandwidth. However, this circuit has a low dc gain.

In this paper a new preamplifier circuit with a high gain bandwidth product is developed. The proposed preamplifier is a band-pass circuit with a high dc gain in a high frequency range. Therefore, this circuit is suitable for high speed applications. By using the proper design of the circuit parameters, the locations of zero and poles are adjusted to obtain high gain and high bandwidth. Thus, the proposed preamplifier has a greater characteristic in comparison with the other preamplifiers. In section (2), the main idea of the proposed preamplifier circuit is described. In section (3), a comparison between different preamplifier is accomplished and considered simulations are presented. Conclusions are expressed in section (4).

2. Proposed preamplifier

A simple differential preamplifier is shown in Fig. 1(a) [1]. In this circuit, input voltage is considered as pulses. This voltage is reinforced, and desirable output voltage which is suitable for the first stage of circuits, is provided. This circuit has a dominant pole at the output node:

$$s_p = \frac{-1}{R_o.C_p} \tag{1}$$

Where, C_p is the parasitic capacitance and R_o is the output equivalent resistance at the output node. According to Eq. 1, both R_o and C_p, are small quantities, so the dominant pole is located at high frequencies and a high bandwidth is obtained. However, since the output resistance R_o is a small value, gain is small. Initially, the circuit which is shown in Fig. 1(b), is designed in [10] to resolve this tradeoff.

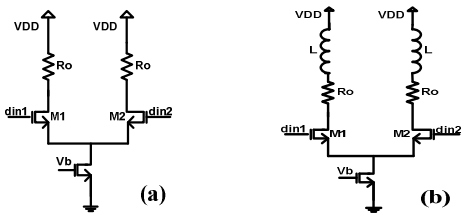

Fig. 1. (a) Conventional preamplifier [1] (b) Preamplifier circuit with spiral inductor [10]

The gain is equal to [10]:

$$A_{v-dc} = g_{m1}R_o \tag{2}$$

$$A_v = g_{m1}[(R_o + sL) \| \frac{1}{C_P s}] = \frac{g_{m1}(R_o + sL)}{C_P L s^2 + R_o C_P s + 1} \tag{3}$$

Relations of zero and poles circuit are given below:

$$S_Z = \frac{-R_o}{L} \tag{4}$$

$$S_{P1} = \frac{R_o}{2L}\left[-1+\sqrt{1-\frac{4L}{C_P {R_o}^2}}\right],\ S_{P2} = \frac{R_o}{2L}\left[-1-\sqrt{1-\frac{4L}{C_P {R_o}^2}}\right] \tag{5}$$

This circuit has two poles and one zero. If the value of L and R_o parameters are chosen properly, then S_Z and S_{P1} will be equal to zero. The value of zero neutralize the small pole. Therefore, the second pole, that located at higher frequencies, remains and causes to increase the bandwidth. But in the above circuit, inductor will occupy a lot of places in circuit. An active inductor [8], which is shown in Fig. 2 can be used to solve the above problem.

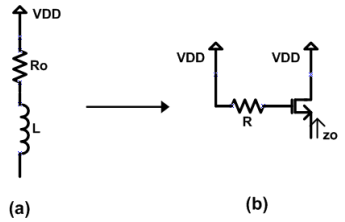

Fig. 2. Active inductor load [8]

The equivalent resistance of this circuit can be obtained as indicated in Eq. 6 [8];

$$Z_o = \frac{S(C_{gd} + C_{gs}) + \frac{1}{R}}{S^2 C_{gd} C_{gs} + S(\frac{C_{gs}}{R} + C_{gd} g_m) + \frac{g_m}{R}} \tag{6}$$

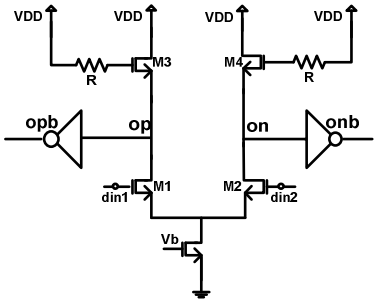

Fig. 3. Preamplifier circuit with active inductor load [9]

Preamplifier circuit with active inductor load [9], is shown in Fig. 3. The values of gain, zero and poles of this circuit, are obtained as follows;

$$A_v = g_{m1}(Z_o \| \frac{1}{C_P S}) = \frac{g_{m1} Z_o}{Z_o C_P S + 1} \tag{7}$$

$$S_{Z1} = \frac{-1}{R(C_{gd4} + C_{gs4})} \tag{8}$$

$$S_{P1} = \frac{(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} + \frac{C_P}{R})}{2(C_{gd4}.C_{gs4} + C_P(C_{gd4} + C_{gs4}))} \times(-1 + \sqrt{1 - \frac{4g_{m4}(C_{gd4}.C_{gs4} + C_P(C_{gd4} + C_{gs4}))}{R(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} + \frac{C_P}{R})^2}}) \tag{9}$$

$$S_{P2} = \frac{(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} + \frac{C_P}{R})}{2(C_{gd4}.C_{gs4} + C_P(C_{gd4} + C_{gs4}))} \times(-1 - \sqrt{1 - \frac{4g_{m4}(C_{gd4}.C_{gs4} + C_P(C_{gd4} + C_{gs4}))}{R(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} + \frac{C_P}{R})^2}}) \tag{10}$$

According to the places of zero and poles, the value of gain in each frequency is obtained as follows [11];

Gain = BW × (distance to the zero)

/((distance to one pole) × (distance to other pole)) (11)

Where, BW is -3dB bandwidth. According to the above equation, to increase the gain, the zero must be occurred at very low frequency. The value of zero neutralize the small pole. The second pole that located at higher frequencies, remains and causes to increase the bandwidth. In this condition, the gain and bandwidth are increased and the proposed preamplifier with high gain in high frequency range is designed.

By take the limit as R approaches infinity, S_Z and S_{P1} will be equal to zero. Therefore, S_{P1} can be compensated with S_Z, and bandwidth will be increased as compared to the previous circuits. In Fig. 3, the circuit gain in Dc mode is obtained as follows;

$$A_v = \frac{g_{m1}}{g_{m4}} \tag{12}$$

The gain value is not sufficiently large. However, by using crossover transistors pairs M_{1L} and M_{2L} as shown in Fig. 4, the gain will be increased and obtained as follows;

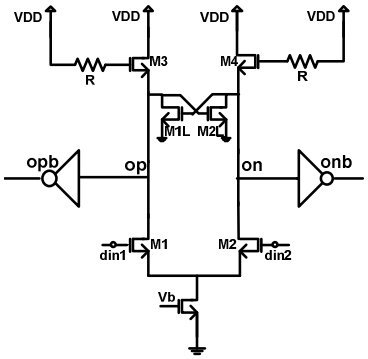

Fig. 4. Preamplifier circuit with crossover transistor for enhancement of gain

$$A_V = g_{m1}(Z_O \| \frac{1}{C_p S} \| \frac{-1}{g_{m2L}}) \tag{13}$$

Relations of zero and poles of this circuit are given below;

$$S_{Z1} = \frac{-1}{R(C_{gd4} + C_{gs4})} \tag{14}$$

$$S_{p1} = \frac{(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} - g_{m2L}(C_{gd4} + C_{gs4}) + \frac{C_p}{R})}{2(C_{gd4}.C_{gs4} + C_p(C_{gd4} + C_{gs4}))} \times (-1 + \sqrt{1 - \frac{4(\frac{g_{m4}}{R} - \frac{g_{m2L}}{R})(C_{gd4}.C_{gs4} + C_p(C_{gd4} + C_{gs4}))}{((\frac{C_{gs4}}{R} + C_{gd4}) - g_{m2L}(C_{gd4} + C_{gs4}) + \frac{C_p}{R})^2}}) \tag{15}$$

$$S_{p2} = \frac{(\frac{C_{gs4}}{R} + C_{gd4}.g_{m4} - g_{m2L}(C_{gd4} + C_{gs4}) + \frac{C_p}{R})}{2(C_{gd4}.C_{gs4} + C_p(C_{gd4} + C_{gs4}))} \times (-1 - \sqrt{1 - \frac{4(\frac{g_{m4}}{R} - \frac{g_{m2L}}{R})(C_{gd4}.C_{gs4} + C_p(C_{gd4} + C_{gs4}))}{((\frac{C_{gs4}}{R} + C_{gd4}) - g_{m1L}(C_{gd4} + C_{gs4}) + \frac{C_p}{R})^2}}) \tag{16}$$

By take the limit as R approaches infinity, S_z and S_{p1} will be equal to zero. Therefore, S_{P1} can be compensated with S_Z. It means that, the gain and bandwidth are increased. The value of Dc gain is obtained as follows;

$$A_V = \frac{g_{m1}}{g_{m4} - g_{m2L}} \tag{17}$$

It can be seen that the dc gain of this circuit is increased compared to the previous circuit. If the size of M_4 and M_{2L} (M_3 and M_{1L}) are chosen to be almost equal, then the values of g_{m4} and g_{m2L} (g_{m3} and g_{m1L}) will be equal and the value of gain will increase extremely. For stability consideration, the value of $g_{m3,4}$ must be a little smaller than gmL.

However, utilizing a great resistance at a GΩ range is not reasonable in circuit design. Crossover transistors M_5, M_6, M_7 and M_8 are used to solve the above problem, which are shown in Fig. 5. The size of transistors is adjusted to obtain infinite resistance value. The differential output signal (op and on) is coupling to the opp and onn nodes through the gate-source capacitances of M_3 and M_4. Therefore, the value of equivalent resistance in opp node (or onn node) is given below;

$$R_{eq(opp,onn)} = (\frac{1}{g_{m7,8}} \| \frac{-1}{g_{m5,6}}) = (\frac{1}{g_{m7,8} - g_{m5,6}}) \tag{18}$$

The size of $M_{7,8}$ and $M_{5,6}$ are chosen to be almost equal, then the values of $g_{m7,8}$ and $g_{m5,6}$ will be equaled and $R_{eq(opp,onn)}$ will be obtained as infinity. However, to ensure the stability, the value of $g_{m7,8}$ must be a little larger than the value of $g_{m5,6}$. In all of the above circuits and relations, V_b is the bias voltage and its value is 1V and C_p is the parasitic capacitance at the output node. The values of transistors aspect ratio are given in table 1.

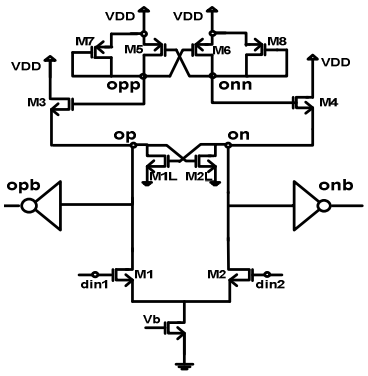

Fig. 5. Proposed preamplifier

Table 1. The values of transistors aspect ratio

Transistor	W/L (μm/μm)
M_1 , M_2	50/0.18
M_3 , M_4	2/0.18
M_5 – M6	3/0.18
M7-M8	3.2/0.18
M_9	50/0.18
M_{1L} , M_{2L}	3/0.18

3. Simulation results

The proposed preamplifier circuit is simulated based on TSMS 0.18 μm CMOS process model using HSPICE. The simulation results of the proposed circuit (Fig. 5) are shown in Fig. 6(a). Therefore, this circuit is a band-pass preamplifier. The high gain is 41.8 dB. The value of unit gain bandwidth is obtained as 12 GHz. A comparison between the proposed circuit and present circuits in Figs. 1(a) and 3 [1,9] is shown in Fig. 6(b). In Fig. 1(a), the high bandwidth is obtained, but the gain is low. Fig. 3 is designed using a large value of R which is equal to 10000MΩ that is unprofitable in circuits. Therefore, the high bandwidth and low gain are obtained. In proposed circuit, the transistors of M_{1L} and M_{2L} are added to increase the gain. In addition, the crossover transistors pairs of M_5, M_6, M_7 and M_8 are employed to replace the large R. Thus, a high gain and high bandwidth preamplifier is created. In Fig. 7(a) input waveform is changed from 0 to 0.6 V (din1,din2). As can be seen the output is changed from 0 to 1.8 V (opb,onb). The output waveform delay time is 0.24ns that is less than quarter of period in 1 GHz working frequency. In Fig. 7(b), the differential outputs in opp and onn nodes that are coupled due to the gate-source capacitances of M_3 and M_4 transistors, are illustrated. A comparison between different preamplifiers is performed in Table 2. In this table, gain-bandwidth product is given to accomplish a fair comparison. The performance of preamplifier is improved by increasing this quantity. In the proposed preamplifier this value is almost improved while the power consumption of the circuit is minimum and the gain is maximum.

Jitter histogram and eye diagram at 1 GHz working frequency are illustrated in Figs. 8(a), 8(b). These figures

demonstrate about 1.27 ps and 4.34 ps RMS and peak-to-peak jitters, respectively. The input noise is a combination of flicker and thermal noises in the operational amplifier [12], which are given below to proposed preamplifier, respectively:

$$\overline{V^2_{n,in,\frac{1}{f}}} = \frac{2K_N}{Cox(wL)_{1,2}} \cdot \frac{1}{f} + \frac{2K_N}{Cox(wL)_{3,4}} \cdot \frac{1}{f} \frac{g_{m3,4}{}^2}{g_{m1,2}{}^2} + \frac{2K_N}{Cox(wL)_{1L,2L}} \cdot \frac{1}{f} \frac{g_{m1L,2L}{}^2}{g_{m1,2}{}^2} \quad (19)$$

$$\overline{V^2_{n,in,th}} = 4KT\gamma\left[\frac{2}{g_{m1,2}} + \frac{2g_{m3,4}}{g_{m1,2}{}^2} + \frac{2g_{m1L,2L}}{g_{m1,2}{}^2}\right] \quad (20)$$

Where, K is the Boltzmann constant, K_N and K_P are the flicker noises coefficients of NMOS and PMOS, respectively, that it is less for PMOS compared to that for NMOS, Cox, f, γ, T, L and W are the gate oxide capacitor, frequency, the thermal noise coefficient which depends on the effective mobility and channel length modulation, temperature in Kelvin, the length and width of each transistor, respectively [12].

In proposed preamplifier, $g_{m1,2}$ is higher than $g_{m3,4}$, $g_{m1L,2L}$, $g_{m5,6}$ and $g_{m7,8}$. In addition, $W_{1,2}$ has a large value. Therefore, the flicker and thermal noises are minimized. The input noise of proposed preamplifier is shown in Fig. 9. Therefore, this preamplifier has a low noise in all of the frequency range.

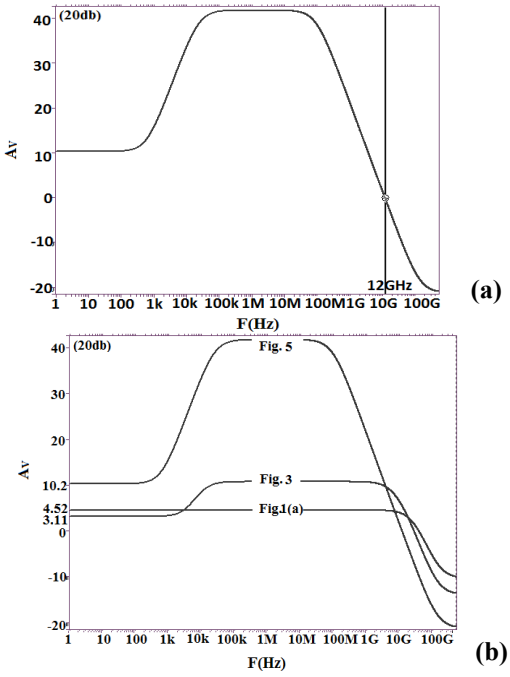

Fig. 6. (a) Proposed circuit as a band-pass preamplifier (b) Comparison of frequency response at mentioned circuits

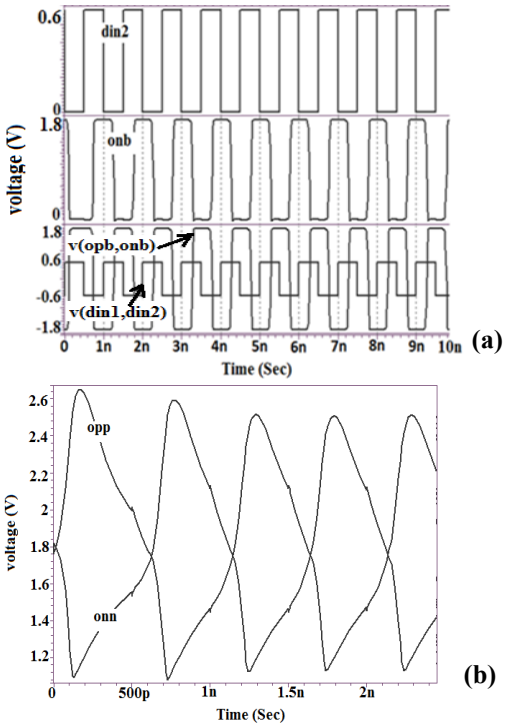

Fig. 7. By din1 and din2 in input nodes (a) Simulated transient response (simulation results with piecewise waveform) (b) Output differential voltage in output nodes of opp and onn

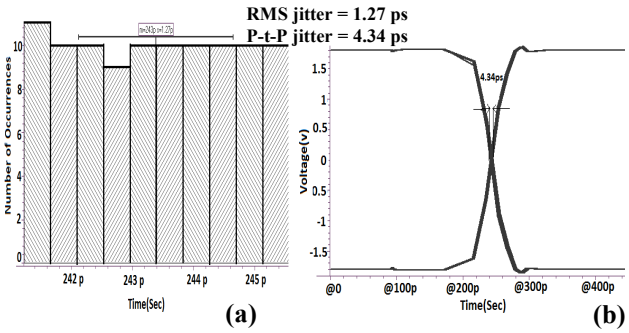

Fig. 8. (a) Output jitter histogram at 1 GHz (b) Output jitter eye diagram at 1 GHz

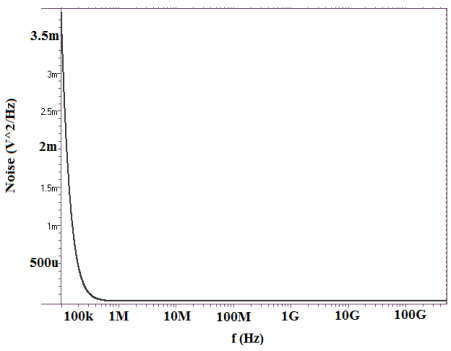

Fig. 9. Input noise diagram

4. Conclusions

In this article a low-power, high gain and bandwidth preamplifier at the 0.18 µm CMOS technology is presented. The results show that the maximum gain, gain-bandwidth product and power consumption are 41.8 dB, 12 GHz and 1.39 mW, respectively. In this circuit the high gain is obtained in high frequency range. This preamplifier can be expressed as one of the high-bandwidth preamplifier and is suitable for the first stage demodulators. The RMS and peak-to-peak jitters of this preamplifier at 1 GHz are 1.27 and 4.34 ps respectively.

5. References

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Table 2. The comparison between different preamplifiers

Preamplifier	Characters of Preamplifiers						
	Supply voltage	Technology	Gain	Bandwidth (-3db)	Gain× Bandwidth	power	Single-ended (SE) or Differential (Diff.)
Proposed	1.8 V	0.18µm	41.8 dB	95 MHz	12 GHz	1.39 mW	Diff
[6]	2.5 V	0.18µm	11 dB	19 GHz	24 GHz	113 mW	Diff
[13]	1.8 V	0.18 µm	24.3 dB	40-1200MHz	4.1 GHz	14.4 mW	SE
[14]	1.2 V	65 nm	10 dB	30-36 GHz	44 GHz	20-68.1 mW	SE