VOLTAGE TO FREQUENCY CONVERTER WITH PHASE MODULATION POSSIBILITY

Milan STORK

e-mail: stork@kae.zcu.cz
University of West Bohemia, Faculty of Electrical Engineering, Department of Applied Electronics, 30614 Plzen, Czech Republic

Keywords: Voltage to frequency converter, fractional phase locked loop, sigma delta converter

ABSTRACT

Voltage to frequency converter (VFC) is an oscillator whose frequency is linearly proportional to control voltage. In this paper, the New Synchronous Voltage to Frequency Converter (NSVFC) or "sigma delta" (Σ-Δ) voltage to frequency converter is described. This NSVFC works similarly as conventional SVFC but it has a better frequency spectral property then other SVFC and therefore it is possible to used in fractional phase locked loop (PLL). More over, the NSVFC has a phase modulation possibility. A experimental NSVFC was constructed and simulated to verify operation of the converter. Analysis and prototype of NSVFC is described.

I. INTRODUCTION

The VFC have become quite popular due to their low cost and application versatility in variety of electronic control and measurement systems. With a good quality VFC, this circuit will match the performance of many commercial A/D converters. Its only disadvantage is relatively slow conversion time. Σ-Δ modulator [1] can be used for synchronous VFC (SVFC). In SVFC charge balance pulse length is now defined by two successive edges of the external clock. The block diagram of the Σ-Δ VFC is shown on Fig. 1. If this clock has low jitter the charge will be defined very accurately. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and they have excellent temperature stability [2], but is not pure tone for constant input voltage (output pulses are not equally spaced). Fig. 2 c) shows the waveforms of Σ-Δ SVFC. From Fig. 2 c) can be seen that output periods are not the same, but they have changed between 3 and 4 clock cycles. This disadvantage was taken away in NSVFC1 and NSVFC2.

II. NEW SYNCHRONOUS VFC

In Fig. 3 is NSVFC1 block diagram. Only one-shot is added and connected to comparator output. Fig. 2 shows waveforms of this NSVFC1. Number of pulses is same for usual Σ-Δ SVFC [2] and NSVFC (NSVFC1 and NSVFC2). The output frequency f_O is given by (1):

$$f_O = f_{CLK} (1 - V_i / V_R) / 2 \qquad \text{[Hz, V]} \qquad (1)$$

where V_i is input voltage, V_R is reference voltage and f_{CLK} is clock frequency. It is important to note, that for NSVFC1 this equation is limited for V_{imin} given by (2). The minimal input voltage value V_{imin} (for NSVFC1):

$$V_{imin} > 2 f_{CLK} V_R t_{dC} \qquad \text{[V, Hz, sec]} \qquad (2)$$

where t_{dC} is comparator time delay. E.g. for $f_{CLK} = 10$ *kHz*, $V_R = 5$ *V* and $t_{dC} = 200$ *ns,* the minimal value $V_{imin} > 0.02$ *V.*

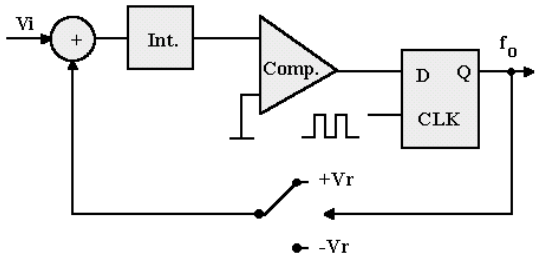

Figure 1. Conventional Σ-Δ voltage to frequency converter (SVFC). Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, D - flip flop.

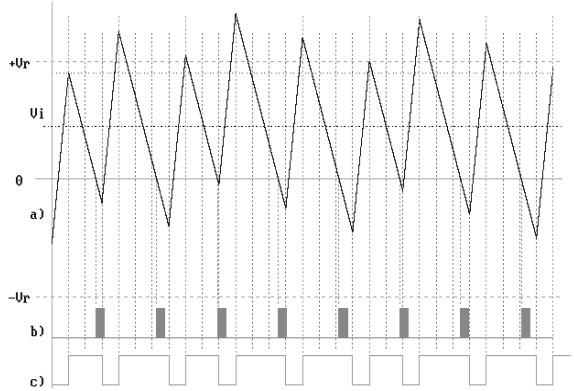

Figure 2. Waveforms of SVFC (a, c) and NSVFC (a, b, c). a) integrator - output voltage, b) one shot output, c) D-flip flop output. $V_i = 1.8$ V, $V_R = 4$ V, period of one shot is $3.636\ T_{clk}$

III. NSVFC OUTPUT FREQUENCY EVALUATION

The key to Σ-Δ modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the integrator is feed to 1-bit analog/digital converter (ADC). This is simply a comparator with its reference input at a level of half the input range, 0 V in this case. The ADC output feeds a 1-bit digital/analog converter (DAC) which has output levels equal $+V_R$ or $-V_R$. A summing amplifier completes the loop by summing the current input signal and the previous sample DAC output. The aim of the feedback loop is to try to maintain the average output change of the integrator at the comparator reference level, 0 V. Therefore:

$$const + \sum_{k=1}^{\infty} V_{o1}(k) + \sum_{k=1}^{\infty} V_{o2}(k) = 0 \qquad (3)$$

where $k = 1, 2, \ldots \infty$, *const* is voltage depending on starting conditions and $V_{o1}(k)$ and $V_{o2}(k)$ are integrator output voltage in k output frequency period, see Fig. 4. The NSVFC and equivalent period time diagram is shown on Fig. 5.

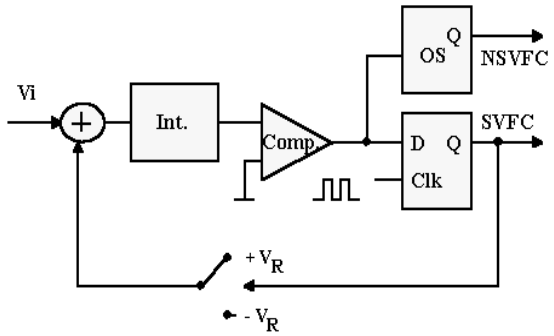

Figure 3. NSVFC1 - New Σ-Δ voltage to frequency converter type1. Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, D - flip flop, OS - one shot.

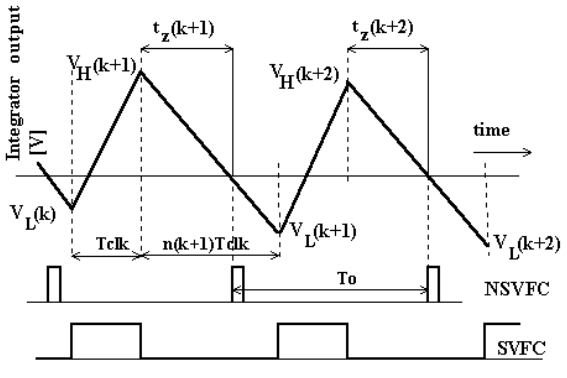

Figure 4. Time diagram for ideal converter - output frequency evaluation

Change ΔV_a is given by (4):

$$\Delta V_a = C \int_0^{T_{clk}} (V_i(t) + V_R)dt \qquad (4)$$

and ΔV_b is given by (5):

$$\Delta V_b = C \int_0^{nT_{clk}} (V_i(t) - V_R)dt \qquad (5)$$

where C is the integrator constant. The integrator output is given by:

$$V_{o2}(k) = V_{o1}(k) + C \int_{T_{clk}}^{(n+1)T_{clk}} (V_i(t) - V_R)dt \qquad (6)$$

$$V_{o1}(k) = V_{o2}(k-1) + C \int_0^{T_{clk}} (V_i(t) + V_R)dt \qquad (7)$$

and for $V_i(t) = V_i$ (constant input voltage):

$$V_{o1}(k) = V_{o2}(k\text{-}1) + C(V_i + V_R)T_{clk} \qquad (8)$$

$$V_{o2}(k) = V_{o1}(k) + C(V_i - V_R)nT_{clk} \qquad (9)$$

Integrator output voltage change is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)nT_{clk} \qquad (10)$$

where n must be an integer for SVFC. For NSVFC output is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)mT_{clk} \qquad (11)$$

where m is real for NSVFC. From (11) $(V_R > V_i)$:

$$m = \frac{V_i + V_R}{V_R - V_i} \qquad (12)$$

and for SVFC, n is given by (13):

$$n = ceil\left(\frac{V_i + V_R}{V_R - V_i}\right) = ceil(m) \qquad (13)$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9.01/3) =4.

IV. OUTPUT FREQUENCY EVALUATION FOR IDEAL NSVFC

For this ideal NSVFC it is supposed, that comparator has a zero time delay and noise value voltage on second comparator input is zero. Output period for NSVFC can be determined from Fig. 4. It is supposed, that $V_R > V_i$, where V_R is reference voltage and V_i is input voltage. The $V_L(i)$ and $V_H(i)$ are voltage at integrator output.

Output period T_0 from Fig. 6 is given by:

$$T_0 = T_{clk}\,[n(k+1) - t_z(k+1) + 1 + t_z(k+2)] \qquad (14)$$

Time from $V_L(i)$ to $V_H(i+1)$ is always $1*T_{clk}$ if no error occurs (error can be caused by comparator delay, comparator hysteresis or voltage change on second comparator input. This will discuss in next part). For $T_{clk} = 1$, the output period ${}^1T_0$:

$$ {}^1T_0 = n(k+1) - t_z(k+1) + 1 + t_z(k+2) \quad (15) $$

Strait line from $V_L(i)$ to $V_H(i+1)$ has a slope: $V_i + V_R$
The line is given by equation (all following equations are given for $T_{clk} = 1$):

$$ V_H(k+1) = V_L(k) + (V_i + V_R).1 \quad (16) $$

The line slope from $V_H(i)$ to $V_L(i+1)$ is: $V_R - V_i$. Line equation is:

$$ V_L(k+1) = V_H(k+1) - (V_R - V_i)\, n(k+1) \quad (17) $$

where $n(k+1)$ is given by:

$$ n(k+1) = ceil(V_H(k+1)/(V_R - V_i)) = $$
$$ ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \quad (18) $$

hence

$$ V_L(k+1) = V_H(k+1) - (V_R - V_i)\, n(k+1) = $$
$$ V_H(k+1) - (V_R - V_i)\, ceil(V_H(k+1)/(V_R - V_i)) = \quad (19) $$
$$ V_L(k)+V_i+V_R -(V_R -V_i)\, ceil((V_L(k)+V_R +V_i)/(V_R -V_i)) $$

The term $(V_R - V_i)\, ceil((V_L(k) + V_R + V_i)/(V_R - V_i))$ can't be reduced, because $ceil()$ is nonlinear function, e.g.: $y(ceil(x/y)) \neq ceil(x)$.
Time $t_z(k)$ is given by:

$$ t_z(k) = V_H(k)/(V_R - V_i) \quad (20) $$

Output period equation is given by (for $T_{clk} = 1$):

$$ {}^1T_0 = n(k+1) - t_z(k+1) + 1 + t_z(k+2) = $$
$$ ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) - V_H(k+1)/(V_R - V_i) $$
$$ + 1 + V_H(k+2)/(V_R - V_i) \quad (21) $$

After multiplication by term $(V_R - V_i)$, equation (21) is changed to:

$$ (V_R -V_i)\,{}^1T_0 = (V_R -V_i)\, ceil((V_L(k)+ V_R +V_i)/(V_R -V_i)) $$
$$ - (V_L(k) + V_R + V_i)+ V_R -V_i + V_L(k+1) + V_R +V_i \quad (22) $$

$V_L(k+1)$ is substitute by equation (19), hence:

$$ (V_R -V_i)\,{}^1T_0 = (V_R -V_i) ceil((V_L(k) + V_R +V_i)/(V_R -V_i)) $$
$$ -(V_L(k) + V_R +V_i) +2V_R +V_L(k) +V_i +V_R -(V_R -V_i) $$
$$ ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \quad (23) $$

After reduction, output period ${}^1T_0$ is given by:

$$ {}^1T_0 = 2V_R /(V_R - V_i) \quad (24) $$

and output frequency ${}^1f_0$ hence:

$$ {}^1f_0 = (V_R - V_i)/2V_R \quad (25) $$

and for $T_{clk} \neq 1$ the output frequency f_0:

$$ f_0 = f_{clk}\, (V_R - V_i)/2V_R \quad (26) $$

where $f_{clk} = 1/T_{clk}$

From (26) is shown, that ideal NSVFC output frequency is linearly dependent on input voltage (f_{clk} and V_R are constants).

V. OUTPUT FREQUENCY EVALUATION FOR REAL NSVFC

In this part, error caused by comparator delay, comparator hysteresis or voltage change on second comparator input is described. This error is displayed on Fig. 5 and is sign by X point. The error can arise especially when input voltage $V_i \approx 0$. The error occur when 2 clock cycles are need for $V_L(k)$ to $V_H(k+1)$ transition. In this case, this must be detected and additional output pulse is generated, when integrator output voltage on one comparator input is greater than voltage on second comparator input (it is important to note, that in ideal condition, output pulse is generated only when voltage on integrator output is lower then voltage on second comparator input - leading edge of integrator output). The additional logic is used for this purpose. The block diagram of this NSVFC2 is shown in Fig. 6.

Output period T_0 from Fig. 5 is given by:

$$ T_{e1} = T_{clk}\, [n(k) - t_z(k) + t_e(k)] \quad (27) $$

For $T_{clk} = 1$, $V_i << V_R$ output period ${}^1T_{e1}$ is given by:

$$ {}^1T_{e1} = ceil(V_H(k)/(V_R -V_i)) - V_H(k)/(V_R -V_i) $$
$$ + |V_L(k)/(V_R + V_i)| \quad (28) $$

In (28) $ceil(V_H(k)/(V_R - V_i)) = 2$ and $V_H(k) \approx V_R$ and $|V_L(k)| \approx V_R$ for $V_i \approx 0$. Hence:

$$ {}^1T_{e1} = 2 - V_R/(V_R -V_i) + V_R/(V_R +V_i) \approx 2(1 - V_i/V_R) \quad (29) $$

Similarly the output period ${}^1T_{e2}$ is given by:

$$ {}^1T_{e2} = 2 - t_e(k) + V_R/(V_R - V_i) $$
$$ = 2 - V_R/(V_R +V_i) + V_R/(V_R +V_i) \approx 2(1 + V_i/V_R) \quad (30) $$

Equations (29) and (30) for T_{clk} are simplified to:

$$ T_{e1} \approx 2T_{clk}\, (1 - V_i/V_R) \quad (31) $$
$$ T_{e2} \approx 2T_{clk}\, (1 + V_i/V_R) \quad (32) $$

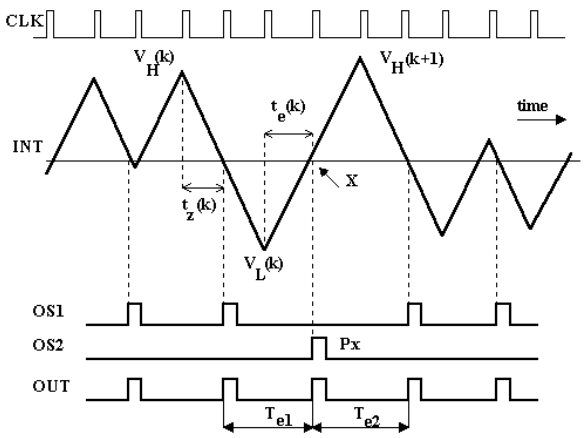

Figure 5. Time diagram for real converter - output frequency evaluation

VI. PHASE MODULATION

The NSVFC2 has phase modulation capabilities. When the modulating voltage V_{PM} is applied to second comparator input, see Fig. 6, the output signal is phase modulated. The $V_{PM} < V_R$ must be satisfied for modulation voltage. The time diagram for phase modulation computing is shown on Fig. 7.
For $T_{clk} = 1$, the output period ${}^1T_{PM}$ is given by (33):

$$ {}^1T_{PM} = n(k+1) - t_z(k+1) + 1 + t_{zPM}(k+2) \quad (33) $$

The equation for $n(k+1)$ and $t_z(k+1)$ are the same as (18) and (20). But $t_{zPM}(k+2)$ is:

$$t_{zPM}(k+2) = (V_H(k+2) - V_{PM})/(V_R - V_i) \quad (34)$$

where V_{PM} is voltage on second comparator input.
After some mathematics manipulation the ${}^1T_{PM}$ is:

$${}^1T_{PM} = (2V_R - V_{PM})/(V_R - V_i)$$

$$= 2V_R/(V_R - V_i) - V_{PM}/(V_R - V_i) = {}^1T_o - \Delta^1T_{PM} \quad (35)$$

hence $\Delta\varphi$ is given by (36):

$$\Delta\varphi = \pi V_{PM}/V_R \quad [\text{rad}, -] \quad (36)$$

From (36) is shown, that NSVFC2 phase change is linearly dependent on input voltage V_{PM}.

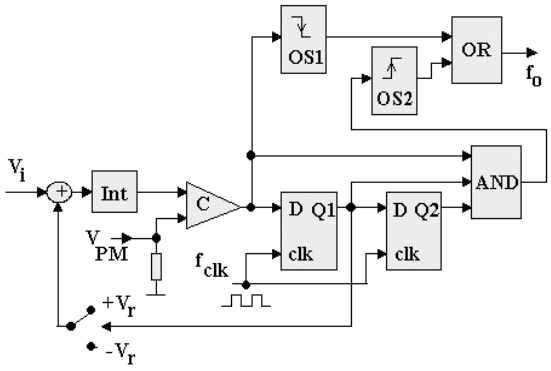

Figure 6. NSVFC2 - Block diagram. Int. - integrator, C - comparator, V_i - input voltage, V_r - reference voltage, V_{PM} - input voltage for phase modulation, D - flip flop, OS - one shot, AND, OR - log. function.

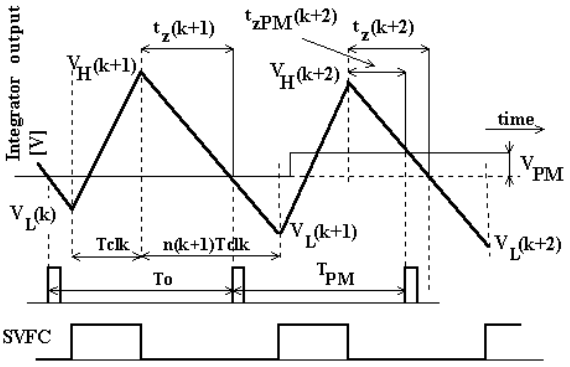

Figure 7. Time diagram for phase modulation evaluation

VII. EXPERIMENTAL RESULTS

Commercially produced SVFC AD7741 and AD7742 [2] were tested and also NSVFC1 was realized and tested [12], [13], [14], [15]. In Fig. 8, experimentally realized NSVFC1 simplified circuit diagram is shown [3]. The voltage/frequency characteristic and frequency spectrum was measured. In common type of SVFC, since the output pulses are synchronized to a clock they are not equally spaced. This need not affect the user of a SVFC for A/D conversion [16], [17], but it does prevent its use as a precision oscillator. Despite this disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC applications. In Fig. 9, the frequency spectrum of SVFC is shown and in Fig. 10, the spectrum of NSVFC1 is displayed. From Fig. 10 can be seen, that spurious spectral lines are rejected.

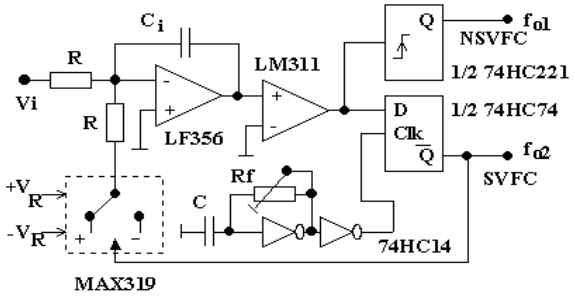

Figure 8. Experimental NSVFC1 simplified circuit diagram.

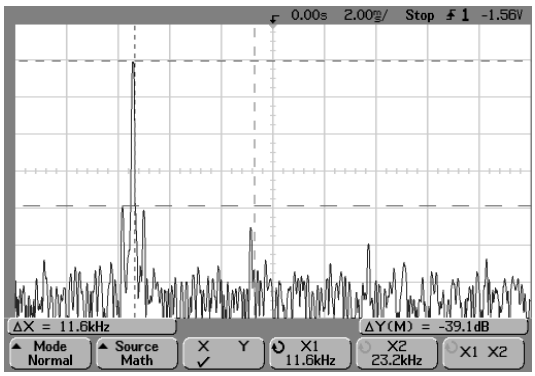

Figure 9. The frequency spectrum of traditional Σ-δ V/f converter

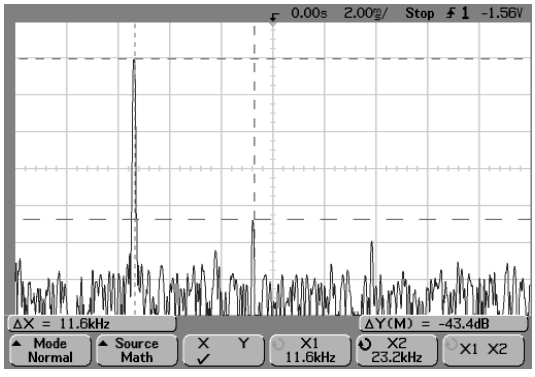

Figure 10. The frequency spectrum of new, modified Σ-δ V/f converter (NSVFC1).

The block diagram of experimental fractional PLL synthesizer is shown in Fig. 11. If the VCO is locked to the reference frequency, then:

$$f_d = f_r \quad (37)$$

where is f_r reference frequency and f_d is frequency on the

output of NSVFC. Because is given by (38):

$$f_d = f_o\,(1 - V_i / V_R)/2 \qquad (38)$$

where f_o is frequency of VCO. After substituting for f_d from (38) into equation (37), frequency of VCO is given by (39):

$$f_o = 2f_r\, 1/(1 - V_i / V_R) \qquad (39)$$

The VCO frequency f_o can be changed according equation (39) by means of changing V_i.

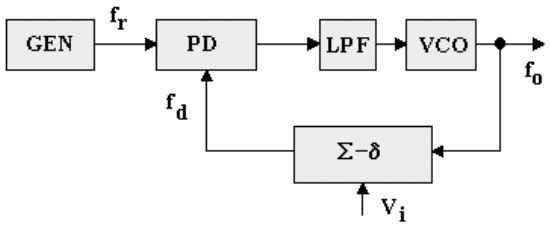

Figure 11. The block diagram of experimental fractional PLL synthesizer with Σ-δ V/f converter (NSVFC) used as fractional divider, f_r - ref. frequency, f_o - output frequency, V_i - control voltage, GEN - generator, PD - phase detector, LPF-lowpass filter, VCO - voltage controlled oscillator .

VIII. CONCLUSION

A very detailed look at the concept of new type sigma-delta voltage to frequency converter circuit has been presented in this article. A prototype system was constructed to verify operation of the converter. Analysis of new type voltage to frequency converter was described. The NSVFC simulation results and measured results were compared. From analysis, simulation and measured results can be seen very good agreement from different point of view. It was pointed out that this new converter has better properties than other synchronous types of VFC. This main disadvantage of SVF described above was removed in new type of NSVFC. Because output pulses are equally spaced in NSVFC (some spurious spectral lines are rejected), this device can be used also as fractional frequency divider.

ACKNOWLEDGMENT

This research work has been supported by New Technologies - Research Center in West Bohemian Region LN00 B084 and partly also by Spezial-Electronic (Maxim IC's).

REFERENCES

1. Sangil Park, Principles of Sigma-Delta Modulation for Analog-to-Digital Converters, Motorola Application Notes APR8, 1999.
2. Single and Multichannel, Synchronous Voltage-to-Frequency Converters, AD7741, AD7742, Analog Devices 1999.
3. Analog Multiplexers/Switches, Maxim 1995 New Releases Data Book, Vol. IV, 1995.
4. B. Gilbert, D. Grant, Applications of the AD537 IC Voltage-to-Frequency Converter, AN277, Analog Devices.
5. W. Jung, Operation and Applications of the AD654 IC Voltage-to-Frequency Converter, AN278, Analog Devices.
6. B. Gilbert, C. Kitchin, K. Weigel, Build Fast VCAs and VCFs with Analog Multipliers, Voltage-to-Frequency Converter, AN309, Analog Devices.
7. S. Martin, Using AD650 Voltage-to-Frequency Converter As a Frequency-to-Voltage Converter, AN279, Analog Devices.
8. W. Jung, J. Riskin, L. Counts, Circuits Ideas for IC Converters, AN343, Analog Devices.
9. J. Bryant, Ask the Applications Engineer-3, V/F Converters, AN361, Analog Devices.
10. P. Klonowski, Analog-to-Digital Conversion Using Voltage-to-Frequency Converters, AN276, Analog Devices.
11. L. Zuch, Voltage to Frequency Converters, Data Acquisition and Conversion Handbook, Datel-Intersil, pp. 199 - 227, 1980.
12. M. Stork, Modified Σ-Δ Voltage to Frequency Converter, 4-th International Conference on Advanced A/D and D/A Conversion Techniques and Their Applications. IMEKO TC-4, Prague, ISBN 80-01-02540-3, pp. 211 - 214, June 2002.
13. M. Stork, New Fractional Phase-Locked Loop Frequency Synthesizer Using a Sigma-Delta Modulator, 14th International Conference on Digital Signal Processing, DSP 2002, Santorini - Greece, ISBN 0-7803-7503-3, Volume 1, pp. 367 - 370, July 2002.
14. M. Stork, New Σ-Δ Voltage to Frequency Converter, The 9th IEEE International Conference on Electronic Circuits and Systems, Proceedings, Dubrovnik, Croatia, ISBN 0-7803-7596-3, Vol. II, pp. 631 - 634, September 2002.
15. M. Stork, Voltage to Frequency Converter, 12th IMEKO TC4 International Symposium, Electrical Measurements and Instrumentation, Zagreb, Croatia, ISBN 953-96093-8-0, Proceedings Part 2, pp. 464 - 467, September 2002.
16. L. Michaeli, J. Saliga, V. Sedlak, An approach to diagnostic of the AD converter embended on ATMEL microcontrollers. Proceedings of 4-th Workschop on ADC Modeling and Testing. Bordeaux, pp. 247-252, 1999.
17. M. Kollar, V. Spany, T. Gabas, Autocompensative System for Measuring of the Capacitances, Radioengineering, June 2002, Vol. 11, No. 2, ISSN 1210-2512, pp. 26-30, 2002.