A HIGH EFFICIENCY ZVZCS FULL BRIDGE CONVERTER FOR MEDIUM POWER LOW INPUT VOLTAGE APPLICATIONS

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ABSTRACT-*A high efficiency, Zero-Voltage and Zero-Current Switching (ZVZCS) PWM Phase-Shifted (PS) Full-Bridge-Converter (FBC) is applied to a medium power (450W/700W) DC/DC converter fed from low input voltage (12V/24V) batteries. In order to decrease the turns ratio of the SMPS transformer, output voltage is obtained by adding the battery voltage to the DC/DC converter output voltage for the 12V battery option, with the additional cost of two MOSFETs. 90% efficiency is obtained at an output voltage of 28VDC and an output current of 16A when the DC/DC converter is fed from 12V batteries. For 24V batteries, an efficiency of 88% is obtained at an output voltage of 28VDC and an output current of 25A.*

I. INTRODUCTION

Phase-Shifted (PS) Zero-Voltage-Switching (ZVS) Full-Bridge-Converters (FBC) have been successfully used in off-line applications [1,2]. The performances of PS-ZVS-FBCs have been discussed in [3,4]. Phase-Shifted Zero-Voltage and Zero-Current Switching (ZVZCS) Full-Bridge-Converter, however, has been introduced in [5] for an off-line application. The main disadvantage of this topology is the power dissipation problem of the saturable core in series with the transformer primary because of bi-directional flux swing. PS-ZVZCS-FBC configuration has been improved in [6] by replacing the saturable core in [5] by two saturable cores in the right-leg which prevents bi-directional flux swing.

For standard PS-ZVS-FBCs used in off-line applications, primary side freewheeling conduction losses do not constitute a considerable part of the total power loss since the primary current is low. However, the main problem in the medium/high power applications working from low battery voltages is the high currents in the primary side of the DC/DC converter. At low input voltages, standard PS-ZVS-FBC suffers from these high primary side conduction losses during the freewheeling period. Therefore, for medium/high power DC/DC converters working from low input voltages, topologies decreasing the primary current at the beginning of the freewheeling period should be preferred for high efficiency operation. In this work, a medium power PS-ZVZCS type DC/DC converter is designed as the power supply of 'VHF/FM Frequency Hopping Tactical Radio Family' working from low battery voltages (12/24V). When the DC/DC converter is fed from 12V batteries, the maximum output power is 450W. Maximum output power is 700W for the 24V battery case.

II. SYSTEM DESCRIPTION

A. System Specifications

The input/output specifications of the designed converter are as follows:

Output Voltage : 28V

Input Voltage Range

12V Battery : 10.5V-18V
24V battery : 18V-40V

Output Current

12V Battery : 16A
24V Battery : 25A

Efficiency

Half Load : 90%
Full Load : 88%

Switching Frequency : 50kHz

Operating Temperature : -40°C... +55°C

Mechanical Dimensions and Properties :

270 × 347 × 79 mm, MIL-STD-810C

The designed converter meets the military standards such as MIL-STD-461C (EMI/RFI criteria) and MIL-STD-1275A (Input surge and spike criteria).

The battery selection of the converter is done by one pole, two position toggle switch. In 12V battery mode, maximum output current is limited to 16A. In 24V battery mode, the maximum output current is limited to 25A. While setting the maximum output current levels, the predefined value of maximum input current (~50A) is the main factor. The user is warned by the alarm leds on the front panel in the case of short circuit, high internal temperature of the power supply and low input battery voltages.

B. Operating Principles of DC/DC Converter:

The block diagram of the DC/DC converter is given in Figure-1.

- Saturable cores in the primary side are used for the ZCS operation of the MOSFETs in the right-leg of full-bridge-converter.
- Saturable cores in the secondary side are used to decrease the reverse recovery losses of rectifier diodes.
- MOSFETs in the left-leg of full-bridge-converter is operated in ZVS mode.

A switching cycle consists of two symmetrical cycles including 8 time intervals. The typical waveforms of the designed DC/DC converter are shown in Figure-2. These time intervals are explained below:

Interval 1:

$t_0<t<t_1$: A: ON; D: ON

MOSFETs A and D are on. Diode D_2 carries the output current. Saturable cores L_d and L_2 are saturated. Voltage across the blocking capacitor is charging with the constant primary current.

Interval 2:

$t_1<t<t_2$: A: OFF; D : ON

At time t_1, MOSFET A is turned off. The primary current flows through MOSFET D and the output capacitances of MOSFETs A and B. As a result of the resonance between the leakage inductance of the transformer and the output capacitances of MOSFETs A and B, the voltage across MOSFET B begins to decrease. The reverse diode of MOSFET B clamps the voltage to 0V as shown in Figure-2. MOSFET B is turned on in ZVS mode.

Interval 3:

$t_2<t<t_3$: B: ON; D : ON

At time t_2, MOSFET B is turned on. The transformer primary voltage is $-V_{cb}$, and the voltage across the saturable core L_1 is $2nV_{cb}$. At time t_3, saturable core L_1 reaches saturation.

Interval 4:

$t_3<t<t_4$: B: ON; D : ON

The primary voltage is zero since diode D_1 is on. The voltage across the leakage inductance of the transformer becomes $-V_{cb}$. Therefore, the primary current decreases from I_{pfl} down to the saturation current of the saturable core L_d (I_{sat}). (Figure-2)

Interval 5:

$t_4<t<t_5$: B: ON; D : ON

Since the voltage across the leakage inductance is zero, $-V_{cb}$ appears on the saturable core L_d. At time t_5, MOSFET D turns off. MOSFET D turns off at the saturation current of saturable core L_d (ZCS).

Interval 6:

$t_5<t<t_6$: B: ON; D : OFF

Normally, this time period is necessary if IGBTs are used instead of MOSFETs. In this interval, the remaining minority carries of IGBT D are recombined. At time t_6, MOSFET C is turned on.

Interval 7:

$t_6< t<t_7$: B: ON; C : ON

The voltage $V_{in}+V_{cb}$ appears across the saturable core L_c, and at time t_7, saturable core L_c reaches saturation.

Interval 8:

$t_7<t<t_8$: B: ON; C : ON

$V_{in}+V_{cb}$ appears across the leakage inductance of the transformer. Hence, primary current decreases from I_{sat} to $-I_{pfl}$. (Figure-2)

Interval 9:

$t_8<t<t_9$: B: ON; C: ON

MOSFETs B and C are on. Diode D_1 carries the output current. Saturable cores L_c and L_1 are saturated. The voltage across the blocking capacitor is charging with the constant primary current.

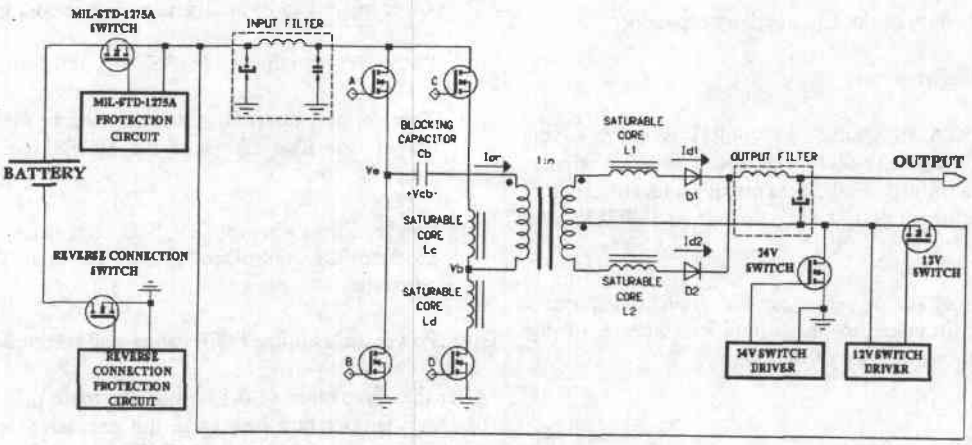

Figure-1. Block Diagram of the DC/DC Converter

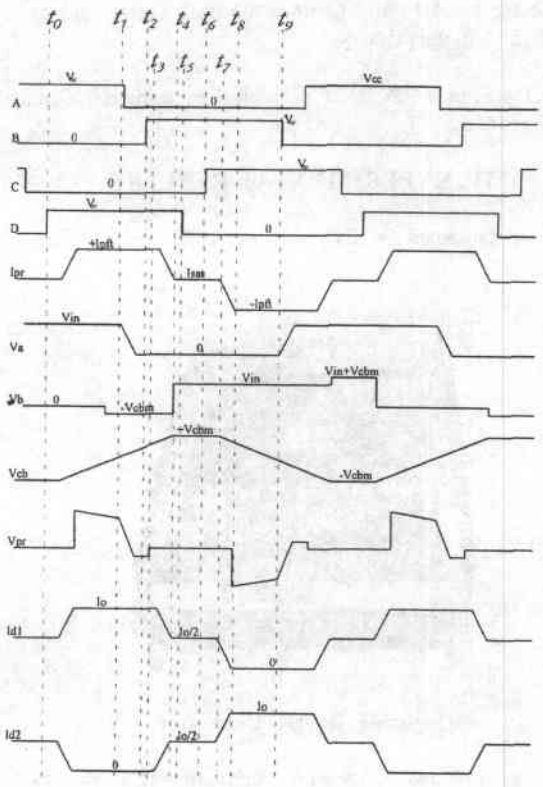

Figure-2. Typical Waveforms of Converter

III. DESIGN CONSIDERATIONS

The high temperature limit and the restricted mechanical dimensions of the DC/DC converter are the main reasons for which high power conversion efficiency is required. While the DC/DC converter is fed from a 12V battery, 12V switch is on, and 28VDC is obtained by adding the battery voltage to the SMPS output voltage. This reduces the power transformer turns ratio from (1:4) to (1:2) which reduces the primary currents from approximately 65A to 35A at an output current of 16A. Hence, high efficiency is obtained for the 12V battery input. For the 24V battery input, 24V switch is on, and 28VDC is obtained directly from the SMPS output voltage. (Figure-1)

A. Design Specifications

Following points are taken into consideration prior to the implementation of the DC/DC converter.

- The maximum voltage stress of the MOSFETs in the left-leg is V_{in}, however, the maximum voltage stress of the MOSFETs in the right-leg are $V_{in}+V_{cbm}$ where V_{cbm} (peak blocking capacitor voltage) is given in (1).

$$V_{cbm} = \frac{I_{pft} \times D_p}{2 \times C_b \times f_s}; \qquad (1)$$

$$I_{pft} = n \times I_o + I_m$$

where,

$$n = \frac{N_s}{N_p} \text{ (Transformer turns ratio);}$$

I_o: output current; Im: magnetizing current

D_p: primary duty cycle; Cb: blocking capacitor;

f_s : switching frequency

SUP75N05-06 (Siliconix, 50V/6mΩ) is used as the switching MOSFET of the DC/DC converter. Hence, V_{cbm} is determined by the maximum input voltage 40V and the maximum drain-source voltage of SUP75N05-06 (50V).

- Fall time of primary current from the positive maximum value to the saturation current of the saturable cores is given in (2).

$$t_4 - t_3 = \frac{I_{pft} \times L_r}{V_{cbm}} \qquad (2)$$

L_r: leakage inductance of transformer

- Fall time of primary current from the saturation current of the saturable cores to the negative maximum value is given in (3).

$$t_{12} - t_{11} = \frac{I_{pft} \times L_r}{V_{in} + V_{cbm}} \qquad (3)$$

- To guarantee the zero-voltage switching for the left-leg MOSFETs, the delay time between the gate signals of the MOSFETs in the left-leg must be greater then the transition time of the drain-source voltage from Vin to 0 volts.

B. Power Losses

The following points are considered in the efficiency calculations.

- MOSFETs in the left-leg have only turn-off switching and conduction losses.
- MOSFETs in the right-leg are turned off at the saturation current of saturable cores (ZCS). When these MOSFETs are turned on, the saturable cores L_c and L_d behave like a turn-on snubber. Hence, switching losses of these MOSFETs can be negligible as compared to the conduction losses.
- Core losses of the saturable cores can be neglected with respect to the copper losses at the given switching frequency.
- Reverse recovery losses of the rectifier diodes can be neglected with respect to the conduction losses at full load.

The power losses can be analyzed mainly in four groups:

(i) Power Semiconductors (MOSFETs and Diodes)

(ii) Transformer, toroidal inductors used in the input, output and EMI filters of the DC/DC converter, saturable cores

(iii) Power losses in the DC/DC converter which produces the control voltages of the main DC/DC converter

(iv) Power losses in the PCB, cables and feedthroughs.

After the completion of the design, the main problem in the high temperature tests was the excessive junction temperatures reached by the MOSFETs and diodes. To overcome this problem, MOSFETS A, B, C, D and diodes D_1, D_2 are paralleled. This reduces the conduction losses of MOSFETs to one fourth and that of the diodes to one half.

The copper losses of the toroidal inductors and the saturable cores are decreased by using double or multiple turns in parallel. This is extremely important for the saturable cores L_c and L_d since the peak current can go up to 50A in the primary.

The losses in the PCB are decreased by using a 70 μm, 4 layer PCB.

IV. EXPERIMENTAL RESULTS

The implemented DC/DC converter is shown in Figure-3.

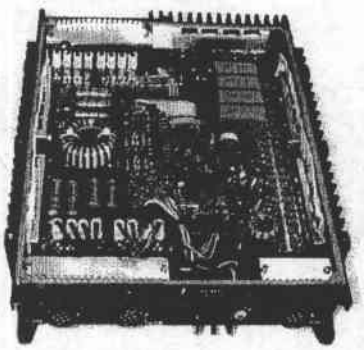

Figure-3. DC/DC Converter

In Figures 4 and 5, measured converter efficiency vs. load current characteristics are given. ZCS of the right-leg MOSFETs at turn-off, and ZVS of the left-leg MOSFETs at turn-on are illustrated in Figures 6 and 7 respectively.

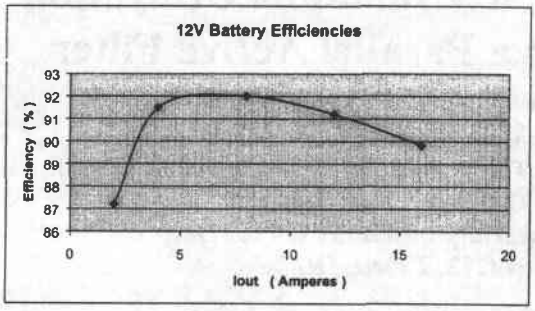

Figure-4. Efficiency vs. Iout (12V Battery)

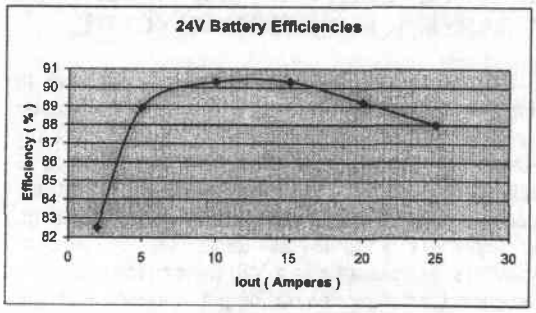

Figure-5. Efficiency vs. Iout (24V Battery)

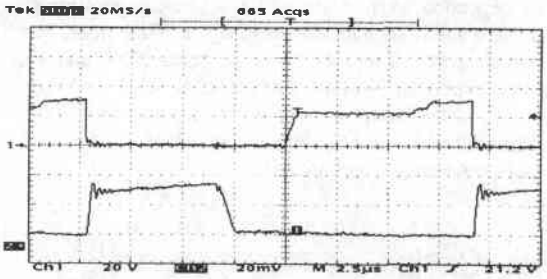

Figure-6. ZCS Waveform of MOSFET D at turn-off

Ch1: V_{ds} (D) (20V/div) Ch2: I_d (D) (20A/div)

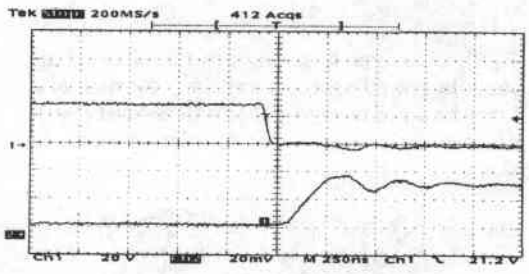

Figure-7. ZVS Waveform of MOSFET B at turn-on

Ch1: V_{ds} (B) (20V/div) Ch2: I_d (B) (20A/div)

V. CONCLUSIONS

PS-ZVZCS-FBC is successfully applied to a medium power DC/DC converter working from very low and wide range of DC input voltages. High primary current is the main problem for the medium/high power DC/DC converters fed from low input battery voltages. In order to decrease the transformer turns ratio, hence, the primary currents, two MOSFETs and additional control circuitry are added. At full load conditions, 90% efficiency is achieved with an output power of 450W when the DC/DC converter is fed from 12V battery. 88% efficiency is achieved at an output power of 700W for the 24V battery case.

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REFERENCES

[1] Fisher, A.R., Ngo, T.D.K., Kuo, H.M., "A 500 kHz, 250W DC-DC Converter with multiple outputs controlled by phase-shifted PWM and Magnetic Amplifiers", HFPC, 1988.

[2] Andreycak B., "Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller", HFPC, 1992.

[3] Hua, G.H., Lee, F.C., "An Improved Full-Bridge Zero-Voltage-Switched PWM Converter Using a Saturable Inductor", IEEE Transactions, 1993.

[4] Watson, R., Lee, F.C., "Analysis, Design, and Experimental Results of a 1kW ZVS-FB-PWM Converter Employing Magamp Secondary Side Control", IEEE APEC, 1994.

[5] Cho, J.G., Sabate, J.A., Hua, G., Lee, F.C., "Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter for High Power Applications", VPEC Seminar Proceedings, 1994.

[6] Rinne K., Theml K., McCarthy O., "An Improved Zero-Voltage and Zero-Current Switching Full Bridge Converter", PCIM, 1995.