A New FGMOS DXDDCC and A KHN Biquad as Application Example

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Abstract

In this work, a new floating gate MOS (FGMOS) dual-X differential difference current conveyor (DXDDCC) is presented. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS DXDDCC is used in a KHN biquad in order to show the versatility of the DXDDCC block. Both the FGMOS DXDDCC circuit and KHN biquad are simulated with SPICE simulation program by using 0.35um technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

1. Introduction

Designing circuits suitable for differential signals leads to have more versatile applications. There are lots of filter topologies in electronics literature employing the extensions of second generation current conveyor like differential difference current conveyor (DDCC) [1-2], differential voltage current conveyor (DVCC) [3-4], inverting current conveyor (ICCII) [5], current controlled conveyor (CCCII) [6-7] and dual-X current conveyor (DXCCII) [8].

In analog design, CCII represents one of the most useful building block. Many efficient applications can be designed with success using CCII as basic component. Anyway, second generation current conveyors, as they have been proposed, show some drawbacks. For example, only one of the input terminals presents a high impedance level. This can be a problem if differential signals have to be handled. To overcome this, a solution using more CCIIs has been proposed [9].

A different approach can be that to implement more complicated basic blocks, one of which will be presented in this paper.

Dual-X differential difference current conveyor (DXDDCC) may be considered as the most versatile building block that can be designed starting from the basic CCII. In fact, its topology can be thought as the "natural differential evolution" of the CCII idea. DXDDCC circuit block combines the advantages and versatility of DDCC and DXCCII together [10]. It has arithmetic signal processing capability of DDCC and gives opportunity to design filters with electronically tunable characteristics by utilizing two X terminals that is similar to DXCCII.

FGMOS structures are also known as multi-input MOS and their multi input advantages make it simpler to realize an arithmetic signal processing circuit. The FGMOS drain current is proportional to the square of the weighted sum of the input signals. In the last few years, FGMOS transistors have found many applications in electronic programming [11], Op-amp offset compensation [12], D/A and A/D converters [13], inverters and amplifiers [14], voltage attenuators [15], current mirrors [16] and low voltage analog circuits [16]. Recently, an increased number of publications on the use of the FGMOS in analog computational circuits have been reported voltage squarers and multipliers [17-18].

In this paper, a new FGMOS DXDDCC is proposed to obtain flexibility in analog IC design. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS DXDDCC is used in a KHN biquad in order to show the versatility of the DXDDCC block. Both the FGMOS DXDDCC circuit and KHN biquad are simulated with SPICE simulation program by using 0.35um technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

Rest of the paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS DXDDCC and simulation results of the proposed circuit are presented in Section III and Section IV, respectively. A KHN biquad, as an application example, is shown in section V followed by conclusion in section VI.

2. The FGMOS Transistor

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications [17-18]. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result the floating gate devices are not only used for memories but are also being used as circuit elements. FGMOS transistors are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements [18].

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node [18]. The equivalent schematic for an n-input n-channel FGMOS transistor is given in Figure 1.

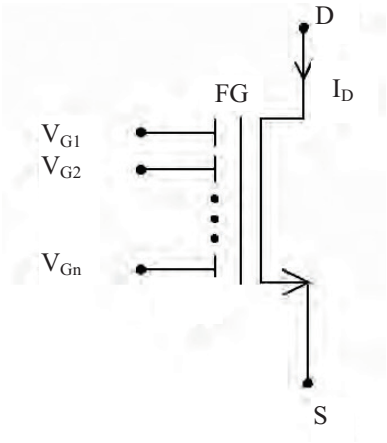

Fig. 1 n-input n-channel FGMOS transistor

3. FGMOS DXDDCC

Starting from the first and second generation current conveyors, many types of new topologies have been designed during the past years. DXDDCC is one of the most versatile circuit block which presents flexibility in analog circuit design with its arithmetic signal processing capability and gives opportunity to electronically tunable characteristics in application examples.

3.1. DXDDCC Circuit Building Block

DXDDCC is characterized by three high-impedance input terminals (Y_1, Y_2 and Y_3), two low-impedance node (X_1 and X_2) and one high-impedance output node (Z). Its block scheme and matrix characteristics are summarized below.

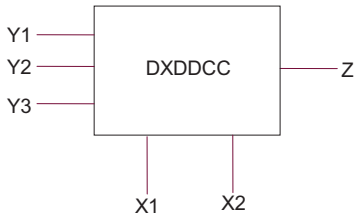

Fig. 2 DXDDCC block representation

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 \\ -1 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_{X1} \\ I_{X2} \\ V_Z \end{bmatrix} \quad (1)$$

In Fig.3 a CMOS DXDDCC is shown [10]. The DXDDCC shown in Fig. 3 is realized by combining the DDCC circuit given in [1] and the voltage inverting structure given in [5].

In the voltage inverting part of the CMOS structure, the ratio V_{X1} / V_{X2} is equal to the ratio of the transconductances of M_{12} and M_{13} [5]. That is,

$$\frac{V_{X1}}{V_{X2}} = -\frac{\mu_{M12}\dfrac{C_{OX}}{t_{OX}}\dfrac{W_{M12}}{L_{M12}}}{\mu_{M13}\dfrac{C_{OX}}{t_{OX}}\dfrac{W_{M13}}{L_{M13}}} \quad (2)$$

$V_{X1} = -V_{X2}$ is satisfied provided that,

$$\frac{\mu_{M12}}{\mu_{M13}} = -\frac{\dfrac{W_{M12}}{L_{M12}}}{\dfrac{W_{M13}}{L_{M13}}} \quad (3)$$

3.2. FGMOS DXDDCC

Fig. 4 shows the proposed floating gate dual-X differential difference current conveyor circuit employing FGMOS differential pairs instead of conventional pairs to improve the circuit behavior. CMOS DXDDCC circuit given in Fig. 3 employs two differential pairs in order to get the relationship of $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and uses a voltage inverting structure (M13 – M20) to take the opposite of V_{X1} namely $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y3}$. In FGMOS DXDDCC circuit given in Fig. 4 only two FGMOS differential pairs are used to get both $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y3}$. It is clearly seen that by using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier [18]. In addition to these, new Y nodes can be added to FGMOS DXDDCC circuit without any new transistors by only increasing the inputs of FGMOS transistors already used in differential pairs. This also reveals the flexibility of using FGMOS transistors in circuit blocks employing arithmetic calculations.

FGMOS transistors in differential pairs have three and four inputs which are applied through equal sized capacitors, C_i. The input signals of V_{Y1}, V_{Y2}, V_{Y3} and the control voltage V_C are applied to one of the floating gates in the differential pairs. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

Determining parameters of voltage and current conveying properties are the slopes of related transistors and it is achieved easily by choosing matched transistors.

Impedance values of X, Y, Z nodes of the FGMOS DXDDCC circuit can be seen as small at X node because of feedback and high at Z node because of the drain nodes of M15 and M16.

4. Simulation Results

The proposed circuit of Fig. 4 is simulated with SPICE by using 0.35µm TSMC technology parameters. The supply voltages are ±1.5V, V_C is set to V_{DD} and bias current I_B = 10µA. The input capacitor values are taken C_i= 16,25fF while the C_{FGD} and C_{FGS} values are calculated as 0.2fF and 1.63fF, respectively. The dimension for n-type transistors is W / L = 0.7µm / 0.7µm and for p-type transistors is W / L = 1.4µm / 0.7µm.

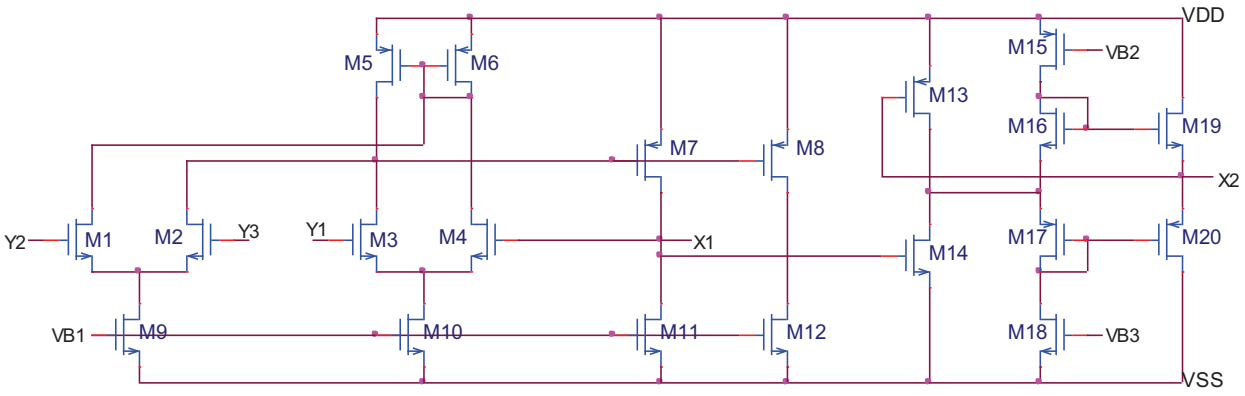

Fig. 3 CMOS DXDDCC circuit

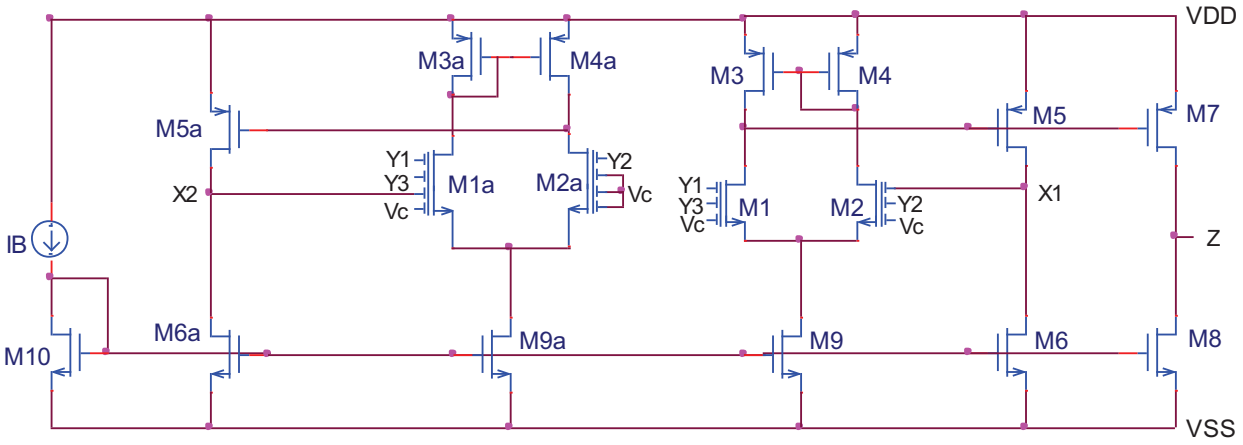

Fig. 4 FGMOS DXDDCC circuit

Fig. 5, Fig. 6 and Fig. 7 show the DC voltage transfer characteristics of the proposed circuit with respect to $V_{Y1, Y2, Y3}$ input DC voltages. DC voltage $V_{Y1, Y2, Y3}$ is swept between -1.5V and 1.5V while the DC voltage $V_{X1, X2}$ is plotted.

In Fig. 5, Fig. 6 and Fig. 7 while V_{Yi} is -1.5V, V_{X1} and V_{X2} take -1.49V and 1.4V, respectively. While V_{Yi} is 1.5V, V_{X1} and V_{X2} take 1.4V and -1.49V, respectively. As it is seen from these values, input swing is almost equal to the supply voltages.

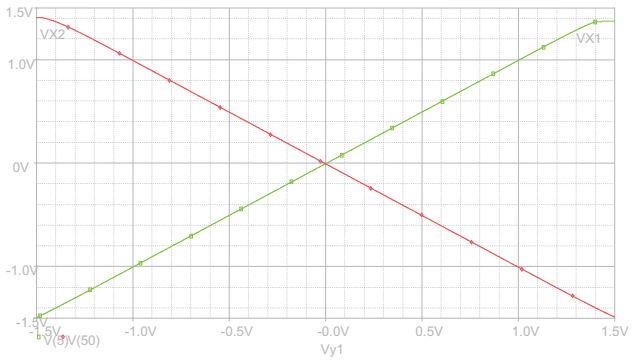

Fig. 5 FGMOS DXDDCC DC voltage transfer characteristics (V_{X1}-V_{Y1} and V_{X2}-V_{Y1})

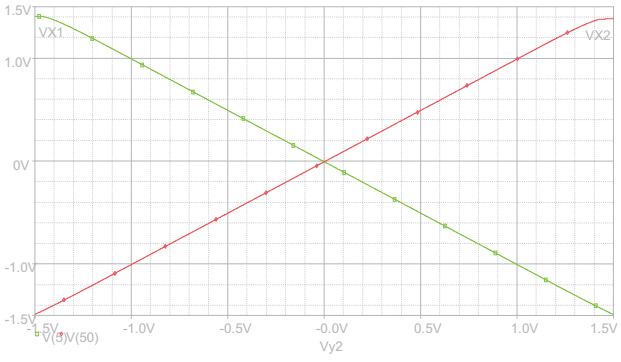

Fig. 6 FGMOS DXDDCC DC voltage transfer characteristics (V_{X1}-V_{Y2} and V_{X2}-V_{Y2})

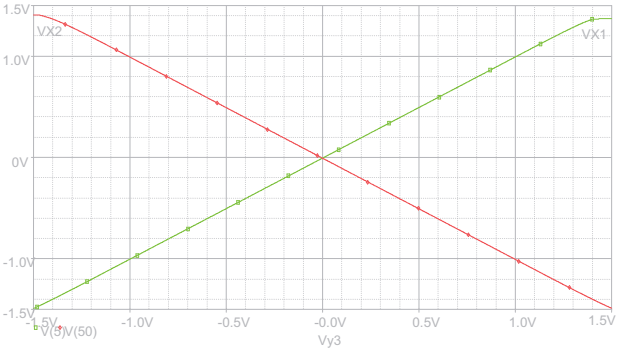

Fig. 7 FGMOS DXDDCC DC voltage transfer characteristics (V_{X1}-V_{Y3} and V_{X2}-V_{Y3})

Fig. 8 shows the DC voltage transfer characteristics of the proposed FGMOS circuit and the CMOS circuit together. V_{X1} is plotted for both circuits. As it is seen from the figure, input swing is increased by using FGMOS transistors.

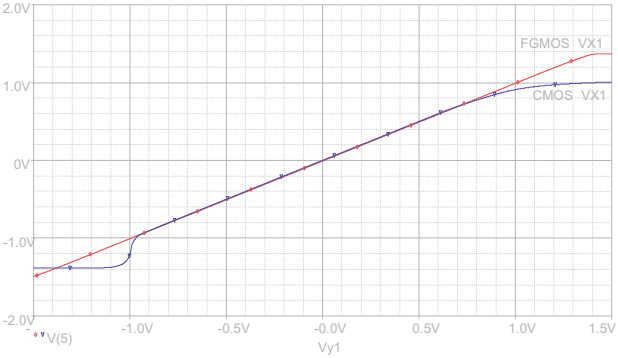

Fig. 8 DC voltage transfer characteristics of the proposed FGMOS circuit and CMOS circuit

Fig. 9 shows the DC current transfer characteristic of the proposed circuit with respect to I_B bias current. DC bias current I_B is swept between -10µA and 10µA while the DC output current I_Z is plotted.

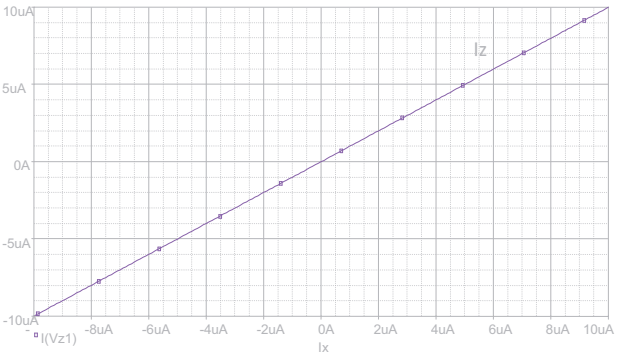

Fig. 9 FGMOS DXDDCC DC current transfer characteristic

Fig. 10 shows the AC voltage transfer characteristics of the proposed circuit with respect to V_{X1} and $V_{Y1,\ Y2,\ Y3}$. 3dB frequency values of the characteristics have been determined as 262MHz for $V_{Y1,\ Y3}$ and 470MHz for V_{Y2}.

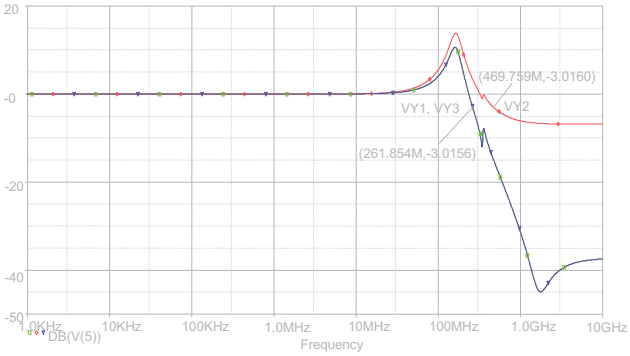

Fig. 10 FGMOS DXDDCC AC voltage transfer characteristics (V_{X1}-$V_{Y1,\ Y2,\ Y3}$)

Fig. 11 shows the AC voltage transfer characteristics of the proposed circuit with respect to V_{X2} and $V_{Y1,\ Y2,\ Y3}$. 3dB frequency values of the characteristics have been determined as 680MHz for $V_{Y1,\ Y3}$ and 535MHz for V_{Y2}.

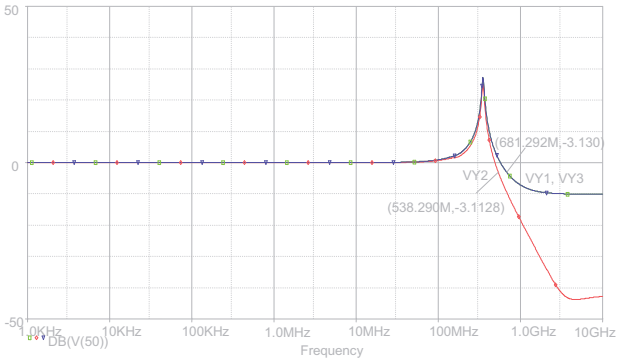

Fig. 11 FGMOS DXDDCC AC voltage transfer characteristics (V_{X2}-$V_{Y1,\ Y2,\ Y3}$)

Fig. 12 shows the AC current transfer characteristic of the proposed circuit with respect to I_{X1} and I_Z. 3dB frequency value of the characteristic has been determined as 475MHz.

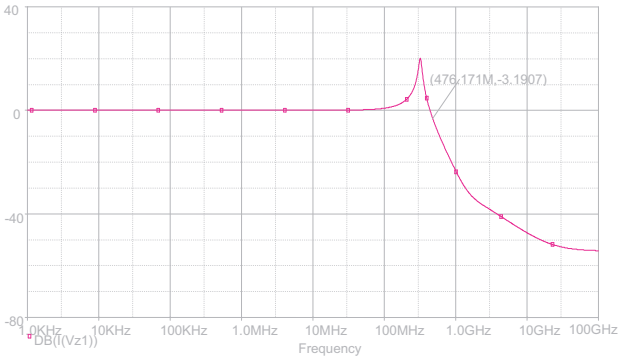

Fig. 12 FGMOS DXDDCC AC current transfer characteristic

Impedance values of X_1, X_2, Y_1, Y_2, Y_3 and Z nodes have been also determined as 1.46kΩ, 1.78kΩ, 1.43TΩ, 1.36TΩ, 1.43TΩ and 1.57MΩ, respectively.

5. A KHN Biquad as Application Example

The KHN biquad is known to be a good filter structure which has preferable properties like low sensitivity, low element value spread and good stability behavior [10].

A resistorless, electronically tunable KHN biquad employing two DXDDCCs, two MOSFETs and two capacitors is given in Fig.13.

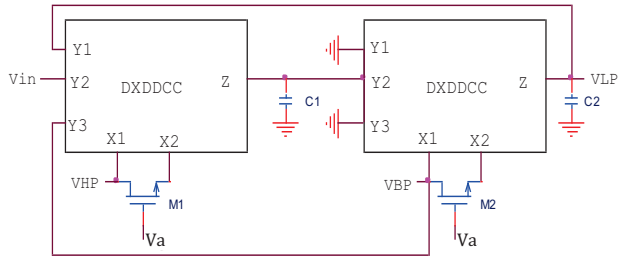

Fig. 13 A KHN biquad employing two DXDDCC

If MOSFETs which are used as resistors (M1 and M2) have equal transconductance parameters and gate voltages, then the angular frequency (ω_0) and the quality factor (Q) can be expressed as;

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2}} 2\beta(V_a - V_{TN}) \tag{4}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{5}$$

As it is seen from the above equations, the angular frequency of the KHN biquad employing DXDDCCs can be electronically tuned by changing the control voltage V_a.

Fig. 14 shows the lowpass, bandpass and highpass characteristics of the filter for various control voltages. Capacitor values are taken as $C_2 = 2C_1 = 1$pF and V_a is stepped between 1V and 1.5V with 0.25V step size.

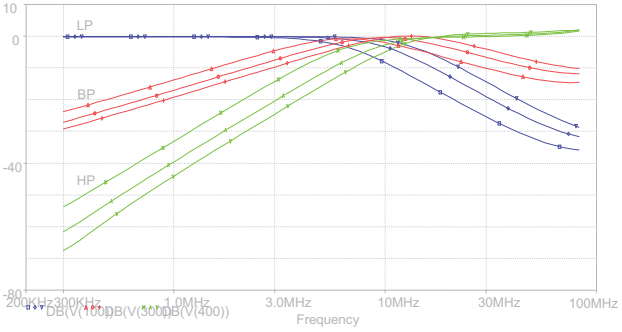

Fig. 14 LP-BP-HP filter characteristics of KHN biquad

6. Conclusion

A new FGMOS DXDDCC has been designed and simulated. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS DXDDCC is used in a resistorless, electronically tunable KHN biquad in order to show the versatility of the DXDDCC block.

7. References

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