A 2.2GHZ-2.9V CHARGE PUMP PHASE LOCKED LOOP DESIGN AND ANALYSIS

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ABSTRACT

This paper studies the design and analysis of charge pump phase locked loops (PLLs), the components of the PLLs are analyzed briefly, with the design of a second order charge pump phase locked loops (PLLs). In the last decade a lot of works have been done about the analysis and design of PLLs.

In this paper the PLLs are analyzed briefly which is used widely in communication systems and digital applications, with the design of 2.2 GHz-2.9V second order CP-PLL.

The design is applied to the SPICE simulation program, which shows the satisfactory results.

I. INTRODUCTION

Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizers in communication systems for clock extraction and generation of a low phase noise local oscillator [1].

The PLLs was first described in early 1930s, where its application was in the synchronization of the horizontal and vertical scans of television. Later on with the development of integrated circuits, it found uses in many other applications. A PLL is a feedback control circuit, and is operates by trying to lock to the phase of a very accurate input through the use of its negative feedback path. A basic form of a PLL consists of three fundamental functional blocks namely [1,2]:

1. A Phase frequency Detector (PD)
2. A Loop Filter (LF)
3. A Voltage Controlled Oscillator (VCO)

With the circuit configuration shown in figure 1:

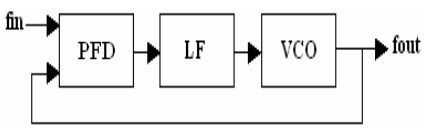


Figure 1. A basic PLL block diagram

The phase frequency detector compares the phase and frequency of the output signal to that of the input signal, and generates an output voltage, which is proportional to the phase error or frequency difference of the two signals. This output voltage passes through the LF and then as an input to the VCO controls the output frequency. Due to this self-correcting technique, the output signal will be in phase and same frequency with the input signal. When both signals are synchronized, the PLL is said to be in lock condition. The phase error and frequency difference between the two signals is always zero at this time [3].

II. PLL ANALYSIS

A typical PLL consists of four main components rather than three components of basic PLLs: The phase frequency detector (PFD), the charge pump (CP), the loop filter (LF), and the Voltage controlled oscillator (VCO) [2,4].

- The phase-frequency detector (PFD) compares feedback and reference signals and generates an error signal, which is proportional to the magnitude of the phase/frequency difference between them.

- This error signal is fed to the charge pump. The charge pump (CP) current controls the magnitude of charge stored in the loop filter [1,5].

- The loop filter (LF) While this can be omitted, resulting in what is known as a first order PLL, it is always conceptually there since PLLs depend on some sort of low pass filtering in order to function properly, thus converting the PFD output to a control voltage input recognizable by the voltage controlled oscillator (VCO).
- A voltage controlled oscillator (VCO). Which is a nonlinear device, which produces an oscillation whose frequency is controlled by the voltage from the loop filter (LF)In this Project phase locked loops are analyzed briefly, with the design of a second order PLL, which is more popular than the other types, easier to design, and it used widely in digital designs and communication systems [6].

Phase Frequency Detector (PFD)

The phase frequency detector detects any difference between the two input signals f_{in} and f_{out}, and generates the control signals to the charge pump to modulate the amount of charge stored in the low pass filter; the output voltage of the low pass filter controls the frequency oscillation in the VCO [5,7].

The output of the PFD is two control signals called UP and DOWN. If f_{in} is higher or leading the f_{out}, the f_{out} has to speed up, hence the Up signal is activated and when f_{in} is lower or lagging the f_{out}, the f_{out} has to slow down, hence, the DOWN signal is then activated [4,6].

A possible implementation of the frequency detector is shown in figure 2.

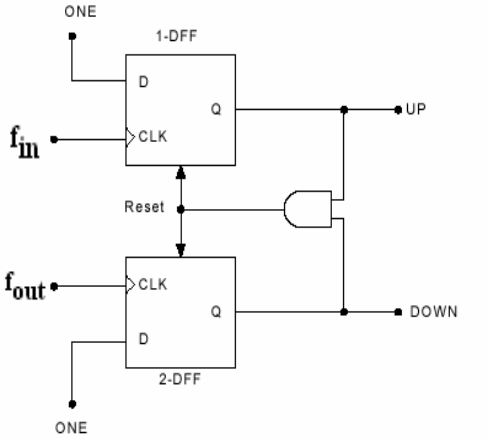


Figure 2. The Phase Frequency detector (PFD)

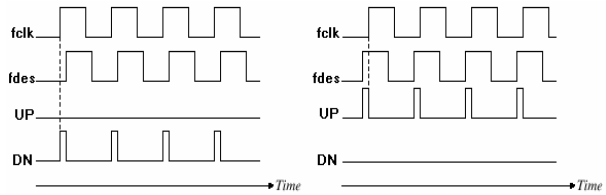
The operation of this circuit is based on two D-type flip-flops and a simple AND gate .the output signal depends on the frequency or phase error between the two inputs:

$$\Delta f = \Delta f_{in} - \Delta f_{out} \quad (1)$$

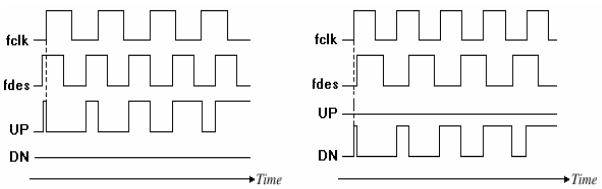
and

$$\Delta \phi = \Delta \phi_{in} - \Delta \phi_{out} \quad (2)$$

If the frequency fin of the input 1 is higher than the frequency fout of input 2 then the frequency detector generate positive pulses at the output Q2, while Q1 remains at zero, same is true for the other case, when fin fout positive pulses appear at Q1 and Q2 remains at zero, the width of pulses is depends on the frequency difference between the two inputs as shown in figure 3.If fin=fout, then no pulse appears at either Q1 and Q2, this case will be introduced in the design of the PLL circuit [3,4,8].



a) $\phi_{in} < \phi_{out}$ b) $\phi_{in} > \phi_{out}$



c) $f_{in} > f_{out}$ d) $f_{in} < f_{out}$

Figure 3. Output of the PFD

Charge Pump (CP)

The Charge Pump (CP) converts the output of the PFD, Up and DN pulses to a DC voltage. CP consists of two switches with two current sources. The output of the CP drives the loop filter (LF). The CP either charges or discharges the capacitor in the LF. It means this component generates the control signal by adding or removing charges in the LF [4,9].

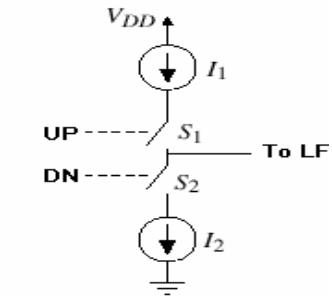


Figure 4. Charge Pump (CP)

The first switch is closed when pulses appear at UP output of the PFD, and these pulses of charge pump charge up the LF capacitance. The second switch is closed when pulses appear at DN output of the PFD. So the voltage at the loop filter rises or falls according to the UP and DN outputs. In practical application the FET transistors can be used instead of the switches and current sources, for both applications the FET transistors can operate as the switch and as the constant current source [9].

Loop Filter (LF)

The function of the loop filter is to convert the output signal of the charge pump to the VCO control voltage and also to filter out any high frequency noise introduced by the PFD.

According to the applications either active or passive loop filter may be employed. Active filters contain amplifying devices to amplify the signal while passive filters contain amplification devices. Therefore, in passive filters the output level is always less than the input. A low pass filter is a combination of capacitance, inductance, or resistance [7,10,11].

The simplest low pass filters consist of a series resistor with a capacitor (RC filter) that is suitable and easy to build.

PLLs typically employ a 2nd order passive RC network for the loop filter implementation.

Figure 5 shows simple RC low pass filter (1st order LF) [11].

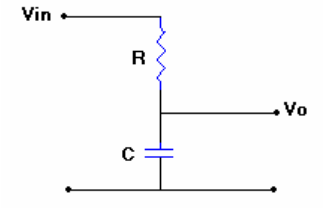


Figure 5. Simple RC low pass filter (1st order LF)

$$Vo = \frac{1/\ jwc}{1/\ jwC + R} Vin \qquad (4)$$

$$\left[Vo = \frac{1}{1/\ jwRC} Vin \right] \qquad (5)$$

Figure 6 shows a combination circuit of PFD, CP, and LF (1st order):

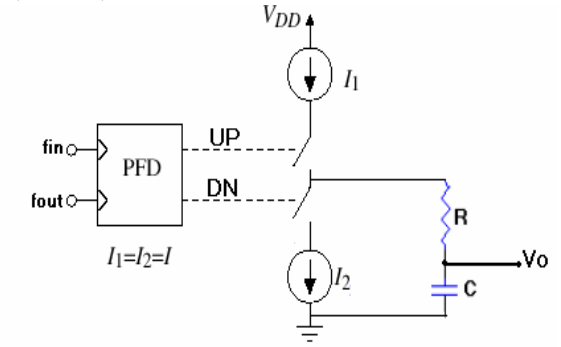


Figure 6. A combination circuit of PFD, CP, and LF

Figure 7 shows output voltage of the LF when UP signal is activated:

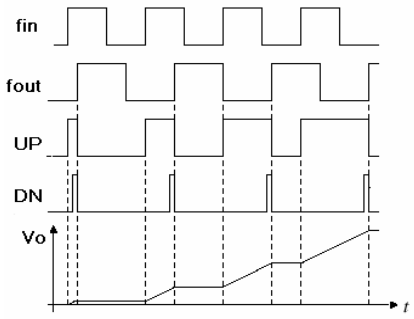


Figure 7. Output voltage waveform of the LF
When UP signal is activated

Voltage Controlled Oscillator (VCO)

Voltage controlled oscillators are means of the generation of periodic signals in circuits. The VCO output frequency is approximately has a linear proportion with the input voltage from the loop filter. Therefore, changing the applied voltage to the VCO results the variable frequency output of a VCO [11,12,13].

There are two main types of VCO's; astable multivibrators and ring oscillators. For high frequencies the ring oscillators VCO is suitable, that can be designed for a fixed and variable frequency operation. Connecting an odd number of inverting stages can generate the oscillation as shown in figure 8:

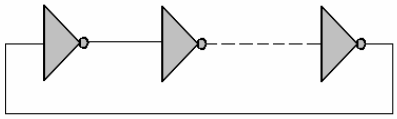


Figure 8. Ring oscillator VCO

The CMOS invertors are a method of implementing a ring oscillator that produce good stability with respect to the control voltage variation, generate a wide range of frequencies, and easy interface with the other circuit elements [14,15].

The frequency of oscillation can be determined by the equation:

$$f = 1/T = 1 / 2\ N\ td \qquad (5)$$

Where,

f is the frequency of oscillation,
td is the propagation delay per stage, and
N is the number of stages.

Figure 9 shows a typical PLL circuit diagram with PFD, CP, LF (1st order), and VCO components:

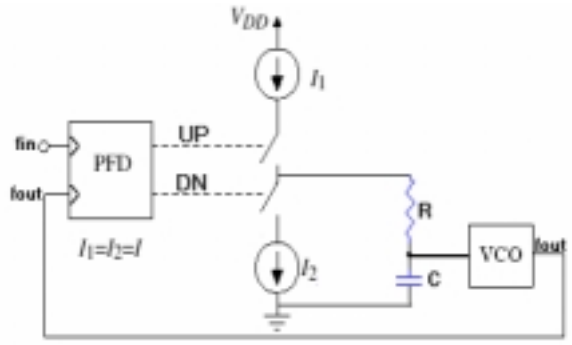


Figure 9. A typical PLL circuit diagram with PFD, CP, LF (1st order), and VCO

III. 2.2GHZ-2.9V CP-PLL DESIGN

Because of the benefits of second order loop filters and its application in microprocessors and digital designs, the 2nd order LF of figure 10 is designed and simulated [11,12].Figure

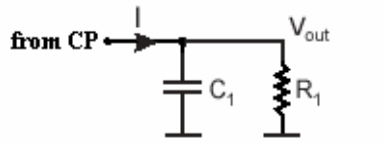


Figure 10. Loop filter (LF) circuit diagram

$$\frac{V_{out}}{I} = \frac{R_1}{1 + SR_1C_1} \quad (6)$$

After the LF circuit simulation, and according to the Equation 6, the values of R and C are determined.

R=2.265 KΩ
C=1.39µF

VCO Design

After the simulation of a simple CMOS inverter to measuring the propagation delay td of a single stage the following results of Table 1 is obtained.

t_d (ns)	V_{DD} (v)	f (GHz)
0.0323	2.9	2.2
0.0336	2.81	2.12
0.0340	2.7	2.1
0.0366	2.68	1.95

Table 1. Time delay vs supply voltage and frequency of CMOS inverter stage

According to the results of table 1and the equation 5, it is clear that the 7-stages (N=5) of the CMOS inverter is possible to the selected ranges of the voltage and frequency.

The complete design circuit of the CP-PLL

The complete design circuit of the 2nd order CP-PLL is shown in figure 11.

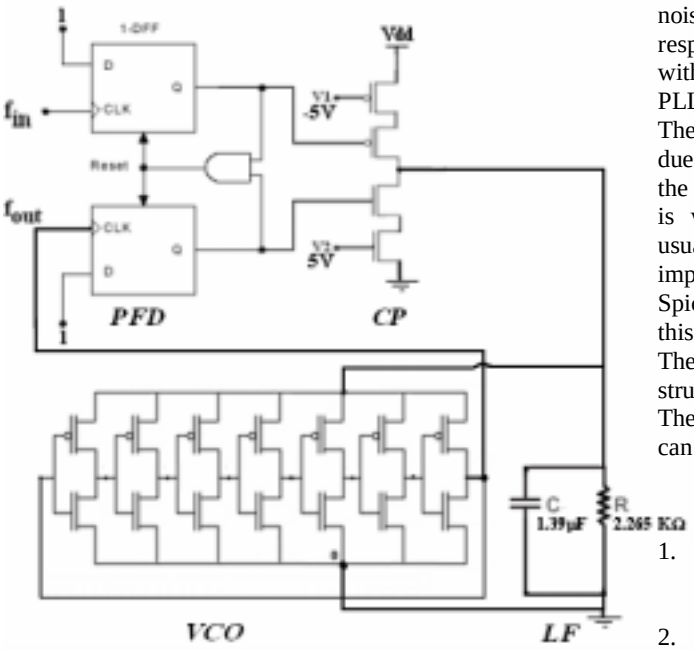


Figure 11. The complete design circuit of the2nd order CP-PLL

V. SIMULATION AND RESULTS

The CP-PLL circuit diagram is simulated for different cases of fin and fout, and then the following results of Table 2 are recorded.

f_{in} (GHz)	f_{out} (GHz)	PFD active pulses	CP output (V)	LF output (V)	VCO output (GHz)
1.95	2	DN	2.733	2.641	1.949
2.75	2.2	DN	2.542	2.492	2.77
2.88	2.88	NONE	2.832	2.774	2.878
2.9	2.8	UP	2.873	2.841	2.9

Table 2. CP-PLL Pspice simulation results

VI. CONCLUSION

Designing and analysis of PLLs is very challenging since a number of performance metrics have to be taken into account simultaneously such as PFD response, the accurate design of LF (the loop filter parameters), VCO gain (KVCO), and charge pump current (I). The design is complicated because these metrics are effect on the improvement and PLLs applications. Any PLL designs don't include all theses metrics could not been considered. The charge pump gain and the loop filter resistance are the two parameters that can be utilized to improve the noise at low frequency offsets and large frequency offsets respectively. In this work the PLLs are analyzed briefly, with the steps to a proper 2nd order 2.2GHz-2.9V CP-PLL design.

The PLL design by this method has a high performance due to accuracy in progress, and can significantly improve the PLL applications such as frequency synthesizer, which is widely used in high-speed data processing, and it usually implemented by PLLs because of low implementation cost and excellent noise performance.

Spice simulation program shows the satisfactory results of this work.

These results prove that the switched tuning CMOS-VCO structure is suitable for digital designs.

Therefore, the analysis and design of PLLs by such away can be considered as a suitable way for any PLL

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