Chip-Dependent Leakage Power-Aware Placement Algorithm for FPGAs

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Abstract— **Leakage power contribution in total power has been more than dynamic one in Deep Sub-Micron (DSM) technologies because of V_{th} decremsent. Furthermore, process variation has become as the main challenge in those technologies. In this paper, an optimized process variation-aware Field Programmable Gate Array (FPGA) placement algorithm has been proposed for leakage power reduction without any architecture modification costs. Estimated process variation-aware Clustered Logic Block (CLB) leakage power in each placement perturbs has been applied into the placement algorithm cost function. V_{th} variation map extraction using test circuits such as Ring Oscillators is the pre-placement processing level. Extracted map has been used for estimating leakage power and critical path delay in placement. Proposed placement algorithm that's named Total Power Aware Placement (TPAP) is implemented on VPR and power estimation and measurement has been computed by PowerModel and ACE tools in 45-nm technology. Simulation results for 20 MCNC benchmark circuits show that Power-Delay Product (PDP) parameter has been improved nearly 7.2% compared with default VPR placement algorithm. Simulations for each benchmark circuit are repeated 10 times for different variation maps. Results show that, PDP improvement standard deviation is 16.8%. As a result, proposed placement algorithm is adaptable with per-chip variation map, so proposed algorithm has been named chip-dependent algorithm.**

Keywords: FPGA; Process Variation; leakage power; placement algorithm

I. INTRODUCTION

As high performance technologies move toward lower feature sizes, leakage power consumption contributes more than dynamic one because of threshold voltage decreasing [1]. As leakage power consumption in FPGAs has been became 6X and CLB's leakage power has been became 15X with technology scaling decreasing from 130-nm to 65-nm [2]. So CLB's leakage power reduction in DSM technologies can have great effects on total leakage power reduction. In this paper CLB's leakage power as one of the major power consumption sources, beside the dynamic power has been optimized with proposing process variation-aware placement algorithm.

The main process variation parameter is threshold voltage that can causes frequency and leakage power variation in DSM technologies. For example in 45-nm technology, leakage power variation between different IC's has been measured 20X variant and up to 30% variant in frequency [2] because of parameter variation.

In this paper, FPGA placement algorithm has been controlled for CLB's leakage power optimization with appropriate using from intrinsic process variation, without any architecture modification costs. Chip-dependent algorithm means variation map-aware placement one that has been proposed in this paper. Chipwise process variation map can be extracted using ring oscillator circuits and according to FPGA programmability feature [3]. So a pre-placement processing level is required for V_{th} variation map extraction that will be introduced in the next sections. In the next step, estimated process variation-aware CLB leakage power in each placement perturbs has been applied into placement cost function. Because of placement effects on dynamic power, estimated dynamic power in each placement perturb is participated with estimated leakage one, into cost function for optimizing total power. As a result, estimated total power has been applied into placement cost function for optimizing total power consumption. Proposed placement algorithm effects on different power consumption resources in the common FPGA architecture have been analyzed for different utilization rate FPGAs.

A. Previous Works

There have so many papers about leakage power optimization methods in FPGAs. The majority of them require architecture modifications such as Multi_V_{th} architecture for routing switches, CLBs and SRAM bits [4, 5, 6]. Against to those papers, proposed method in this paper uses intrinsic variation to leakage power optimization without any modification costs. In this section some of the proposed methods for FPGA power optimization will be introduced.

Process variation in DSM technologies has been converted to one of most important challenges. Several recent papers have proposed variation-aware CAD algorithms for yield, frequency and power optimization in FPGAs. Most of them such as [7,8,9] have focused on frequency optimization without any considering on leakage power consumption. Process variation parameters have been modeled as the random variables with usually normally distribution. Against to proposed technique in this paper, any of them haven't proposed per chip process variation CAD algorithms. Bu in paper [10] a chipwise placement algorithm has been proposed just for frequency optimization without any considering on leakage power consumption.

In paper [11] researchers consider dynamic power control in FPGAs and present CAD techniques for dynamic power reduction. Proposed techniques, comprising power-aware placement, routing, and a novel post-routing transformation, are applied to optimize the power consumed by industrial designs implemented in the Xilinx VirtexTM-5 FPGA. Board-level power measurements on a suite of industrial designs show that the techniques reduce power by 8.6%, on average. Proposed placement algorithm in this paper that's named Dynamic Power Aware Placement (DPAP), is the main comparison case with our proposed placement algorithm. In the result section of mentioned paper several important parameters don't be reported. So for complete comparisons, their proposed placement algorithm has been implemented.

B. Innovations

Extracted process parameter variation map, as the pre-processing step, has been used for appropriate placement to leakage and dynamic power optimization. Following cases can be this paper's innovations:

- **Chip-dependent placement algorithm:** The first pre-placement phase in this paper is variation map extraction using ring oscillator circuits. Extracted V_{th} variation map has been used for leakage power estimation in CLBs, so first innovation in this paper can be proposing an optimized placement algorithm according to extracted V_{th} variation map. Each FPGA chip has a different variation map with the others so to leakage power optimization proposed algorithm should be adaptable with different variation maps. In this paper per chip placement algorithm is proposed and that's adaptable with any variation maps, so the chipwise placement algorithm placing blocks according to the variation map. As a result it would have an appropriate achievement in different fabricated FPGAs.
- **Total power, leakage and dynamic power, optimization:** Leakage power has two different aspects: active leakage power is the consumed leakage power in used and mapped resources and static leakage power is the consumed power in unused ones. In this paper both of them beside dynamic power has been considered in placement algorithm. Estimating each of them in the placement level has different method that considered in this paper. Another word, total power has been considered in the placement cost function for different utilization rates, so optimizing dynamic power, static and active leakage power is the main purpose of proposed algorithm.

Mentioned cases are the most important innovations for this paper. Finally they have been caused to total power consumption optimization.

This paper is organized as follows: Section II introduces FPGA structure, power concepts and process variation modeling method. Section III introduces proposed placement algorithm and it's capabilities to power consumption optimization with power estimation methods illustration. Sections IV and V consist of simulation results, paper results conclusion and future works.

II. BACKGROUND

A. Common Island-Based FPGAs

Island-based FPGAs as the most common FPGA architectures consist of logic resources, routing resources and programmable SRAM bits in their structure. In this paper, placement algorithm has been modified for leakage, dynamic and total power.

B. Leakage Power

In order to maintain the switching speed improvement of the scaled CMOS devices, their threshold voltage is also scaled down to maintain a constant device overdrive. However decreasing V_{th}, cause to exponential increasing in the sub-threshold leakage current [1]. Following equation illustrates a CMOS closed formulation.

$$I_{sub} = \mu_0 . C_{ox} . \frac{W_{eff}}{L_{eff}} . V_t^2 . e^{1.8} . \exp\left(\frac{V_{gs} - V_{th}}{nV_t}\right) . \left(1 - \exp\left(\frac{-V_{gs}}{V_t}\right)\right),$$

Where μ_0 is the device mobility, C_{ox} is the oxide capacitance, W_{eff} and L_{eff} are the effective device dimensions, V_t is the thermal voltage (kT/q) and V_{gs} is the Gate-Source voltage. According to mentioned formulation sub-threshold leakage current contribution in total power dissipation increases with technology scaling due to the continuous reduction in V_{th} to maintain the device performance. As an example, in 45-nm technology leakage power contributes more than 50% of the total consumed power.

C. Dynamic Power

Dynamic power as the consumed power due to signal transition, beside the leakage power is another parameter that's considered in placement algorithm. A netlist's dynamic power is sum of the dynamic power of nets that's formulated as the following formulation [11].

$$P_{dyn} = \frac{1}{2} \sum_{i \in netlist} \alpha_i . C_i . V_{dd}^2 . f,$$

Where α_i activity net is i, C_i is capacitance net i, V_{dd} is the supply voltage and f is the netlist frequency.

D. Processs Variation

Process variation is the most important challenge in DSM technologies. It has die-to-die (D2D) and within-die (WID) components, with the WID component further subdividing into random and systematic components. By

definition, systematic variation exhibits spatial correlation, therefore nearby transistors share similar systematic parameter values. In contrast, random variation has no spatial correlation therefore a transistor's randomly varying parameters differ from those of its immediate neighbors.

$$\Delta P = \Delta P_{D2D} + \Delta P_{WID} = \Delta P_{D2D} + \Delta P_{sys} + \Delta P_{rand},$$

Variation in any parameter can be represented as mentioned formulation. For extracting V_{th} variation map we use VARIUS, as an open source tool for process variation map modeling [12]. Spatially correlation has been modeled as a function of linear distance between two points. V_{th} as the main process variation parameter has great effects on leakage power consumption, frequency and timing yield, so in this paper only V_{th} parameter is considered and its variation map has been considered using VARIUS tool.

III. PROPOSED PLACEMENT ALGORITHM

Proposed placement algorithm requires several pre-processing preliminaries to estimate dynamic power, leakage power and extract process variation map. In this section the proposed placement algorithm has been described and power estimation methods and process variation map extracting method have been introduced too. Chip-dependent placement algorithm has been resulted by considering per-chip extracted variation map in the placement algorithm. Extracting per-chip variation map is a pre-placement step.

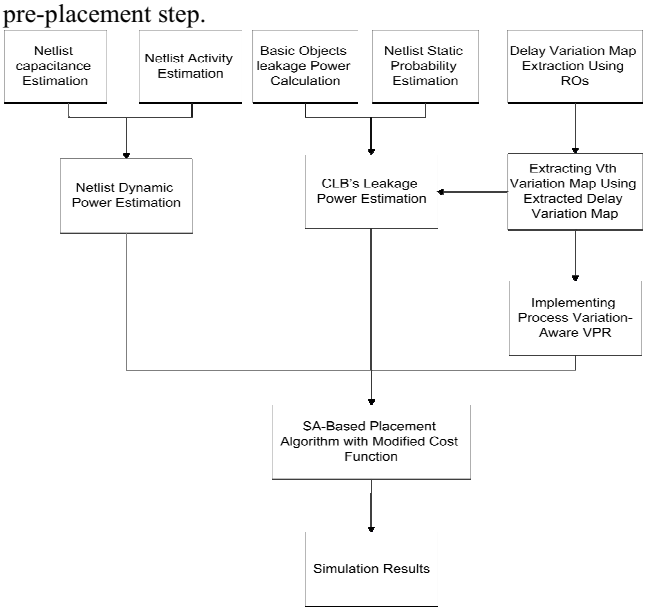

Figure 1. Proposed placement algorithm flowchart

Default cost function in VPR's placement algorithm consists of several parameters for congestion and critical path delay control [13]. Proposed placement algorithm in this paper has a modified cost function that considered power parameters. Variation-aware leakage power and dynamic power estimation are other parameters that considered in this paper. Proposed placement algorithm's flowchart has been specified in the Figure.1. Proposed placement algorithm requires several pre-placement preliminaries include:

- Process variation map extraction
- Dynamic power estimation
- Variation-aware leakage power estimation
- Cost function modification

Proposed chip-dependent placement algorithm defines by mentioned steps. Each of them has been demonstrated in following sections.

A. Process Variation Map Extraction

In this paper, extracting process variation map as a pre-placement processing level is the most important section for chip-dependent algorithm proposing. Extracting deterministic process variation map and using it for leakage power and critical path delay controlling is the main purpose of this section. After extracting variation map and applying it in the mentioned parameters, chip-dependent CAD algorithms can be resulted. Deterministic V_{th} variation map has been extracted by translating extracted delay variation map and delay variation map extraction has been done with Ring Oscillator circuit's distribution all over the chip.

Delay variation map can be extracted using ring oscillator circuits. Ring oscillators are a chain of NOT gates that their frequency measurement in different places can result delay variation map. Extracted delay variation map can be translated to V_{th} variation map by follow formulation [3].

$$\Delta V_{th=} V_{dd} - V_{th0} - \left(\frac{F V_{dd} T^{1.9}}{K}\right), ^{(1/v)}$$

Where V_{dd} is the supply voltage, T is the temperature, K is a proportionality constant, F is the measured frequency for an ring oscillator multiplied by N, the number of transistors in the signal's path in an ring oscillator, v is the velocity saturation coefficient, and V_{th} is the threshold voltage of the underlying transistors. All of the existing parameters in the mentioned formulation considered without variation and so have constant values except measured frequency (F) and threshold voltage (V_{th}).

Extracted V_{th} variation map should be applied in the VPR object's delay and leakage power measurement. FPGA is considered as a grid network, with the same parameter value in each grid. Each grid's size has been considered a CLB and its relevant routing resources.

For applying extracted V_{th} effects on delay, a linear model has been used. Following equation shows the V_{th} variation maps effects on object's delay in FPGA.

$$D_i = D_{i0} + \sum_{\forall j} K.\Delta V_{th,ij},$$

Where D_i is variation-aware delay for object i, D_{i0} is the nominal delay, $V_{th,ij}$ is the threshold voltage variation value in grid j and K is the coefficient.

According to threshold voltage exponential effects on consumed leakage power, a nonlinear modeling has been proposed for applying extracted V_{th} variation map into the CLB's leakage power estimation in placement level and measuring that's shown in the following equation.

$$I_{sub,CLB_i} = I_{sub,CLB_{i,0}}.e^{-K.\Delta V_{th,i}},$$

Where I_{sub,CLB_i} is the leakage power for CLB i after applying extracted V_{th} effects on the nominal CLB leakage power that's specified in the $I_{sub,CLB_{i,0}}$ parameter, $V_{th,i}$ is the threshold voltage variation value in grid i or CLB i and K is the constant coefficient.

B. Leakage Power Estimation Technique

Active and static leakage power for used and unused resources have been estimated in each placement's perturb according to extracted variation map. Due to investigations, routing resource's leakage power can be affected by proposed placement algorithm, which will be analyzed in the next section.

Active leakage power is the consumed leakage one in the mapped and used resources. A mapped resource's leakage power has a great dependency on its input's states. According to active leakage power dependency on input states, a measuring technique has been used for CLB's active leakage power measurement. Each resource's state can be defined with Static Probability for all of its inputs. Static probability for each net is the probability of being high for that net. Netlist's static probability has been measured by ACE tool [14].

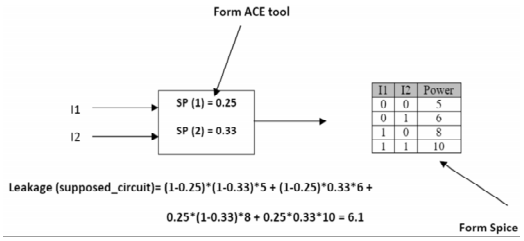

Figure 2. An example of active leakage power measrement

An example in Figure.2 demonstrates active leakage power measuring technique using its input's static probability values. Supposed resource has two inputs with 0.25 and 0.33 static probability values. They have been computed by ACE tool. Supposed resource's leakage power consumption for different input states have been computed and reported in the existing table, mentioned table can be completed by HSpice simulation results.

This method has been used for leakage power consumption measurement in CLBs. After measuring their leakage power, extracted V_{th} variation map effects has been applied into them due to mentioned formulation in the previous section. Against to active leakage power, static leakage power consumption is in the unused and unmapped routing and logical resources just. Measuring their leakage power has a specific flow; number of OFF transistors can be a substitution of their leakage power consumption.

C. Dynamic Power Estimation Technique

Netlist's capacitance for dynamic power consumption measurement hasn't been specified accurately in the placement level. So their capacitance should be estimated by value specified parameters in placement level. In paper [13] an estimation model has been proposed for net's capacitance measuring in placement level. That's mentioned in the following formulation.

$$C_i = f(FO_i, XS_i, YS_i),$$

Where FO_i is the goal parameter, net i capacitance, FO_i is the fan out of net i and XS_i and YS_i are spans of net i in the x- and y-dimensions. Function f is a linear function and the mean error for this model is computed nearly 60%. This model has been used for this paper for proposing a dynamic power optimization placement algorithm beside leakage power optimization.

D. Modified Cost Function Formulation

In this paper, in addition to default parameters, estimated CLB's variation-aware leakage power and estimated net's dynamic power has been considered in the placement cost function. Default parameter in the placement cost function consists of critical path delay optimization and routability improvement. Each of them has specific estimation methods such as Static Timing Analysis (STA) and Congestion controlling methods. That's considerable that in the VPR, $delay - cost$ is the function of net's slack so, for considering the real $delay - cost$, following formulation for cost function has been recommended to optimize the PDP parameter. Estimated variation-aware leakage and dynamic power should be applied into the modified cost function.

$$Modified - Cost - function = \alpha.delay - cost.delay - cost.(CLB - leakage - cost + dynamic - cost) + \beta.congestion - cost,$$

Where $delay - cost$ is the normalized delay cost parameter, $congestion - cost$is the normalized congestion cost parameter, $leakage - cost$ is the normalized leakage power parameter and $dynamic - cost$ is the normalized dynamic parameter. α and β are the constant coefficients. PDP is the main optimization parameter in the proposed cost function.

IV. SIMULATION RESULTS

Simulations have been done for 20 MCNC benchmark with 45-nm BPTM technology. Proposed placement algorithm has been implemented on VPR, PowerModel and ACE tools has been used for leakage and dynamic power estimation. TABLE.I shows the simulation results with utilization rate 60%, different optimization parameters have been reported in the mentioned table.

According to simulation results, PDP as the main optimizing parameter has been improved nearly 7.2% compared with default one. Because of required pre-placement processes and estimations, proposed algorithm run time has been increased nearly 35%. Routing resource's leakage power improvement has been measured very little nearly 3.2% without considering those in the placement algorithm. So placement algorithm that tries to optimize unused CLB's leakage power would optimize unused routing resource's leakage power intrinsically.

All of the benchmark circuits have improvement in PDP parameter, because of proposed placement algorithm. Simulations have been repeated for different utilization rates, Figure.3 shows algorithm effects on 3 different utilization rates: Default VPR utilization more than 92%, utilization rate 75% and real FPGA utilization rate 60%. Simulation results show that there has linear progress in PDP improvement by utilization rate decrement. Utilization rate 60% that's for real FPGAs has better results due to the proposed algorithm.

DPAP algorithm simulation results have been compared with the proposed placement algorithm in this paper. In TABLE.II 3 different placement algorithms have been compared with each other. TPAP is the proposed chip-dependent placement algorithm in this paper, DPAP is the proposed algorithm in paper [11] and finally Pure Total Power-Aware Placement algorithm (PTPAP) is the pure improvements duo to this paper's innovations.

That's considerable that proposed placement algorithm that's named TPAP consists of DPAP with the extra section for leakage power optimizing so PTPAP can show the pure improvements according to my paper's innovations.

TABLE I. SIMULATION RESULTS FOR UTILIZATION RATE 60%

Test Circuit	Delay	total leakage	Dynamic power	Total power	PDP
alu4	-10.5%	3.4%	2.5%	2.8%	2.6%
apex4	-5.8%	28.2%	0.3%	11.4%	11.0%
clma	-7.2%	22.9%	0.4%	9.4%	6.6%
diffeq	-15.2%	6.6%	7.0%	6.8%	2.3%
elliptic	6.3%	6.6%	5.2%	5.7%	15.3%
ex5p	-4.8%	23.7%	5.5%	12.7%	9.8%
misex3	3.5%	28.3%	2.30%	12.7%	17.3%
S38417	-7.9%	8.9%	5.5%	6.8%	3.9%
seq	-14.6%	11.2%	8.5%	9.5%	1.5%
tseng	0.5%	23.3%	2.3%	10.7%	13.6%
apex2	-5.8%	23.1%	4.3%	11.8%	7.4%
bigkey	-3.2%	20.0%	2.6%	9.5%	5.0%
des	-1.6%	14.2%	5.3%	8.8%	6.3%
dsip	0.5%	9.4%	4.7%	6.5%	7.3%
Ex1010	-7.3%	14.3%	3.4%	7.7%	1.5%
frisc	1.4%	13.6%	6.2%	9.1%	9.3%
pdc	-3.9%	26.3%	2.9%	12.2%	6.3%
s298	-5.2%	30.2%	4.2%	14.6%	7.3%
S38584.1	-1.9%	19.3%	6.3%	11.5%	7.3%
spla	-4.9%	15.3%	3.7%	8.3%	3.7%
average	-5.5%	16.3%	4.1%	9.4%	7.2%

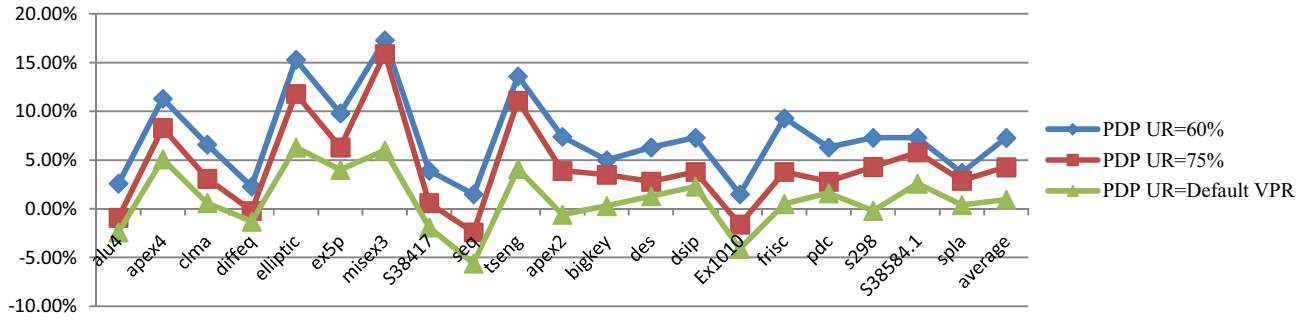

Figure 3. Different utilization rates effects on proposed placement algorithm's improvement

TABLE II. TPAP, DPAP & PTPAP SIMULATION RESULTS

Algorithm	Delay	CLB's leakage	Total leakage	Dynamic power	Total power	PDP
TPAP	-5.5%	47.0%	16.3%	4.2%	9.4%	7.2%
DPAP	-5.6%	9.5%	3.6%	5.8%	3.6%	2.1%
PTPAP	0.1%	37.5%	12.7%	-1.6%	5.8%	5.1%

Pure improvement for PDP parameter has been measured 5.1% compared with default VPR CAD algorithms. It's considerable that our algorithm penalty in critical path delay is nearly the same as the DPAP, it can because of the real values in FPGAs objects delay that have been considered in TPAP against to DPAP. Simulations have been repeated for different V_{th} variation maps to extract proposed algorithm effects on different variation maps. Simulation results in TABLE.III show that proposed algorithm has a little dependency on different variation maps.

Maximum standard deviation for PDP improvement has been measured less than 17%, so proposed algorithm in this paper named chip-dependent algorithm and it can be adaptable with different FPGAs with different variation maps. Another word, proposed algorithm is adaptable with different variation maps so it can be used as the placement algorithm in different chips with different variation maps.

V. CONCLUSION AND FUTURE WORKS

Proposed placement algorithm, TPAP, is the first work to reduce leakage power consumption in FPGAs due to extracted process variation map. According to simulation results proposed algorithm has considerable effects on PDP parameter improvement. In this paper, real FPGAs have been simulated with utilization rate 60% and improvement value for PDP parameter was measured more than 7.2%. Dynamic, active leakage and static leakage power optimization due to TPAP have been considered. But for extracting the pure improvement according to proposed idea a dynamic power-aware placement algorithm is implemented, simulation results show that our proposed innovation that's named PTPAP algorithm has been caused to 5.1% improvement in PDP parameter.

Proposing process variation-aware routing algorithm for routing resources leakage power control can has better results compared with placement algorithm. There can be considered as the future works. "Chip-dependent CAD algorithms" is the most important concept, that's proposed in this paper. FPGA placement algorithm with a chip dependency feature has been analyzed and implemented as one of the samples in the proposed scope. Proposed placement algorithm just includes CLB's leakage power, so there have so many open problems in this scope includes:

- Another chip-dependent CAD algorithms implementation such as chip-dependent routing algorithm.
- Early prediction model for routing resource's leakage power consumption and so applying it in the proposed chip-dependent placement algorithm.
- Distribute variation map extraction to another variation parameters such as L_{eff} and T_{ox}.

All of the mentioned cases as my paper's future work will be caused better results in the process variation aware leakage power optimization techniques.

VI. REFERENCES

[1] D.Chen, J.Cong and P.Pan, "FPGA design automation: A survey," Electronic Design Automation, 2003.

[2] H.Hassan, "Design methodologies and CAD tools for leakage power optimization in FPGAs," PHD thesis, Waterloo University, Canada, 2008.

[3] A.Bsoul, "Reliability and Variation-Aware Placement for Field-Programmable Gate Array," Master Thesis, Queen's University, September 2009.

[4] J. Kao and A. Chandrakasan, "Dual-threshold voltage techniques for low-power digital circuits," IEEE J. Solid-State Circuits, 2000.

[5] S. Bijansky and A. Aziz, "TuneFPGA: Post-silicon tuning of dual-Vdd FPGAs," in Proceedings of the 45th Design Automation Conference, 2008.

[6] A. Kumar and M. Anis, "A leakage-tolerant dual-Vt CAD flow for FPGAs," IEEE Trans. Computer-Aided Design, 2007.

[7] H.Chang, S.S.Sapatnekar, "Full-Chip Analysis of leakage power under process variation, including spatial correlations," Design Automation Conference (DAC), 2005.

[8] A.B.Kahng, S.Muddu and P.Sharma, "Detailed placement for leakage reduction using systematic through-pitch variation," ISLPED, 2007.

[9] Y. Lin, M. Hutton, and L. He, "Placement and timing for FPGAs considering variations," in Proceedings of the International Conference on Field Programmable Logic and Applications, 2006.

[10] L. Cheng, J. Xiong, L. He, and M. Hutton, "FPGA Performance Optimization via Chipwise Placement Considering Process Variations," in Proceedings of the International Conference on Field Programmable Logic and Applications, pp. 1-6, Aug. 2006.

[11]] S.Gupta, J.Anderson, L.Farragher and Q.Wang, "CAD Techniques for Power Optimization in Virtex-5 FPGAs," IEEE Custom Integrated Circuits Conference (CICC), 2007.

[12] S.R.Sarangi, B.Greskamp, R.Teodorescu, J.Nakano, A.Tiwari and J.Torrellas, "VARIUS: A Model of Process Variation and Resulting Timing Errors for Micro- architectures," IEEE Transactions on Semiconductor Manufacturing, VOL. 21, NO. 1, February 2008.

[13] V. Betz and J. Rose, "VPR: A New Packing, Placement and Routing Tool for FPGA Research," in Proceedings of the 7th International Workshop on Field-Programmable Logic and Applications, pp. 213-222, Sep. 1997.

[14] N. C. K. Choy, S. Chin, C. Lee, K. Poon, J. Lamoureux, A. Yan, S. Wilton, S.-S. Ang, and W. Luk, "Power Modeling for FPGAs." http://www.ece.ubc.ca/~stevew/powermodel.html