SIMULATION OF SIX-LEVEL DIODE-CLAMPED MULTILEVEL INVERTER USING PWM MODULATION IN MATLAB AND PSIM

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ABSTRACT

In this study, the PWM switching technique in six-level diode-clamped multilevel inverter (DCMLI) has been implemented in PSIM and Matlab/Simulink software packages. The DCMLI power circuit is drawn using the PSIM software package. The switching pattern generated using Matlab/Simulink file is linked with an inverter circuit through the Simcoupler module.

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1].

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three-level inverter, also known as a "neutral-clamped" inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The waveform obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used [2].

The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes [3]. Multilevel PWM has lower *dV/dt* than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. [4]

II. DIODE-CLAMPED MULTILEVEL INVERTER

An m-level diode-clamp inverter typically consists of m - 1 capacitors on the dc bus and produces m levels of the phase voltage. A three-phase six-level diode-clamped inverter is shown in Figure 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition *1* means the switch is on, and *0* means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg *a* are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$). Table 1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series. For a six-level inverter, a set of five switches is on at any given time [5].

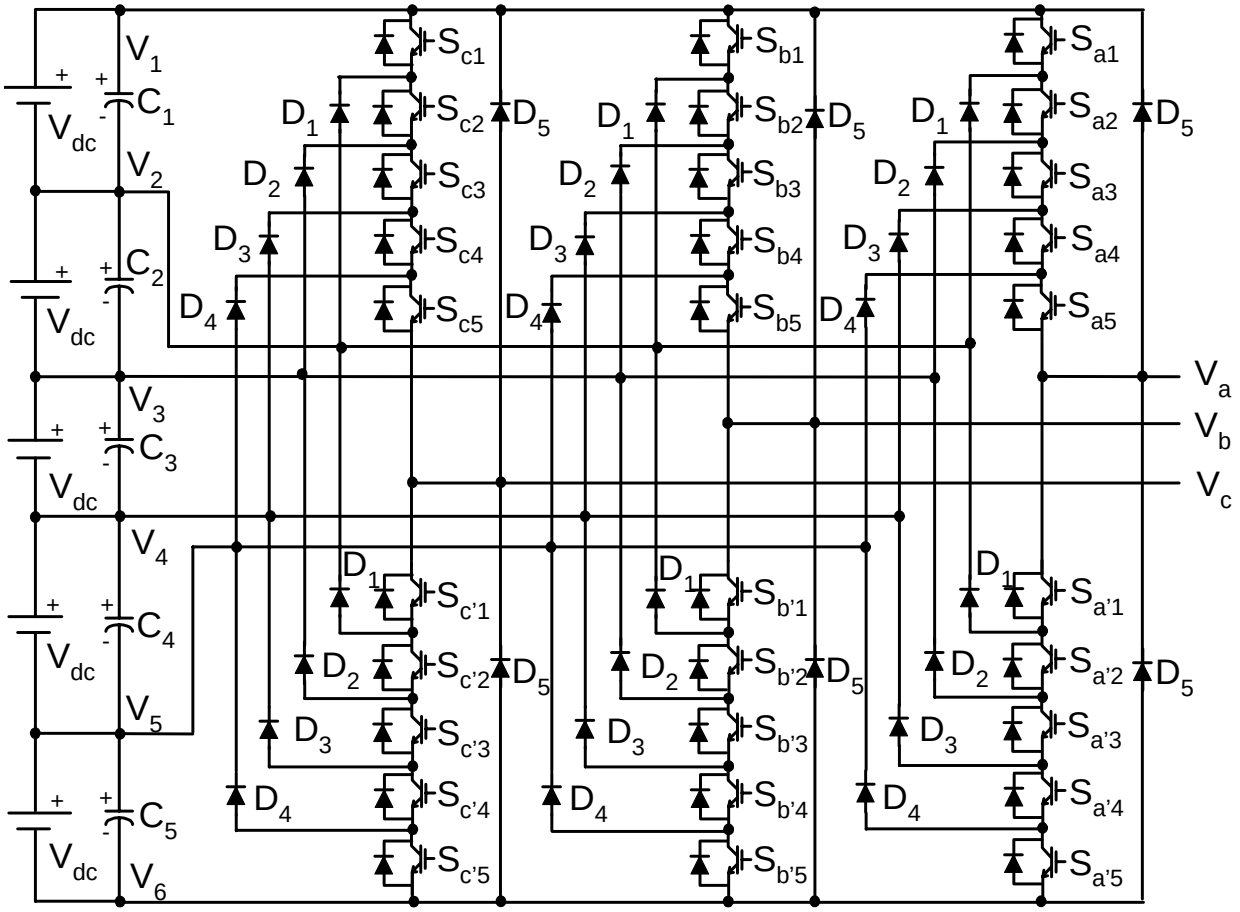

Figure 1. A three-phase six-level diode-clamped multilevel inverter.

Table 1. Six-level diode-clamped multilevel inverter voltage levels and corresponding switch states.

Voltage V_{a0}	Switch State									
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$	$S_{a'5}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

Figure 2 shows one of the three line-line output voltage waveforms for a six-level multilevel inverter. The line voltage V_{ab} consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is an 11-level staircase waveform. This means that an *m*-level diode-clamped inverter has an *m*-level output phase voltage and a (2*m*-1)-level output line voltage.

Although each active switching device is required to block only a voltage level of V_{dc}, the clamping diodes require different ratings for reverse voltage blocking. Using phase *a* as an example, when all the lower switches $S_{a'1}$ through $S_{a'5}$ are turned on, D_4 must block four voltage levels, or $4V_{dc}$. Similarly, D_3 must block $3V_{dc}$, D_2 must block $2V_{dc}$, and D_1 must block V_{dc}. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require *n* diodes in series; consequently, the number of diodes required for each phase would be $(m\text{-}1) \times (m\text{-}2)$. Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped inverter.

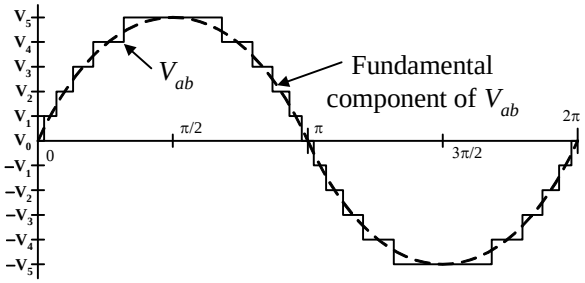

Figure 2. Line voltage waveform for a six-level DCMLI.

DCMLI has the following advantages and disadvantages.

Advantages:

(1) DC-link capacitors are common to three phases.
(2) Switching frequency can be low.
(3) Reactive current and negative-phase-sequence current can be controlled.

Disadvantages:

(1) Many diodes are used for clamping.
(2) Many diodes make physical layout difficult, e.g. increase stray inductance [6].

III. PWM METHOD for SIX-LEVEL DCMLI

Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel inverters. Previous authors have extended several different two-level multilevel carrier-based PWM techniques as a means for controlling the active devices in a multilevel inverter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. Figure 3 shows the principle of the PWM method for a multilevel inverter. The PWM method generates switching signals by comparing one sinusoidal signal and five triangular wave signals, which have DC bias for each voltage level, as shown in Figure 3. In this modulation method, the duty cycle of each voltage level is determined by the ratio of the sine wave amplitude to the triangular carrier signal amplitude. That is, the sine wave amplitude determines modulation factor, and one modulation factor generates only one pattern of output pulse width [7].

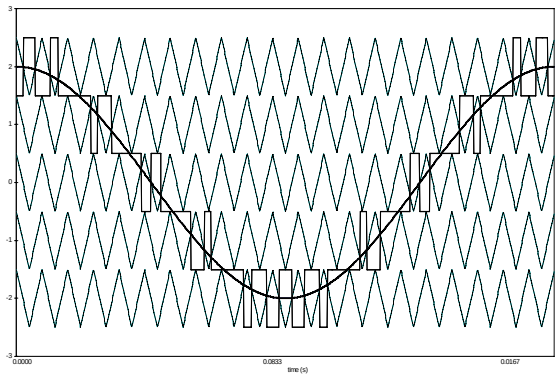

Figure 3. PWM modulation of six-level DCMLI.

IV. SIMULATION RESULTS

Matlab/Simulink and PSIM software packages were linked and run concurrently to perform this software implementation. Blocks in Matlab/Simulink generates the PWM switching pattern technique. SimCoupler module provides interface between Matlab/Simulink and PSIM software packages for co-simulation. The SimCoupler Module is an add-on module to the PSIM software [8]. It provides interface between PSIM and Matlab/Simulink for co-simulation, so that part of a system can be implemented and simulated in PSIM, and the rest in Matlab/Simulink.

The SimCoupler Module enables Matlab/Simulink users to implement and simulate power circuits in their original circuit form, thus greatly shortening the time to set up and simulate a system, which includes electric circuits and motor drives. First, the DCMLI power circuit is simulated in PSIM, and the PWM control in Matlab/Simulink. The SimCoupler Module is straightforward and easy to use with minimum input from users. The simulation parameters are shown in Table 2.

Table 2. Simulation parameters.

Switching frequency	2000 Hz
Frequency	50 Hz
DC Bus voltage ($5xV_{DC}$)	120 V
Load Rs	20 ohm
Load Ls	0.00139 H

Using PWM modulation explained above, simulations have been conducted to verify the effectiveness of the algorithm. PWM modulation in Matlab Simulink block diagrams and the six-level DCMLI power circuit in PSIM are shown in Figure 4 and Figure 5, respectively. The gate signals of six-level DCMLI power circuit are produced by triangle and sinusoidal comparison in Matlab/Simulink blocks. The interface is done through link nodes in PSIM, and the SimCoupler model block in Simulink. With the SimCoupler Module, one can make full use of PSIM's capability in Power simulation and Matlab/Simulink capability in control simulation in a complementary way.

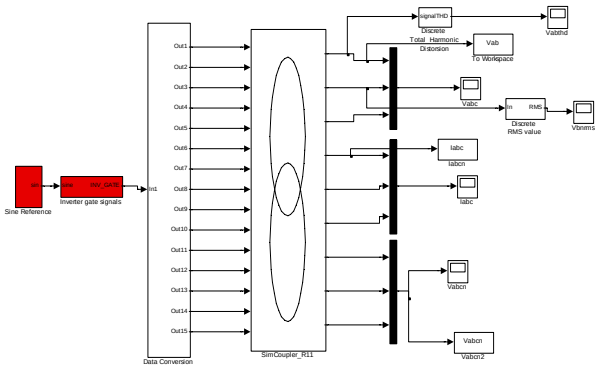

Figure 4. PWM Modulation in Matlab Simulink.

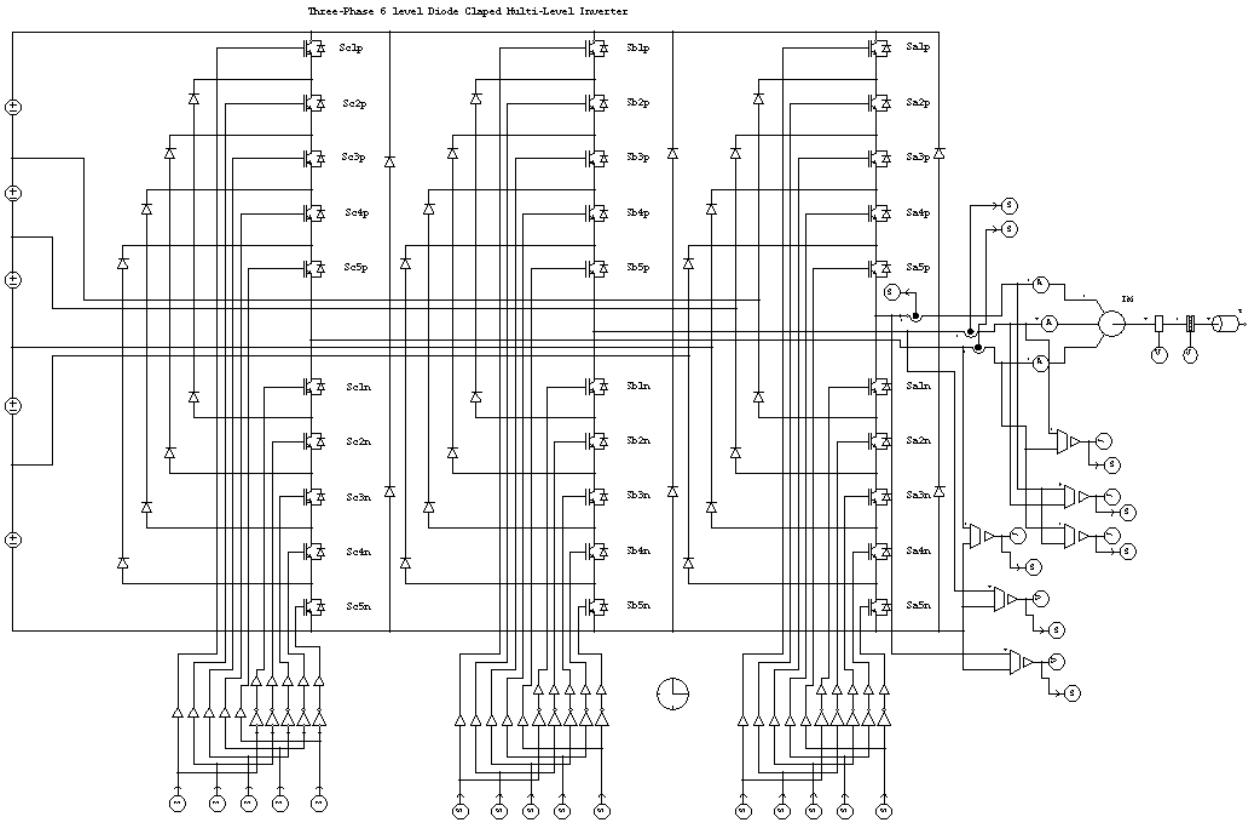

Figure 5. Six-level DCMLI power circuit in PSIM.

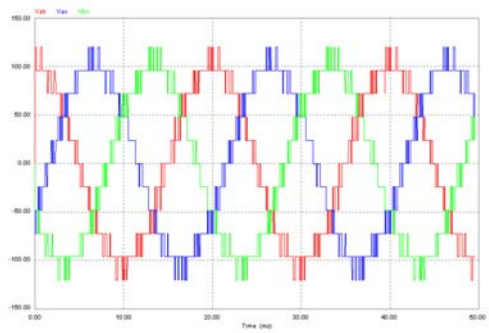

Figure 6. Three-phase line voltage waveforms.

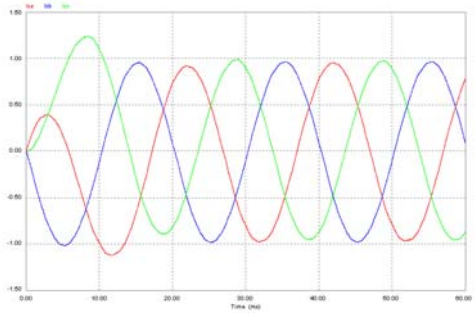

Figure 7. Three-phase line current waveforms.

Three-phase line voltages and currents waveforms of the induction motor load of six-level DCMLI are shown in Figure 6 and Figure 7 respectively. Three-phase currents are in sinusoidal shape and have very low THD level in lower switching frequency. In order to understand line-to-line voltage waveform, both phase voltages and producing line voltage waveforms are given in Figure 8. In order to get total harmonic distortion (THD) level of the waveform, a fast Fourier transform (FFT) is applied to obtain the spectrum of the output voltage, which is shown in Figure 9. The THD of the output voltage is 13%, which shows that lower order harmonics have been eliminated.

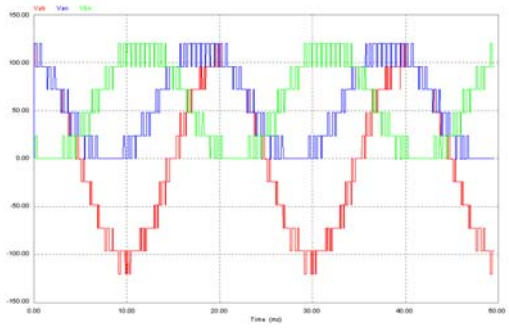

Figure 8. Line and phase voltage waveforms.

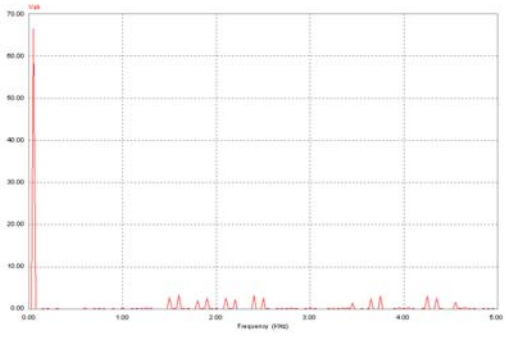

Figure 9. THD spectrum of the output voltage.

V. CONCLUSION

This paper has been presented a six-level diode-clamped multilevel inverter for harmonic elimination in both Psim and Matlab/Simulink software packages. The interface is done through link nodes in PSIM, and the SimCoupler model block in Simulink. With the SimCoupler Module, one can make full use of PSIM's capability in Power simulation and Matlab/Simulink capability in control simulation in a complementary way. Using multilevel inverters not only solves harmonics and EMI problems, but also avoids possible high frequency switching induced motor failures.

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