A Low Power, Low Noise Neural Amplifier, Using Bulk-driven Cascode Current Mirror Load

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Abstract

Multi-channel neural recording amplification and receiving systems are an inseparable component in the treatment and investigation process of human nervous system. Due to the low amplitude of neural signal range and high number of neural recording channels, these systems should have low noise and low power consumption. In this work, a new telescopic transconductance operational amplifier is presented using the current source launched via the body (bulk-driven cascade current mirror (BDCCM)). The output swing of this amplifier has a considerable increase compared to the other telescopic transconductance amplifiers. The neural amplifier designed by the proposed transconductance amplifier has a high output swing as well as low noise efficiency factor, noise, and power consumption.
The proposed amplifier has a power consumption of 6.9 µw, effective input noise of 2.45 $\mu V / \sqrt{hz}$, noise efficiency factor of 2.2, and gain of 38.9 dB in bandwidth of 0.089Hz-7kHz. This amplifier is simulated in the 180 nm MOSFET process; its output swing and power supply voltages are 0.7v and ±0.9v, respectively.

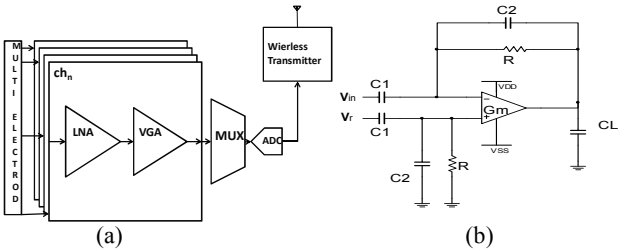
1. Introduction

Investigating neural signals, in the human body, for the purpose of diagnosis, treatment, and modification of neurological diseases, requires long-term displaying and monitoring of signals from a large number of nervous system cells. This issue has become possible in recent years considering the development in the field of electronics in terms of miniaturizing electronic components and reducing power consumption and noise. Neural signals with the voltage amplitude of 50µV-10mV and frequency amplitude of 1mHz-10kHz can be received from the skin surface[1]. The noises which are stablished during the amplification process of these signals include flicker noise, thermal noise and background noise, in which flicker noise is the dominant one because of the low operating frequency. The background noise usually varies between 10 and 30µV, depending on the installation location of electrode and distance to the neuron [2].

Because of current passing through the resistance between the electrode, electrolyte, and neuron, a rectified signal (DC) of about 1v is created on the input signal. This DC signal must be removed or stabilized due to the saturation of the amplifier. Therefore, in most cases, the neural signal is connected to the neural amplifier by AC coupling or DC stabilization [3][4]. In AC coupling, due to the low-frequency of neural signals for reaching the low cut-off frequency close to DC, a large input capacitor is selected for the amplifier which increases the surface area occupied by the amplifier.

Fig.1 (a) shows the structure of a multi-channel neural signal recorder. There is a low noise amplifier (LNA) in each channel. Fig.1 (b) shows a closed-loop low-noise amplifier which is composed of an operational transconductance amplifier (OTA), a high-pass filter, and a low-pass filter.

So far, different structures have been proposed for the operational transconductance amplifiers in order to increase the open-loop gain and decrease noise, power consumption, and the occupied surface area. Symmetrical current mirror and Miller operational transconductance amplifiers are widely used in low-noise neural signals amplifiers [4][5][6]. These amplifiers have low-noise and high-output swing; however, since they are two stage amplifiers, their power consumption is also high.



(a) (b)

Fig. 1. (a) Structure of a system for recording neural signals; b) An amplifier of neural signals [5]

The folded cascode ooperational transconductance amplifiers with high input and output voltage swing have been also used in [7][8]. But, they have greater noise and higher power consumption, since they have a large number of transistors. In order to improve the power consumption and reduce the noise in the amplifiers, fully differential self-bias OTA was used in [9]. In [2][10][11], telescopic Cascode amplifiers have been used with the lowest noise and power consumption among other structures of operational transconductance amplifiers. Since the telescopic Cascode amplifiers limit the output swing amplitude, they have been used in the design of conventional operational transconductance amplifiers less frequently. However, since the input neural signal has low swing amplitude, these amplifiers can be utilized, using some methods to improve their output voltage swing. In [12], bulk driven (BD) method was used in the input transistors in order to improve the output swing and reduce the voltage level in the power supply. Using this method increases the input noise and decreases the amplifier gain. In [13], the dynamic threshold was used in the input transistors. Although this method reduced the voltage level in the power

supply and increased the output swing, it was only used in power supply with the voltage level below 0.8V.

In this paper, in order to increase the output swing, BD method is used in the current mirror source of telescopic Cascode amplifier load, which significantly increases the output swing of the amplifier and, at the same time, prevents the input noise from increasing.

In Section 2, besides examining the bulk-driven current source, design of the amplifier as well as the reasons for noise reduction will be explained. In Section 3, results of simulation are presented, while Section 4 presents the discussion and conclusion.

2. Bulk-driven current mirror source

One way to increase the output swing is to reduce the voltage drop on an amplifier load. The gate-driven cascode current mirror source (GDCCM) or modified cascode mirror load is used in the load of a single-ended telescope amplifiers. These loads limit the maximum output swing; therefore, application of single-stage telescopic amplifiers has some limitations [6]. Using BD method in the bulk-driven Cascode current mirror source (BDCCM) reduces the transistors' threshold voltage and their drain source voltage. In the case of using these current sources in the telescopic amplifiers, the output swing would be increased.

In Fig. 2(a) and Fig.2 (b), the BDCCM and GDCCM are indicated. According to [14], voltage and output resistance of a BDCCM are equal to:

$$\begin{aligned} V_{out} &= V_{ds6}(sat) + V_{ds8}(sat) \\ V_{ds6} &= [I - (g_{m6} + g_{mb6})V_{GS6}]r_{o6} \\ r_{out} &\approx r_{o6}r_{o8}(g_{m6} + g_{mb6}) \end{aligned} \quad (1)$$

While voltage and output resistance of a GDCCM are equal to:

$$\begin{aligned} V_{out} &= V_{ds6}(sat) + V_{ds8}(sat) \\ V_{ds6} &= [I - g_{m6}V_{GS6}]r_{o6} \\ r_{out} &\approx r_{o6}r_{o8}g_{m6} \end{aligned} \quad (2)$$

Decreasing V_{ds6} in (1), compared to (2), increases the output voltage swing in BDCCM compared to GDCCM.

Unlike the use of BD in the input transistors of the amplifiers which increases the noise and decreases the gain [12], using BDCCM in the amplifier loads will result in the lack of increase in noise and decrease in gain.

Fig. 3 shows the BDCCM circuit and its noise sources. The effective noise voltage in this circuit is equal to:

$$V^2_n = V^2_{n,\frac{1}{f}} + V^2_{n,th} \quad (3)$$

$$V^2_n = \frac{16kT\gamma g_m^2}{3} + \frac{4K_f g_m^2}{Coxwlf} \quad (4)$$

Considering the fact that the amount of noise in GDCCM current source is also equal to Relations (3) and (4), it can be concluded that, in case of using BDCCM in an amplifier load, the input noise of the amplifier will not be increased.

3. Amplifier Design

Fig. 4(a) shows a conventional closed-loop neural signal amplifier[5]. Fig. 4(b) demonstrates the proposed operational transconductance amplifier used in the neural signal amplifier. In Fig. 4(a), capacitors C1 and C2 along with transistors Ma-Md, which have been used as resistance, will produce the gain and low cut-off frequency for the amplifier. Gain as well as high and low cut-off frequencies are respectively equal to:

$$Av = \frac{C1}{C2} \quad (5)$$

$$f_l = \frac{1}{2\pi RC_2 \times C_{in}} \quad (6)$$

$$f_H = \frac{Gout}{2\pi C_l} \quad (7)$$

Where C_L, C_{in}, and R are load capacitance, input capacitance of the amplifier, and equivalent resistance of M_a-M_b respectively.

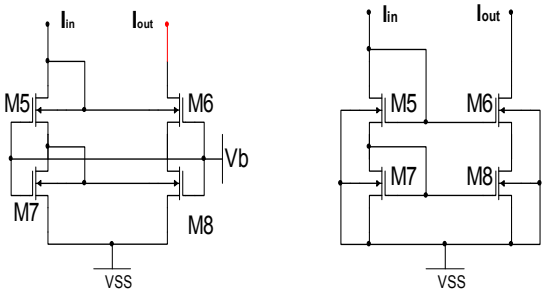


Fig. 2. (a) BDCCM. (b) GDCCM[14]

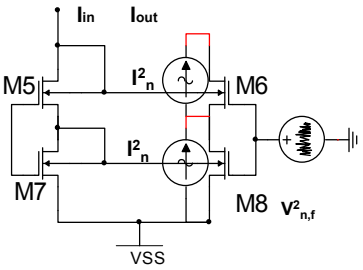


Fig. 3. Sources of noise in BDCCM circuit

In the proposed operational transconductance amplifier, transistors M_1-M_4 are considered to be input cascode transistors, where input signal is applied to M_1,M_2. Transistors M_5-M_8 are the bulk-driven cascode current mirror source that have been used as an amplifier load. Transistors M_9-M_{10} are the amplifier's current source and M_{11}-M_{12} transistors are load bias circuit. According to Fig. 4 (a), the closed-loop input noise for the amplifier is obtained according to (8):

$$V_{n,in,eff} = \int_{fl}^{fH} \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 V^2_{n,in,OTA}.df \quad (8)$$

Where f_H and f_l are the high and low cut-off frequencies respectively and C_{in} is the OTA input capacitance. $V^2_{n,in,OTA}$ is the noise of the operational transconductance amplifier which is obtained according to (9), (10), and (11) [2].

$$V^2_{n,in,OTA} = V^2_{n,in,th} + V^2_{n,in,\frac{1}{f}} \quad (9)$$

$$V^2_{n,in,\frac{1}{f}} = \frac{K_f}{Cox(wl)f} + \frac{K_f}{Cox(wl)f}\frac{g_{m,load}^2}{g_{m,in}^2} \quad (10)$$

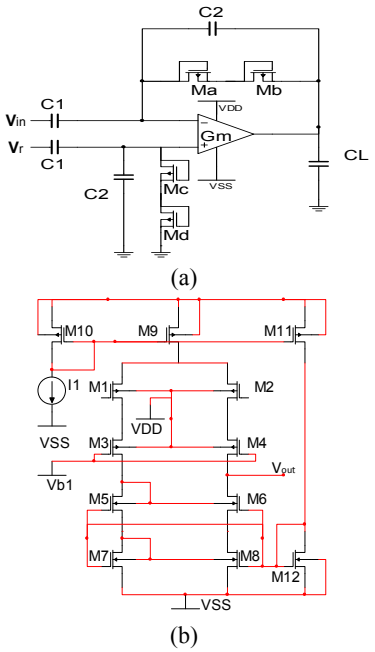


Fig.4. (a) Neural signal amplifier[5] (b) The proposed operational transconductance amplifier

$$V^2_{in,th} = \frac{4kT\gamma}{g_{m,in}} + \frac{4kT\gamma {g_{m,load}}^2}{{g_{m,in}}^2} \qquad (11)$$

where K is the Boltzmann constant, Kf is the coefficient of technology that is less for PMOS compared to that for NMOS, Cox is the gate oxide capacitance, f is frequency, and W and L are the length and width of each transistor respectively. [2].

As shown by (8), the amplifier's input noise is composed of noise in the capacitive feedback network plus the noise in the operational transconductance amplifier; these two parts should be minimized in order to design a low-noise neural signal amplifier. According to (9), the input noise in the operational transconductance amplifier is composed of thermal and flicker noises. The value of flicker noise is equal to:

$$V_{n,in,\frac{1}{f}} = \frac{2K_f}{Cox(wL)_{1,2}f} + \frac{2K_f}{Cox(wL)_{3,4}}\frac{{g_{m3,4}}^2}{{g_{m1,2}}^2} + \frac{2K_f}{Cox(wL)_{3,4}}\frac{{g_{m5,6}}^2}{{g_{m1,2}}^2} + \frac{2K_f}{Cox(wL)_{7,8}}\frac{{g_{m7,8}}^2}{{g_{m1,2}}^2} \qquad (12)$$

To minimize the flicker noise, the PMOS transistors have been used in input amplifier, since Kf is smaller in PMOS. Also, by designing the amplifier so that gm1,2>gm3-8, flicker noise in the input level dominates and, by selecting a large value of (W×L)1,2, the flicker noise of the amplifier is minimized. According to (11), the thermal noise in the operational transconductance amplifier is equal to:

$$V_{n,in,th} = 8kT\gamma\left(\frac{1}{gm_{1,2}} + \frac{{gm_{3,4}}^2}{{gm_{1,2}}^2} + \frac{{gm_{5,6}}^2}{{g_{m1,2}}^2} + \frac{{gm_{7,8}}^2}{{g_{m1,2}}^2}\right) \qquad (13)$$

Since gm1,2>gm3-4, the thermal noise in the operational transconductance amplifier is also minimized. Increasing gm of the input transistors in order to minimize the effective input noise is possible through increasing the current in these transistors which also increases the power consumption. In order to obtain the highest amount of gm for low current, the input transistors are biased in the subthershold region. In this area, the gm/I_D ratio has the highest value among the other areas of MOSFET transistor bias. The specific current (Is) of the subthershold region is equal to:

$$I_s = \frac{2\eta\mu CoxwU_T^{\ 2}}{L} \qquad (14)$$

Where η is related to the subthershold region and U_T is the thermal voltage. The value of the ratio of the drain current (Id) in each transistor to Is is equal to Ic, i.e. the reverse coefficient. In case Ic<0.1, the transistor is biased in the subthershold region. To satisfy Ic<0.1, a large value must be selected for W/L ratio of the input transistors in (14). Here, Ic equals 0.074. Information regarding length, width, current, and bias area of each transistor is presented in Table 1.

According to (8), to minimize the input noise of the neural signal amplifier, the noise in capacitive network should also be minimized which is possible by selecting Cin,C2<< C1. Selecting a large value for C1 capacitance increases the surface area occupied by the amplifier. To reduce the value of the C1 capacitor, a small value should be selected for C2 capacitance. The value of C2 capacitance is obtained according to (6) by considering the required low cut-off frequency which is lower than 1 mHz. In order to reduce the value of C2, the resistance R should be selected as large as possible; therefore, by selecting the W/L ratio of the Ma-Md transistors as 0.3/30 µm, the values of C1 and C2 are selected as 150fF and 15pF respectively. The amplifier gain is considered to be 100, according to (5).

By using a BDCCM in the proposed amplifier load for maximizing the output swing amplitude, the W/L ratio of transistors M5-M8 is selected such that the flicker noise is minimized. The output voltage swing equals 0.7v at THD<1%. This amplifier amplifies a wide range of neural signals created in the body.

4. Simulation Results

According to the above-mentioned discussion, finally, the proposed neural signal amplifier was simulated by Hspice using the measurements presented in Table 1 according to Fig. 4(a) and Fig. 4(b). The output swing diagram, Bode diagram, and its input noise are shown in Fig. 5 and compared with other neural signal amplifiers with single-stage telescope Cascode structure in Table 2 as well as with two-stage neural signal amplifier in Table 3.

5. Conclusions

In the conducted study, an innovative neural signal amplifier with bulk-driven cascode current mirror load (BDCCM) was proposed. This amplifier had a gain equal to 38.9 dB within the 0.089Hz-7kHz frequency band, power consumption of 6.9µw, effective input noise of 2.45$\frac{\mu V}{\sqrt{Hz}}$, and output voltage swing of 0.7V in the power supply of ±0.9v. In comparison with other neural signal amplifiers with single-stage telescopic Casocode structure, the proposed amplifier increased the output swing significantly.

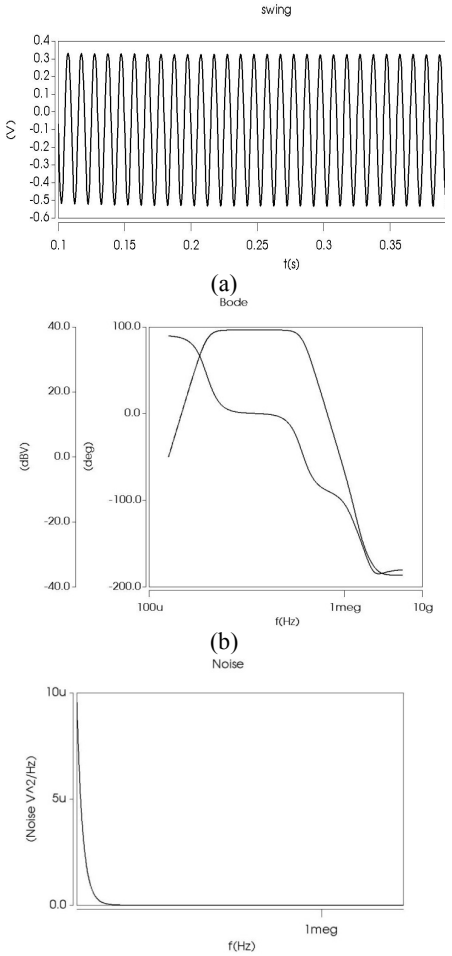


Fig. 5. (a) Output swing diagram (b) Bode diagram (c) Input noise diagram

Table 1. Transistors Information

	W(μm)	L(μm)	Region	I(μA)
M1,M2	200	1	Subthreshold	1.7
M3,M4	30	2	Saturation	1.7
M5,M6	9.8	9	Saturation	1.7
M7,M8	22	2	Saturation	1.7
M9,M10	16	2	Saturation	3.4
Ma-Md	0.3	30		

Table 2 Performance comparison of proposed circuit with single stage amplifier

Parameter	**[10]**	**[2]**	**This work**
CMOS technology(μm)	0.35	0.13	0.18
Gain (dB)	38.1	37	38.9
Band with(Hz)	8.54k	5-7k	0.089-7 k
Input Referred noise(μV)	13.3	5.5	2.45
NEF	7.87	2.58	2.2
Supply Voltage(v)	3	1.5	±0.9
Power consumption(μw)	6	1.5	6.9
Load capacitance(pf)	-	-	10
Input capacitance(pf)	1.6	10	15
Max output swing(v) withTHD<1%	0.192	0.028	0.7
Max input swing(mv)	2.4	0.4	8
OTA Topology	Telescopic cascode	Telescopic cascode	Telescopic cascode

Table 3 Performance comparison of proposed circuit with two stage amplifier

Parameter	[5]	[16]	[15]	This work
CMOS technology(μm)	1.5	0.6	0.13	0.18
Gain (dB)	39.8	39.4	40	38.9
Band with(Hz)	0.025-7.2	0.36-1.3k	0.05-10.5k	0.089-7 k
Input Referred noise(μV)	2.2	3.07	2.7	2.45
NEF	4	3.9	2.9	2.2
Supply Voltage(v)	±2.5	2.75	1	±0.9
Power consumption(μw)	80	2.4	12.1	6.9
Load capacitance(pf)	17	11	-	10
Input capacitance(pf)	20	20	18	15
Max output swing(v) with THD<1%	1.6	0.933	0.1	0.7
Max input swing(mv)	16.7p-p	10 p-p	1 p-p	8
OTA Topology	Symmetric current mirror	Symmetric current mirror	Complementary-input closed-loop amplifier	Telescopic cascode
Stage of OTA	2	2	2	1

6. References

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