EFFECTS OF CHARGE INJECTION ERROR ON SWITCHED CURRENT DIVIDER CIRCUITS.

E.GARNIER, PH. ROUX and Ph.MARCHEGAY.

Laboratoire IXL – C.N.R.S. UMR 5818 – E.N.S.E.I.R.B
Université Bordeaux I
351, cours de la libération – 33405 Talence – France
Tél : 33 (0)5 56 84 26 32 – Fax : 33 (0)5 56 37 15 45
E mail : mailto:garnier@enseirb.fr

Abstract

This paper presents the effects of charge injection error on switched-current Divider Circuits. Algorithmic structures of current dividers are presented and the charge injection error is evaluated at each iteration of the Algorithm. Therefore, the current final value is estimated. So, compensated methods to cancel this error are proposed.

I.- INTRODUCTION

The circuit technology used in portable electronic systems has been changing from the conventional analog circuit technology to a mixed-signal technology.
"Low-voltage/low power circuit" design like Digital to Analog Converters (DAC's) is strongly needed for both analog to digital circuits to increase operation time and decrease occupied die area and consumption [11]. Therefore, overall system cost can be reduced significantly if both analog and digital circuits can use the same supply-voltage and the analog circuits can be fabricated using the low cost digital CMOS process [10].

A class of analog circuits wherein current rather than voltage is conveyed has been received considerable attention [12]. With SI (switched-current) technique, no highly-linear capacitance is needed, the same low-cost digital CMOS process for the digital portion of mixed signal circuits can also be used for the analog part.

The need for small yet accurate DAC's is becoming increasingly important. Ideally, the DAC must be compatible with presently available digital VLSI processes like S.I technique and consequently must not rely on closely matched devices or high performance analog components.
When current is used as the active parameter, the need of matched signals implies a need for matched currents. Typically though, matched currents are generated using current mirrors which depend on good device matching [1], [2]. To avoid this device parameter dependence, alternative copying sequence to resolve the matching problem of the basic divider are used which are algorithmic structures [6], [7], [8].

Many authors proposed different structures as Robert and al. divider [6], Wey and Krishman structure [7] and Wang and Wey circuit [8]. But the accuracy of these dividers is limited by clock feedthrough error effects.

So this paper presents the effects of charge injection error on switched-current divider circuits and proposes, for each structure, adapted compensated methods to minimize this error and to obtain a greater accuracy.

At first, in the second section, the different structures of algorithmic S.I divider circuits are analyzed. In the next section, the clock feedthrough error (CFT) effects and the test circuit are presented. Section 4, the evolution of CFT error, for each Algorithmic structure, is analyzed and compensated methods are proposed. Finally, a concluding remark is given in section 5.

II.- CURRENT DIVIDER CIRCUITS.

The principle of current division is often used in SI D/A conversion. Such conversion generally requires many successive divisions by two which must be very accurate. Due to mismatch, an accuracy of few percent is very hard to achieve for a DAC's circuit, which limits the number of bits to be converted [1], [2] .

So the use of Algorithmic dividers by two allow to achieve a very high accuracy [5], [4]. Robert and al [6] proposed the first algorithmic current divider which is shown in figure 1.

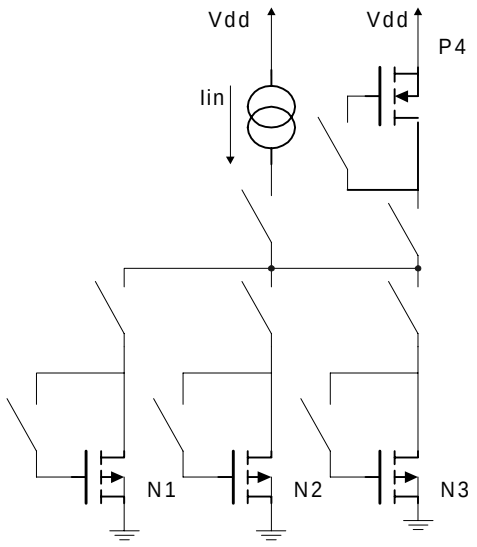

Fig-1: basic Algorithmic current divider.

The number of iterations necessary to obtain half the current with certain accuracy depends on the mismatch of transistors N_2 and N_3. Each iteration takes three clock cycles, as illustrated below.

First iteration: a- $I_{in} \rightarrow N_2$ and N_3
b- $N_2 \rightarrow P_4$
c- P_4 and $N_3 \rightarrow N_1$

Other iterations: a- I_{in} and $N_1 \rightarrow N_2$ and N_3
b- $N_2 \rightarrow P_4$
c- P_4 and $N_3 \rightarrow N_1$

If α_2 and α_3 are the mismatch factors of the transistors N_2 and N_3, respectively, the mismatch ratio γ is equal to $((\alpha_3/\alpha_2)-1)$, $I_2 = \alpha_2 I_{in}$ and $I_3 = \alpha_3 I_{in}$.
According to the current copying sequence, the current held in N_3 at the end of the first cycle of the k-th iteration, I_{3k}, is expressed as [7].

$$I_{3k} = \frac{Iin}{2}\left[1+(-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right]$$

The error due to mismatch decreases rapidly as k increases and authors [6] show that an accuracy of 0.1% can be achieved by taking only three iterations for γ = 20%.
But the NMOS copier proposed stores only a positive current, hence the divider functions properly only when $I_2 > I_3$.
Because the transistor mismatch is generally unknown in advance, this structure could be used, only with biased S.I cells. An alternative structure with the same algorithm was proposed by Wey and al.[7] where the NMOS copier has been replaced by a CMOS stage as illustrated in figure 2

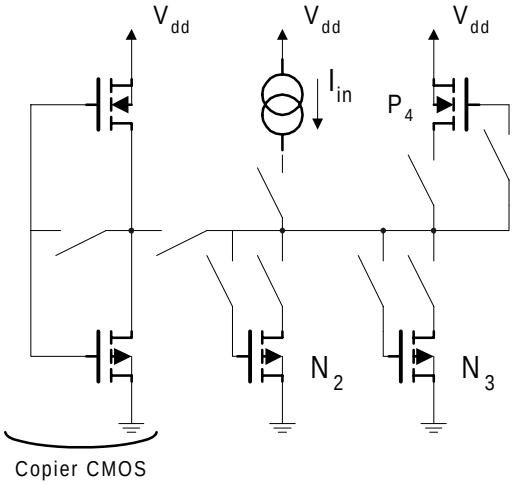

Fig-2: CMOS Algorithmic current divider.

So, N_2, N_3 and P_4 stages can be unbiased cells.
To eliminate the CMOS stage Wang and al. [8] proposed a new structure realized entirely with unbiased cells (figure 3).

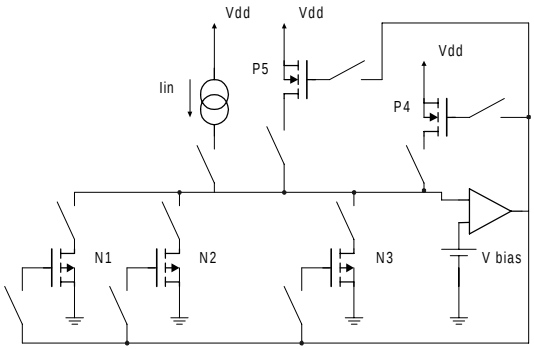

Fig-3: Wang and al. divider.

The copying sequences between N_2 and N_3 are then illustrated below:

First iteration: a- $I_{in} \rightarrow N_1$
b- $N_1 \rightarrow P_4$
c- $N_1 \rightarrow P_5$

Others iterations: a- $P_4 \rightarrow N_2$ and N_3
b- P_5 and $N_3 \rightarrow N_1$
c- N_1 and $N_2 \rightarrow P_4$

The current is held in N_1 during the first cycle from the third iteration.
This structure presents a lower occupied area than the other structures and a very low power consumption, to the detriment of a more complex digital part.

So with a lower occupied die area and a more complex copying sequence, it is possible to obtain a very accurate current divider by two almost insensitive to the mismatch.

III.- LIMITATIONS.

A current matching circuit's resolution is limited, also, by both systematic and random errors.
Ideally through careful design, the systematic errors can be reduced to acceptable levels, leaving only the random errors to determine the circuit's fundamental performance limitations. In current matching circuits there are two primary sources of systematic errors, the transistor's finite output resistance r_0 and charge injection from switches [3].

To increase r_0, cascoded devices or a single long-channel device can be used.
The second source of systematic error is associated with the charge injection from the MOS switches. Various authors have investigated the nature of charge injection problem itself [14], [15], and various solutions have been proposed [9], [10]. The simplest consists in increasing the hold capacitor with a decrease of maximum frequency running.

So it is interesting to know the evolution of the CFT error during each iteration of the various structures in order to propose the most adapted method to compensate it. To validate the study of the effects of CFT error, simulations under cadence environment with CMOS 0.6 µm AMS technology were done. The cells (biased or unbiased) used for these simulations have a cascoded stage associated to the hold transistor to increase r_0 and no hold capacitor is added in order that CFT error is sufficient. Therefore its effects are more obvious.

IV.- EVOLUTION OF THE CFT ERROR

In current matching circuits, charge injection produces an error voltage δ_v on the gate capacitors of memory transistors which leads to an error current δ_I in the memorizing transistors. For a fixed process, the error voltage is dependent on the voltage between switch's channel and ground at turn off and may be approximated as:

$$\delta_v = mVg + b \qquad (1)$$

Where m and b are constant dependent on layout, processing and switching waveforms.
An input current I_{in} will, for each of the n-channel devices, lead to a gate voltage V_{gn} of:

$$V_{gn} = \sqrt{\frac{I_{dn0}}{Kn\frac{w}{L}}} + |VTn| \qquad (2)$$

Where $K_n = \frac{\mu nCox}{2}$, V_{Tn} is the threshold voltage of each of the n-channel devices, I_{dn0} is the drain current of memory transistor and $\frac{w}{L}$ is the NMOS transistor's sizes

$I_{dn0} = I_B + \frac{Iin}{2}$ for biased cells.

And $I_{dn0} = \frac{Iin}{2}$ for unbiased cells.

Due to charge injection though, after turn off, V_{gn} is modified and becomes:

$$V'_{gn} = V_{gn} + mV_{gn} + b \qquad (3)$$

Consequently, the current held changes to:

$$I'_{dn} = I_{dn_0} + Kn\frac{w}{L}(mVgsn+b)[(mVgsn+b)+2(Vgsn-V_{Tn})] \quad (4)$$

For each of the n-channel devices, the error $\delta I_n = I'_{dn} - I_{dn0}$ becomes:

$$\delta I_n = Kn\frac{w}{L}(mVTn+b)^2 + \sqrt{\frac{KnwIdn0}{L}} * \left[\sqrt{\frac{Idn0}{Kn\frac{w}{L}}}(m2+2m)+2(mVTn+b)(m+1)\right] \quad (5)$$

By neglecting the second and higher order terms, the error may be rewritten as:

$$\delta I_n = \delta I_{ndc} + \delta I_{nac} \qquad (6)$$

$$\text{with } \delta I_{ndc} = kn\frac{w}{L}(mV_{T_n}+b)^2 + \sqrt{k_n\frac{w}{L}*I_b}*\left[2(mV_{T_n}+b)\right] \quad (7)$$

$$\text{and } \delta I_{nac} = Iin*2m + \sqrt{k_n\frac{w}{L}*I_b}*\left[2(mV_{T_n}+b)\right]*\frac{\frac{I_{in}}{Ib}}{2} \qquad (8)$$

Where δI_{nac} is the signal dependent error, δI_{ndc} the signal independent error, I_b and I_{in} the biased current and the input current respectively.
In a similar manner, an input current I_{in} in the p-channel device will lead to a current error of:

$$\delta I_p = \delta I_{pdc} + \delta I_{pac} \qquad (9)$$

- If the basic algorithmic divider is considered, the current error at the end of the first iteration during the second cycle is:

$$(\delta IN_3)_2 = \left(\frac{\delta I pac}{2}\right) + \left(\frac{\delta I pdc}{2}\right) - \left(\frac{\delta I ndc}{2}\right) - \delta Inac \qquad (10)$$

which becomes $(\delta IN_3)_2 = (\frac{\delta I pac}{2}) - \delta I_{nac}$ (11)

If $\delta I_{pdc} = \delta I_{ndc}$

For the other iterations $(\delta I_{N3})_k$ will be unchanged. To achieve a good cancellation of the signal independent charge injection error, the current matching approach relies on matching between n-channel and p-channel devices.

As $\delta I_{pdc} = \delta Indc \pm \varepsilon_1$, $\delta I_{pac} = \delta Inac \pm \varepsilon_2$,

$\varepsilon_1 < \delta I_{pdc}$ and $\varepsilon 2 < \delta I_{pac.}$

Finally:

$$(\delta I_{N3})_k \cong \pm\left(\frac{\varepsilon_1}{2}+\frac{\varepsilon_2}{2}\right)-\frac{\delta I_{nac}}{2} \quad (12)$$

So a basic algorithmic current divider is quite insensitive to the signal independent error like the algorithmic multiplier [3]. The use of cells which compensate the signal dependant error as replica techniques or multi-sampling techniques will allow to obtain a very good accuracy.
Simulations show that the current error [tab 1] after the first iteration is of the order of 1% of $\frac{Iin}{2}$ if classical biased S.I cells are used.

I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA
20	6.9	10.28	10.28
40	16.82	20.2	20.2

-Tab 1- I_{N3} during the second cycle of each iteration with basic cells

If S^2I cells are used, the current error after the first iteration is constant and independent of the input current (Tab 2).

I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA
20	12.96	10.06	10.06
40	22.95	20.06	20.06

-Tab 2- I_{N3} during the second cycle of each iteration with S^2I cells

This error has been reduced at least by a factor of two or four and it is easier to compensate it because it is constant [13].
To obtain the same accuracy with classical biased cells, it is necessary to add capacitors of 1pF.

In this case the maximum frequency of algorithmic divider with S^2I biased cells is higher than that of algorithmic divider which uses SI biased cells.
To decrease the power consumption, class AB cells can be used.

- For the algorithmic current divider with CMOS stage, the last current error is equal to:

$$(\delta I_{N3})_k = \left(\frac{\delta I_{dc_{CMOS}}}{2}\right)\pm\left(\frac{\varepsilon_2}{2}\right)-\left(\frac{\delta I_{nac}}{2}\right) \quad (13)$$

The greatest part of this error comes from the CMOS stage (Tab 3-a).

	I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA	
(a)	40	19.61	21.73	21.73	Without added capacitors to the CMOS stage.
(b)	40	19.61	19.83	19.83	With added capacitors of 1pF.
(c)	40	19.61	19.80	19.80	With CMOS switch for the CMOS stage.
(d)	40	19.61	19.77	19.77	With a dummy circuit.

-Tab 3- I_{N3} during the second cycle without added capacitors for unbiased cells

Thus, to cancel the charge injection error two compensated methods must be implemented, one for the CMOS stage as the add of capacitors (Tab 3-b) or the use of CMOS switch (Tab 3-c) or the use of dummy circuit (Tab 3-d), and one for unbiased cells as the add of capacitors.

So, it is possible to achieve quite the same accuracy that the previous divider with a lower power consumption and a lower occupied die area than the basic algorithmic divider to the detriment of maximum frequency running due to the add of capacitors.

- For the last structure, it is more interesting to keep the output current on the transistor N_1 during the first cycle. The current error after the second iteration is equal to:

$$(\delta I_{N1})_3 = \delta I_{nac} - \delta I_{pac} \quad (14)$$

And this error becomes for the other iterations:

$$(\delta I_{N1})_k = \left(\frac{\delta Inac}{2}\right) \quad (15)$$

with $k > 3$

Tab 4- resumes the results obtained for this divider with the same cells that those used for the previous divider.

I_{in} µA	$(I_{N1})_3$ µA	$(I_{N1})_4$ µA
40	19.29	19.825

-Tab 4- I_{N1} during the first cycle of each iteration

To achieve the same accuracy than the other dividers, it is necessary to add capacitors.
So, if the occupied die area and power consumption are lower, this divider presents a more complex digital part and a poor maximum frequency.

V.- CONCLUSION

This paper presents the evolution of the CFT error in algorithmic current dividers using switched current technique.
First the basic algorithmic divider is considered and it is demonstrated that the final current error is quite insensitive to the signal independent error. Also, simulation results show that, if S^2I class AB cells are used, it is possible to obtain a high accuracy with a low power consumption.

Second the algorithmic divider with a CMOS stage is analyzed. However, the accuracy of this divider is limited by the CFT error of the CMOS stage. So, to obtain the same accuracy as the first divider, it must be necessary to add dummy circuit to CMOS stage and capacitors to unbiased cells to the detriment of speed performance and occupied die area.

Finally, for the structure proposed by Wang and al. a high accuracy is obtained if the output current is kept on N_1 transistor and if added capacitors are used.
So, this last structure presents the lowest power consumption, and a low occupied die area but speed performance are degraded by the add of capacitors.
Consequently, with more occupied die area, the basic algorithmic divider which uses S^2I class AB cells has the greatest accuracy and the best maximum frequency with still a low power consumption.

REFERENCES.

[1] P.Riffaud-Desgreys, E.Garnier, Ph.Roux, Ph.Marchegay, "New Structure of Algorithmic DAC in Switched-Current technique", International IEE Conference on Advanced A/D and D/A Conversion Techniques and their Applications - Glasgow 1999.

[2] P.Riffaud-Desgreys, E.Garnier, Ph.Roux, M..Loulou and J.Tomas, "A Switched-Current Algorithmic D/A Converter", 2nd Int. Workshop on Design of Mixed-mode Integrated Circuits and Applications - 1998.

[3] D.G.Nairm and C.A.T. Salama, Fellow IEEE, "A Ratio-Independent Algorithmic Analog to Digital Converter Combining Current Mode and Dynamic Techniques", IEEE Transactions on Circuits and Systems - Vol 37, N°3, March 1990.

[4] S.Wang, B.B.Bhattacharya and M.O. Ahmad, "A Novel Ratio-Independent Cyclic Multiplication D/A Converter", IEEE Int. Symposium on CAS - 1992.

[5] J.S.Wang and C.L.Wey, « High Speed CMOS Switched-Current D/A Converters for Low Power / Low Voltage Signal Processing Applications", - 1998.

[6] J.Robert, P.Deval, G.Weymann, "Very Accurate Current Divider", Electronics Letters - Vol 25, N°14, 6th July 1989.

[7] C.L.Wey and S.Krishman, "Current Mode Divide by two Circuit", Electronics Letters - Vol 28, N°9, 23rd April 1992.

[8] J.S.Wang and C.L.Wey, "Accurate CMOS Switched-Current Divider Circuits", IEEE – 1998.

[9] W.Groeneveld, H.Schouwenaars, H.Termeer, "A Self Calibration Technique for Monolithic high-Resolution D/A Converters", IEEE Int. Solid-State Circuits Conference – ISSCC 89.

[10] G.A.S.Machado, N.C.Battersby and C.Toumazou, "On the Development of Analogue Sampled-Data Signal Processing", Analog Integrated and Signal Processing – 1997.

[11] A.Matsuzawa, "Low–Voltage and Low–Power Circuit Design for Mixed Analog/Digital Systems in Portable Equipment", IEEE journal of Solid–State Circuits – Vol 29, N°4, April 1994.

[12] T.S.Fiez, Member IEEE, G.Liang, Member IEEE and D.J.Allstot, Senior Member IEEE, "Switched-Current Circuit Design Issues", IEEE journal of Solid-State Circuits – Vol 26, N°3, March 1991.

[13] C.K.Tse and M.H.L.Chow, "A New Clock-Feedthrough Cancellation Method for Second Generation Switched-Current Circuits", IEEE ISCAS – Vol 3, pp2104-2107, May 1995.

[14] W.B.Wilson, student Member IEEE, H.Z.Massoud Member IEEE, E.J.Swanson, Member IEEE, R.T.George, Jr. Member IEEE and R.B.Fair, Senior Member IEEE, "Measurement and Modeling of Charge Feedthrough in n-channel MOS Analog Switches", IEEE journal of Solid-State Circuits – Vol SC-20, N°6, December 1985.

[15] G.Wegmann, student Member IEEE, E.A.Vittoz, Senior Member IEEE and F.Rahali, "Charge Injection in Analog MOS Switches", IEEE journal of Solid-State Circuits – Vol SC-22, N°6, December 1987.