A New Current-mode Squaring Circuit with Compensation for Error Resulting from Carrier Mobility Reduction

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Abstract

This paper presents a new current-mode squaring circuit. The design is based on MOSFETs translinear principle in strong inversion. A new compensation techniques to minimize the second order effects caused by carrier mobility reduction in short channel MOSFETs is proposed. Tanner T-spice simulation tool is used to confirm the functionality of the proposed design in 0.18µm CMOS process technology. Simulation results indicate that the maximum linearity error is 1.16 % and the power consumption is 331µW.

1. Introduction

The squaring circuit is a very important building block in analog signal processing applications. This include but not limited to RMS-DC converters, pseudo-exponential cells, CMOS commanding filters, fuzzy control, multipliers, etc. [1]-[12]. As the transistor is scaled down, second order effects become more important and require modifications to the MOS models or a way to compensate for the errors due to these effects. The main effects that can be compensated for are the channel length modulation, body effect and the carrier mobility reduction. At large gate-source voltage, the high electric field developed between the gate and the channel confines the charge carrier to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. Since scaling has substantially deviated from the constant-field scenario, small-geometry devices experience significant mobility degradation.

Many compensation techniques in OTA based circuits are reported in the literature [13-17]. There is no much done to compensate for the error generated by the carrier mobility reduction in the current-mode circuits employing MOS trans-linear loop. Reference [13] proposed a technique to reduce the error of the output current caused by carrier mobility reduction. The circuit is voltage- mode and a controllable voltage source is required for the circuit to work properly.

In reference [18], a squarer/divider circuit is proposed. The main drawback of the design is the use of a resistor to compensate the error due to carrier mobility reduction which leads to high linearity error.

In this work, a new squaring circuit with compensation for the errors due to carrier mobility reduction employing MOSFETs Translinear Loop (MTL) is proposed. In section 2, the proposed circuit is presented. Simulation results are presented in section 3. Section 4 concludes the paper.

2. Proposed Circuit

The proposed squaring circuit is shown in Figure1. The squaring circuit is based on translinear loop formed by transistors (M1-M4). The current I_B is the bias current and I_X is the input current. The output current is given by:

$$I_{out} = \frac{I_x^{\,2}}{8I_B}$$

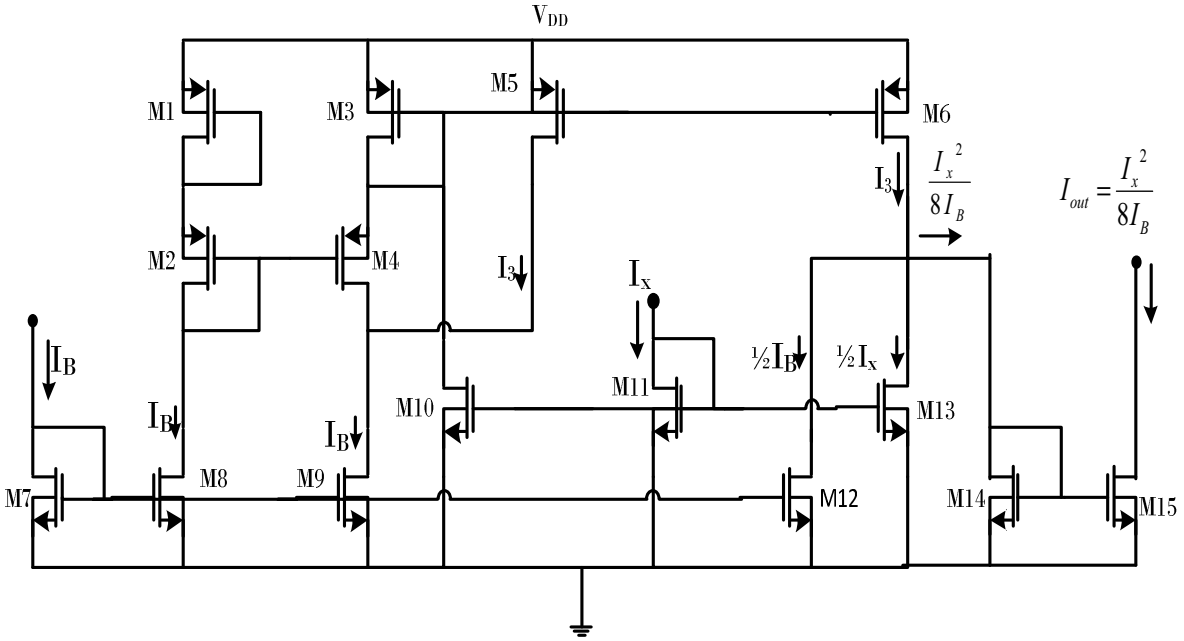

Fig.1 Proposed Current-mode squaring Circuit

With reference to Figure 1, writing MTL around transistors M1- M4 to get:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{1}$$

If the carrier mobility reduction is taken into consideration, the MOS drain current is given by:

$$I_D = \frac{\beta}{2}\frac{(V_{GS} - V_{TH})^2}{1+\theta(V_{GS} - V_{TH})} \tag{2}$$

where θ is a fitting parameter and β is the aspect ratio of transistor. Using equation (2), the gate-to source potential can be written as:

$$V_{GS} \approx \frac{I_D\theta}{\beta} + \sqrt{\frac{2I_D}{\beta}} + V_{TH} \tag{3}$$

Combining equations (1) and (3) to get:

$$\frac{I_{D1}\theta_1}{\beta_1} + \sqrt{\frac{2I_{D1}}{\beta_1}} + \frac{I_{D2}\theta_2}{\beta_2} + \sqrt{\frac{2I_{D2}}{\beta_2}} = \frac{I_{D3}\theta_3}{\beta_3} + \sqrt{\frac{2I_{D3}}{\beta_3}} + \frac{I_{D4}\theta_4}{\beta_4} + \sqrt{\frac{2I_{D4}}{\beta_4}} \tag{4}$$

Assuming the aspect ratios of the transistors satisfy the condition $\beta_1 = \beta_2 = 2\beta$, $\beta_3 = \beta_4 = \beta$ and $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta$ where β is the transconductance parameter of the pMOS and θ ≈ 0. 25 V-1 is a fitting parameter.

Equation 4 can be rewritten as:

$$\frac{I_{D1}\theta}{2\beta} + \sqrt{\frac{2I_{D1}}{2\beta}} + \frac{I_{D2}\theta}{2\beta} + \sqrt{\frac{2I_{D2}}{2\beta}} = \frac{I_{D3}\theta}{\beta} + \sqrt{\frac{2I_{D3}}{\beta}} + \frac{I_{D4}\theta}{\beta} + \sqrt{\frac{2I_{D4}}{\beta}} \tag{5}$$

Since the drain current of transistors M1 and M2 are the same, equation (5) can be expressed by:

$$\frac{\theta}{\beta}I_b + \frac{1}{\sqrt{\beta}}\left[2\sqrt{I_B}\right] = \frac{\theta}{\beta}[I_{D3} + I_{D4}] + \frac{1}{\sqrt{\beta}}\left[\sqrt{2I_{D3}} + \sqrt{2I_{D4}}\right] \tag{6}$$

If we force the following condition $\frac{\theta}{\beta}I_B = \frac{\theta}{\beta}[I_{D3} + I_{D4}]$, then

$$I_B = I_{D3} + I_{D4} \tag{7}$$

Using the condition in equation (7) then equation (6) can be rewritten as:

$$\frac{1}{\sqrt{\beta}}\left[2\sqrt{I_B}\right] = \frac{1}{\sqrt{\beta}}\left[\sqrt{2I_{D3}} + \sqrt{2I_{D4}}\right] \tag{8}$$

Equation (8) can be rewritten as:

$$\sqrt{2I_{D4}} = 2\sqrt{I_B} - \sqrt{2I_{D3}} \tag{9}$$

From the circuit schematic shown in Figure 1, with current Ix mirrored in transistor M10 and I_{D3} is mirrored in M5 and M6.

$$I_{D3} = I_X + I_{D4} \tag{10}$$

Combining equations (10) and (9), the drain current for M4 is given by:

$$I_{D4} = \frac{I_B}{2} - \frac{I_x}{2} + \frac{I_x^2}{8 I_B} \tag{11}$$

Combining equations (11) and (10) to get:

$$I_{D3} = I_X + \frac{I_B}{2} - \frac{I_x}{2} + \frac{I_x^2}{8 I_B} = \frac{I_x}{2} + \frac{I_B}{2} + \frac{I_x^2}{8 I_B} \tag{12}$$

The first two terms to the right are subtracted using transistors M10 and M13 and the output is mirrored via M14 and M15 to get:

$$I_{out} = \frac{I_x^2}{8 I_B} \tag{13}$$

Equation 13 can be written as:

$$I_{out} = kI_x^2 \tag{14}$$

Where, $K = \frac{1}{8} I_B$

It is clear that equation (14) implements squaring circuit with compensation of errors due to carrier mobility reduction.

3. Simulation Results

The functionality of the proposed design is confirmed using Tanner T-spice in 0.18µm CMOS process. The bias current is 60 µA and the input current is swept from -40-to-40µA. The circuit is operated by 1.5V DC supply. The DC transfer characteristic is shown in Figure 2. It is clear from the figure that the proposed design is in a close agreement with the theory.

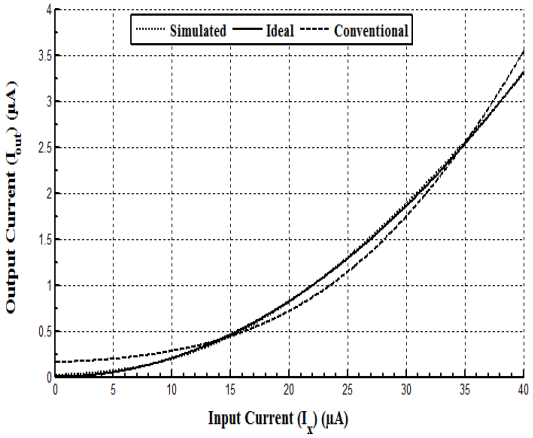

Fig.2 DC Simulation result for squaring circuit

Plot of the error between calculated and simulated results is shown in Figure 3. The maximum linearity error is 1.16%

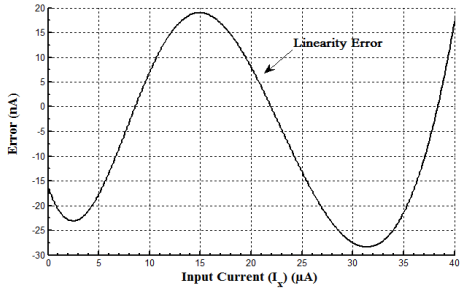

Fig.3. Error between calculated and simulated

Comparison of the performance between this work and previous art is given in table1. It is clear from the table the proposed design has a superior performance.

Table1. Performance comparison

	[14]	[15]	[16]	[17]	[18]	proposed
Technology (µm)	0.8	0.8	0.5	0.35	0.25	0.18
Maximum linearity error %	-	-	-	-	1.9	1.16
Bandwidth (MHz)	2.5	≈50	1.96	-	0.03	82.4
Input range (µA)	10	±20	±20	7	±40	±40

4. Conclusion

A new squaring circuit using short channel MOSFET is achieved. The circuit is free of errors due to carrier mobility reduction. The maximum linearity error is 1.16 % and the power dissipation is 331μW. The circuit is a core block in multiplier design using MOSFETS in strong inversion.

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