A New Topology for Multilevel Current Source Inverter with Reduced Number of Switches

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Abstract

In this paper, a new topology for multilevel current source inverter (CSI) is presented. The proposed topology employs reduced switches number to generate desired multilevel output current. The proposed topology uses $(n+7)/2$ switches and $(n-1)/2$ current-sharing inductors for an *n*-level CSI. Two modulation methods are applied for the proposed topology. One method is fundamental frequency modulation method and the other is carrier phase-shifted sinusoidal pulse width modulation (SPWM) method. As simulation results using PSCAD/EMTDC will show, the proposed topology can generate the desired output current levels and current balance of the current-sharing inductors is completely provided in each control method.

1. Introduction

Multilevel converters were developed as a result of requirement for higher power converters [1]. These converters have substantial advantages for higher power applications comparing with two level inverters, such as reduced harmonics, and higher power ratings because of reduced switching device voltage and current stresses. Voltage Source Inverter (VSI) has been the mostly used multilevel topology up to now. However, as one of multilevel converter types, Current source Inverters (CSIs) have also some advantages such as inherent four-quadrant operation capability, direct control of the output current and easier fault management for higher power applications such as high power drives. Moreover the power circuit of the CSI is simpler and more robust than the VSI due to no freewheeling diodes with unidirectional current flow. Also the CSI can provide a higher reliability related with a dc-link inductor than a capacitor for the VSI [2, 3, 4]. CSIs are not as common as VSIs. An important reason for this reduced interest in CSIs is that inductors used in a CSI as storage elements have higher conduction losses and lower energy storage efficiency compared to DC link capacitors in VSIs. But, with the development of superconducting magnetic energy storage (SMES) technologies many of the problems of conventional inductors can now be solved, and hence their applications are developing specially for higher power ratings [5].

There are some different topologies proposed for multilevel CSI in the literature. In [6] an *n*-level CSI has been presented that uses $2(n-1)$ power electronic switches and $(n-3)$ current-sharing inductors. In [7] a new topology for single-phase multilevel CSI has been proposed using $(n+3)$ switches and $(n-3)/2$ current-sharing inductors then extended to three-phase system in [8]. In [9] and [2] two new topologies have been proposed for three-phase multilevel CSI. In [3] a three-phase multilevel CSI using two types of CSI is presented. One is thyristor-based load-commutated converter and the other is a GTO-based converter operating in parallel.

A new topology is proposed in this paper that uses reduced switches number. This topology employs $(n+7)/2$ switches and $(n-1)/2$ current-sharing inductors for an *n*-level CSI. At first, the power circuit of the proposed topology will be presented and then the switching method will be described. Two modulation methods will be applied. Finally the simulation results in PSCAD/EMTDC environment will be presented for 5-level and 7-level CSI to validate the proposed topology.

2. The new proposed topology for CSI

The proposed topology is shown in Fig. 1. As this figure shows, for an *n*-level CSI, $(n+7)/2$ power electronic switches and $(n-1)/2$ current-sharing inductors are used. The current-sharing inductors are the same. So applying appropriate control method, the current balance between them is guaranteed and we have:

$$L_1 = L_2 = L_3 = \cdots = L_{(n-1)/2}$$
$$I_1 = I_2 = I_3 = \cdots = I_{(n-1)/2} = \frac{2I}{n-1} \tag{1}$$

In the above equation, I is the source current and $I_1, I_2, I_3, ..., I_{(n-1)/2}$ are the current-sharing inductors current.

So each inductor acts as a current source that can be short-circuited by means of switches $S_5, S_6, \cdots, S_{(n+7)/2}$ or conducted to the load. Therefore the output current can be a multilevel current.

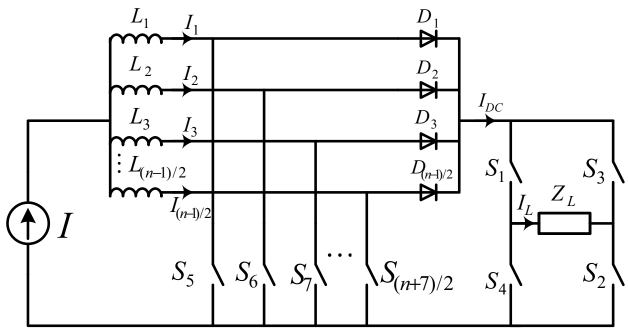

Fig. 1. Power circuit of the proposed *n*-level CSI

Switches S_1, S_2, S_3 and S_4 are used to change the output current direction in positive and negative half cycles. So these switches work at output current frequency. Other switches (i.e. $S_5, S_6, \cdots, S_{(n+7)/2}$) are used to generate the desired levels of output current and must be higher frequency switches in the case of carrier phase-shifted SPWM control method. Diodes $D_1, D_2, ..., D_{(n-1)/2}$ are used to separate switches $S_5, S_6, \cdots, S_n$ and without using these diodes it is not possible to achieve the desired levels in the output current.

In order to compare the proposed topology with the other topologies presented in the literature, the switches number and current-sharing inductors number of the different topologies are illustrated in figures 2 and 3 respectively. As these figures show, in the proposed multilevel CSI the number of switches is reduced considerably. For example, for a 7-level CSI, the topologies presented in [6] and [7] uses 12 and 10 switches respectively while the proposed topology in this paper uses only 7 switches. According to Fig. 2, as level number increases, difference between switches number of the topologies grows up considerably while the switches number of the proposed CSI has the least increasing rate against level number. Fig. 3 shows the number of current-sharing inductors in each structure. As this figure shows, in the proposed structure, the number of current-sharing inductors decreased comparing with the structure that presented in [6] but, comparing with the structure that is presented in [7], only one additional current-sharing inductor is used for each output current level number.

Fig. 4 and 5 show the power circuit of the proposed 5-level and 7-level CSI respectively. These topologies will be analyzed in detail. Table I and II show the switching combinations to achieve the desired levels in the output current for 5-level and 7-level CSI respectively.

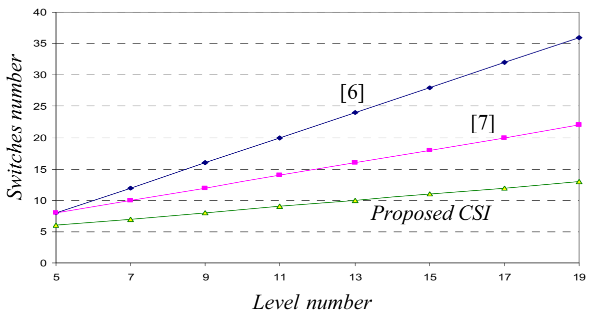

Fig. 2. The number of switches against to level number in different topologies

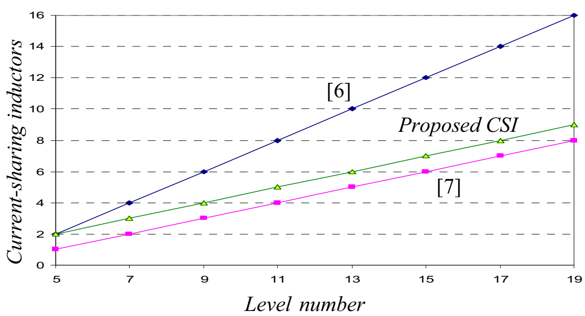

Fig. 3. The number of current-sharing inductors against to level number in different topologies

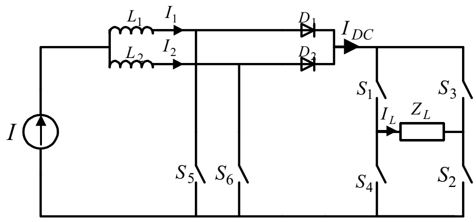

Fig. 4. Power circuit of the proposed 5-level CSI

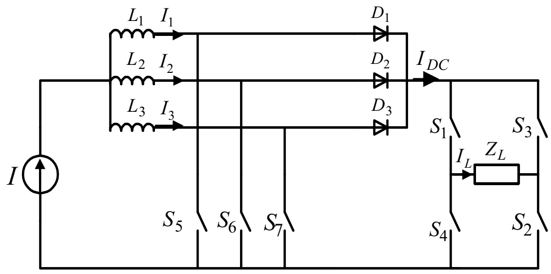

Fig. 5. Power circuit of the proposed 7-level CSI

Table 1. Switching combinations of the 5-level CSI

Level	ON Switches	Output Current	DC bus Current (I_{DC})
1	S_5, S_6	0	0
2	S_1, S_2, S_6 or S_1, S_2, S_5	$\frac{I}{2}$	$\frac{I}{2}$
3	S_1, S_2	I	I
4	S_3, S_4, S_5 or S_3, S_4, S_6	$-\frac{I}{2}$	$\frac{I}{2}$
5	S_3, S_4	$-I$	I

Table 2. Switching combinations of the 7-level CSI

Level	ON switches	Output current	DC bus current (I_{DC})
1	S_5, S_6, S_7	0	0
2	S_1, S_2, S_5, S_6 or S_1, S_2, S_5, S_7 or S_1, S_2, S_6, S_7	$\frac{I}{3}$	$\frac{I}{3}$
3	S_1, S_2, S_5 or S_1, S_2, S_6 or S_1, S_2, S_7	$\frac{2I}{3}$	$\frac{2I}{3}$
4	S_1, S_2	I	I
5	S_3, S_4, S_5, S_6 or S_3, S_4, S_5, S_7 or S_3, S_4, S_6, S_7	$-\frac{I}{3}$	$\frac{I}{3}$
6	S_3, S_4, S_5 or S_3, S_4, S_6 or S_3, S_4, S_7	$-\frac{2I}{3}$	$\frac{2I}{3}$
7	S_3, S_4	$-I$	I

3. Switching strategy

3.1. Fundamental frequency modulation method

The switching strategy should ensure two main requirements; (1) generation of the desired levels of the output current and (2) current balance between current-sharing inductors. To satisfy these requirements we should use all the possible switching combinations that are presented in Table I and II for 5-level and 7-level CSI respectively. In other words, if we have more than one possible combination for an output current level, all of the combinations should be used to ensure the current balance between current-sharing inductors. For example, two different combinations are available to achieve the output current level of $I/2$ and both should be used in each output current cycle. For the 5-level CSI we can use all of the switching combinations in a cycle of output current. So, the switching states will be as Table 3.

Taking Table 2 into consideration, there are 6 possible switching combinations to achieve each DC bus current levels of $I/3$ and $2I/3$ in the proposed 7-level CSI. So, we have 36 different switching combinations. To ensure current balance between the current-sharing inductors, all of these possible switching combinations should be used but this is available in three cycles of the output current. So, the switching states for the 7-level CSI will be as Table 4.

Table 3. The switching states for 5-level CSI in a period of the output current

θ range	ON switches	Output current
$0 \le \theta \le \theta_1$	S_5, S_6	0
$\theta_1 \le \theta \le \theta_2$	S_1, S_2, S_5	$I/2$
$\theta_2 \le \theta \le \pi - \theta_2$	S_1, S_2	I
$\pi - \theta_2 \le \theta \le \pi - \theta_1$	S_1, S_2, S_6	$I/2$
$\pi - \theta_1 \le \theta \le \pi + \theta_1$	S_5, S_6	0
$\pi + \theta_1 \le \theta \le \pi + \theta_2$	S_3, S_4, S_5	$-I/2$
$\pi + \theta_2 \le \theta \le 2\pi - \theta_2$	S_3, S_4	$-I$
$2\pi - \theta_2 \le \theta \le 2\pi - \theta_1$	S_3, S_4, S_6	$-I/2$
$2\pi - \theta_1 \le \theta \le 2\pi$	S_5, S_6	0

3.2. Carrier phase-shifted SPWM modulation method

Carrier phase-shifted SPWM control can be applied for the proposed topology. Fig. 6 shows the application of this control method. In this figure, m, ϕ and ω_o are modulation index, output current initial phase angle and angular frequency of the output current respectively. In this method, to extract the switching pattern, $(n-1)/2$ triangular carrier waveforms are compared with a reference waveform. Carrier waveforms phase shifted from each other by $4\pi/(n-1)$ radians. As mentioned before, the direction of the output current is changed using switches S_1, S_2, S_3 and S_4. So, the carrier phase-shifted SPWM control only is applied for other switches (i.e. $S_5, S_6, \cdots, S_{(n+7)/2}$). Therefore, variation of carrier waveforms is between 0 and 1. Also absolute value of reference waveform is compared with carrier waveforms.

Table 4. The switching states for 7-level CSI in three periods of the output current

θ range	ON switches	Output current
$0 \le \theta \le \theta_1$	S_5, S_6, S_7	0
$\theta_1 \le \theta \le \theta_2$	S_1, S_2, S_5, S_6	$I/3$
$\theta_2 \le \theta \le \theta_3$	S_1, S_2, S_7	$2I/3$
$\theta_3 \le \theta \le \pi - \theta_3$	S_1, S_2	I
$\pi - \theta_3 \le \theta \le \pi - \theta_2$	S_1, S_2, S_6	$2I/3$
$\pi - \theta_2 \le \theta \le \pi - \theta_1$	S_1, S_2, S_5, S_7	$I/3$
$\pi - \theta_1 \le \theta \le \pi + \theta_1$	S_5, S_6, S_7	0
$\pi + \theta_1 \le \theta \le \pi + \theta_2$	S_3, S_4, S_6, S_7	$-I/3$
$\pi + \theta_2 \le \theta \le \pi + \theta_3$	S_3, S_4, S_5	$-2I/3$
$\pi + \theta_3 \le \theta \le 2\pi - \theta_3$	S_3, S_4	$-I$
$2\pi - \theta_3 \le \theta \le 2\pi - \theta_2$	S_3, S_4, S_7	$-2I/3$
$2\pi - \theta_2 \le \theta \le 2\pi - \theta_1$	S_3, S_4, S_5, S_6	$-I/3$
$2\pi - \theta_1 \le \theta \le 2\pi + \theta_1$	S_5, S_6, S_7	0
$2\pi + \theta_1 \le \theta \le 2\pi + \theta_2$	S_1, S_2, S_5, S_7	$I/3$
$2\pi + \theta_2 \le \theta \le 2\pi + \theta_3$	S_1, S_2, S_6	$2I/3$
$2\pi + \theta_3 \le \theta \le 3\pi - \theta_3$	S_1, S_2	I
$3\pi - \theta_3 \le \theta \le 3\pi - \theta_2$	S_1, S_2, S_5	$2I/3$
$3\pi - \theta_2 \le \theta \le 3\pi - \theta_1$	S_1, S_2, S_6, S_7	$I/3$
$3\pi - \theta_1 \le \theta \le 3\pi + \theta_1$	S_5, S_6, S_7	0
$3\pi + \theta_1 \le \theta \le 3\pi + \theta_2$	S_3, S_4, S_5, S_6	$-I/3$
$3\pi + \theta_2 \le \theta \le 3\pi + \theta_3$	S_3, S_4, S_7	$-2I/3$
$3\pi + \theta_3 \le \theta \le 4\pi - \theta_3$	S_3, S_4	$-I$
$4\pi - \theta_3 \le \theta \le 4\pi - \theta_2$	S_3, S_4, S_6	$-2I/3$
$4\pi - \theta_2 \le \theta \le 4\pi - \theta_1$	S_3, S_4, S_5, S_7	$-I/3$
$4\pi - \theta_1 \le \theta \le 4\pi + \theta_1$	S_5, S_6, S_7	0
$4\pi + \theta_1 \le \theta \le 4\pi + \theta_2$	S_1, S_2, S_6, S_7	$I/3$
$4\pi + \theta_2 \le \theta \le 4\pi + \theta_3$	S_1, S_2, S_5	$2I/3$
$4\pi + \theta_3 \le \theta \le 5\pi - \theta_3$	S_1, S_2	I
$5\pi - \theta_3 \le \theta \le 5\pi - \theta_2$	S_1, S_2, S_7	$2I/3$
$5\pi - \theta_2 \le \theta \le 5\pi - \theta_1$	S_1, S_2, S_5, S_6	$I/3$
$5\pi - \theta_1 \le \theta \le 5\pi + \theta_1$	S_5, S_6, S_7	0
$5\pi + \theta_1 \le \theta \le 5\pi + \theta_2$	S_3, S_4, S_5, S_7	$-I/3$
$5\pi + \theta_2 \le \theta \le 5\pi + \theta_3$	S_3, S_4, S_6	$-2I/3$
$5\pi + \theta_3 \le \theta \le 6\pi - \theta_3$	S_3, S_4	$-I$
$6\pi - \theta_3 \le \theta \le 6\pi - \theta_2$	S_3, S_4, S_5	$-2I/3$
$6\pi - \theta_2 \le \theta \le 6\pi - \theta_1$	S_3, S_4, S_6, S_7	$-I/3$
$6\pi - \theta_1 \le \theta \le 6\pi$	S_5, S_6, S_7	0

Two carrier waveforms phase shifted from each other by π radians are required for the 5-level CSI and three carrier waveforms phase shifted from each other by $2\pi/3$ radians are required for the 7-level CSI. Carrier and reference waves of the 7-level CSI are presented in Fig. 7. Note that in this figure, carrier frequency is selected very low to be easy for understanding.

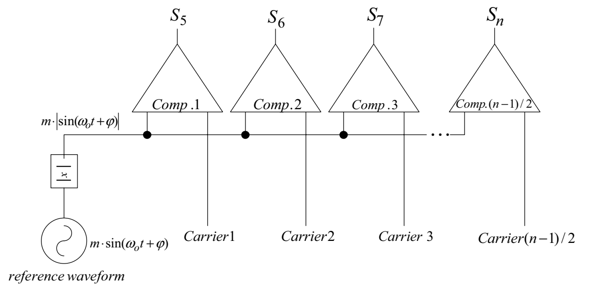

Fig. 6. Carrier phase-shifted SPWM control of the proposed CSI

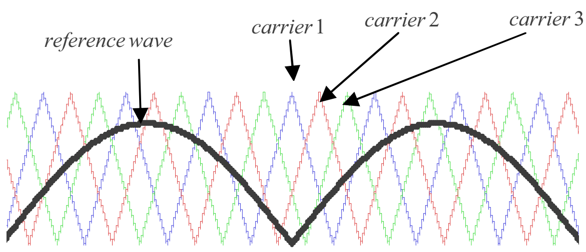

Fig. 7. Carrier and reference waves of the 7-level CSI

4. Simulation results

In this section, the simulation results of the 5-level and 7-level proposed CSI carried out using PSCAD/EMTDC is presented to verify the capabilities of the proposed topology in generating the desired output current and providing current balance of the current-sharing inductors. As mentioned before two different control methods are investigated for the proposed topology. Results of these control method are presented in the next two subsections.

A parallel *R-C* load with $R = 6\Omega$ and $C = 50\mu F$ is connected to multilevel CSI output. The frequency of the output current and carrier waveforms is $50Hz$ and $1250Hz$ respectively. The current source value is $40A$ and the inductance of each current-sharing inductor is $60mH$ and all switches considered to be ideal. Each switch consists of a IGBT series with a diode.

4.1. Simulation results for the fundamental frequency modulation method

Fig. 8(a) and 8(b) show the output current and current-sharing inductors current of the 5-level CSI. As these figure show, the proposed topology is able to generate the desired output current levels while current balance between current-sharing inductors is completely satisfied that verifies the accuracy of the control method. In Fig. 8(b) it can be seen that the current balance of the inductors becomes better as time increases because the circuit reaches to its steady-state condition.

Output current and current-sharing inductors current of the proposed 7-level CSI are shown in figures 9(a) and 9(b) respectively.

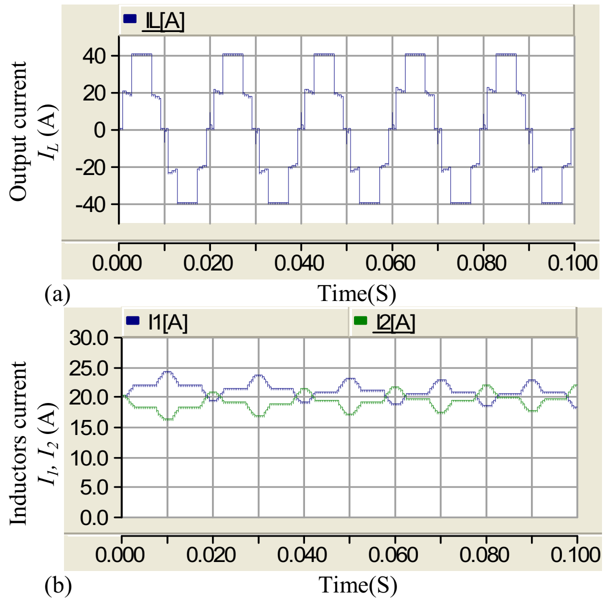

Fig. 8. Simulation results of the 5-level CSI (a) output current and (b) current-sharing inductors current

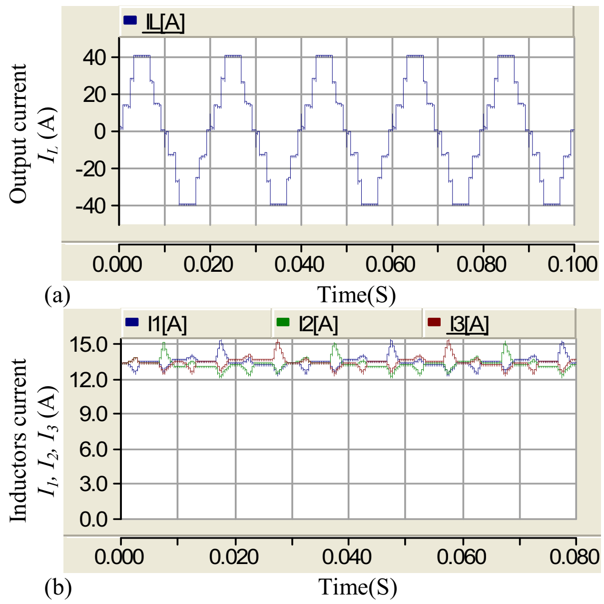

Fig. 9. Simulation results of the 7-level CSI (a) output current and (b) current-sharing inductors current

4.2. Simulation results for the carrier phase-shifted SPWM modulation method

Fig. 10 shows the operation of the proposed 5-level CSI using carrier phase-shifted SPWM modulation method. Fig. 10(a) and 10(b) show the output current and current-sharing inductors current respectively. As these figures show, this control method can be successfully applied for the proposed CSI topology. Applying this control method, the current balance between current-sharing inductors improves considerably compared with the latter control method and the current through current-sharing inductors are almost the same and equal to one half of the output current. Moreover, output current magnitude can be linearly controlled by controlling the modulation index *m*, and also there are no low order harmonic components in the output current. The harmonic components of the output current are around the switching frequency which can be easily canceled out using a small LC filter. So this method is a suitable option to control the proposed multilevel CSI.

Fig. 11 shows the simulation results of the 7-level CSI using carrier phase-shifted SPWM control. Fig. 11(a) shows the output current and Fig. 11(b) shows the current of the current-sharing inductors that have the same values equal to one third of the total output current.

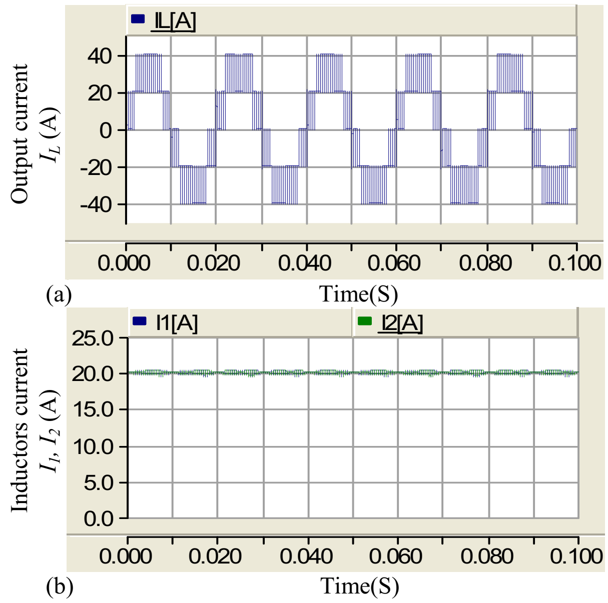

Fig. 10. Operation of 5-level CSI using carrier phase-shifted SPWM modulation method (a) output current and (b) current through current-sharing inductors

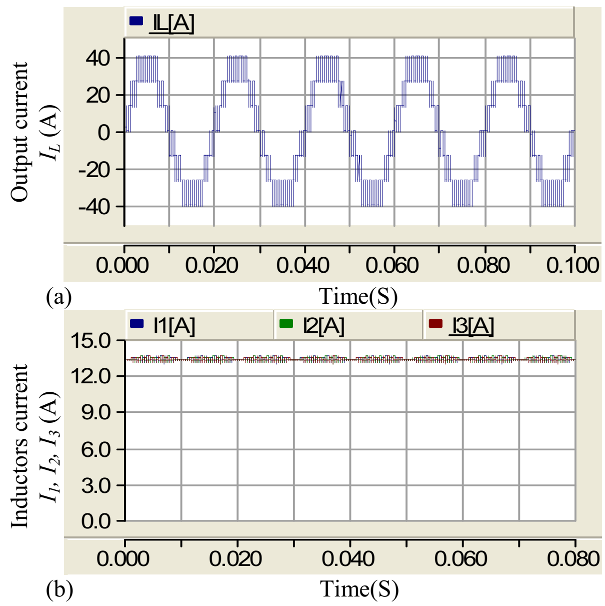

Fig. 11. Operation of 7-level CSI using carrier phase-shifted SPWM modulation method (a) output current waveform and (b) current through current-sharing inductors

5. Conclusion

A new multilevel CSI is proposed. The proposed topology uses reduced number of switches and is able to produce the desired output current while the current balance between current-sharing inductors is guaranteed using appropriate control method. Two modulation methods has been applied for the proposed topology and in each case the two important criteria (1) output current waveform and (2) current balance between current-sharing inductors are completely satisfied. The simulation results carried out using PSCAD/EMTDC validate the capabilities of the proposed topology.

6. References

[1] R. H. Wilkinson, T. A. Meynard, and H. du T. Mouton, "Natural balance of multicell converters: the two-cell case", *IEEE Trans. Power Electron.,* vol. 21, no. 6, pp. 1649-1657, Nov. 2006.

[2] Z. Bai, Z. Zhang and Y. Zhang, "A generalized three-phase multilevel current source inverter with carrier phase-shifted SPWM", in *power electronics specialists conf.*, PESC2007, pp. 2055-2060.

[3] S. Kwak and H. A. Toliyat, "Multilevel converter topology using two types of current-source inverters", *IEEE Trans. Ind. Appl,* vol. 42, no. 6, pp. 1558-1564, Nov./Dec. 2006

[4] B. Wu, J. Pontt, J. Rodríguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives", *IEEE Trans. Ind. Electron,* vol. 55, no. 7, pp. 2786-2797, Jul. 2008

[5] J. Bao, D. G. Holmes, Z. Bai, Z. Zhang and D. Xu, "PWM control of a 5-level single-phase current-source inverter with controlled intermediate DC-link current", in *power electronics specialists conf.,* PESC2006, pp. 1-6.

[6] F. M. Antunes, Henrique A. C. Braga and I. Barbi, "Application of a generalized current multilevel cell to a current source inverter", *IEEE Trans. Ind. Electron.,* vol. 46, no. 1, pp. 31-38, Feb. 1999.

[7] Y. Xiong, D. Chen, S. Deng and Z. Zhang, "A new single-phase multilevel current-source inverter", in *19th Annual IEEE Applied power Electronics conf. and exposition*, Anaheim, California, 2004. pp. 1682-1685.

[8] Y. Xiong, Y. Li, Z. Zhang and K. Wei, "A new three-phase five-level current-source inverter", in *20th Annual IEEE Applied Power Electronics conf. and exposition,* 2005, pp. 424-427.

[9] Y. Xiong, D. Chen, X. Yang, C. Hu, and Z. Zhang, "Analysis and experimentation of a new three-phase multilevel current-source inverter", in *35th IEEE Annual Power Electronics Specialist Conf.,* Aachen, Germany, 2004, pp. 548-551.