Rm-C FILTER DESIGN FOR LOW VOLTAGE POWER SUPPLIES

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ABSTRACT

In this study, a new Rm-C high-pass filter is proposed employing a new CMOS Rm-variable OTRA topology. Proposed OTRA topology can operate with very low voltage power supplies as ± 0.6 V. In this design, CMOS 0.13 µm ST Microelectronics technology transistor models are used for the simulations. The developed CMOS Rm-variable OTRA has a transresistance gain (Rm) of 7279 V/I with a 39.52 MHz transresistance gain bandwidth (-3dB) and a transresistance unity-gain bandwidth of 2.464 GHz with a 5pF load capacitance. The simulated high-pass filter has a cutoff frequency of 6.7 MHz confirming the theoretical analysis.

I. INTRODUCTION

In todays CMOS sub-micron technologies, the power supplies used in the design of the integrated chips are totally of the order of 1V. This very low voltage power supplies lead the designers to develop active circuits that can operate at these voltage levels. In recent years, several active filters have been developed by only using active element and capacitances [1-4]. The developed filters existing in the literature are mostly the transconductance-C (Gm-C) filters that use OTA (Operational Transconductance Amplifier) as the active element. Also a new design concept using the transresistance-C (Rm-C) differentiator as the building block in the filter has been introduced recently that use OTRA (Operational Transresistance Amplifier) as the active element [5-7]. Only bandpass filters are proposed in the previous Rm-C filters which use power supplies as ± 2.5V. The demand for the low voltage designs leads the designers to develope high performance Rm-variable OTRA structures for the current-mode analog system design.

In this work, using the ST Microelectronics CMOS 0.13 µm technology, a Rm-variable OTRA is designed for ± 0.6 V power supplies. The transresistance of the OTRA can be tuned by an external control voltage. Using this OTRA, a second order OTRA Rm-C high-pass filter employing only two OTRA's and three capacitances is proposed. This new CMOS Rm-variable OTRA topology is characterised by the CADENCE simulation program. The characterictic results of the CMOS Rm-variable OTRA, and the high-pass OTRA Rm-C filter are given.

II. PROPOSED CMOS OTRA TOPOLOGY

The Operational Transresistance Amplifier (OTRA) is a three terminal analog building block with a describing matrix in the form given by (1)

$$\begin{bmatrix} V_1 \\ V_2 \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_o \end{bmatrix} \quad (1)$$

Circuit symbol of the OTRA is illustrated in Figure 1.

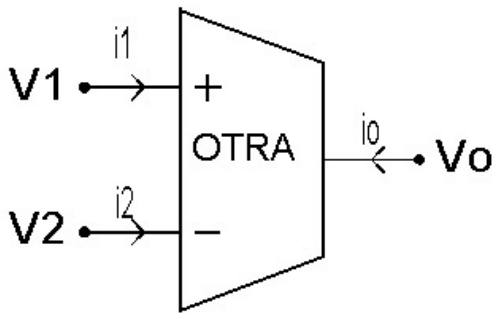

Figure 1: Circuit symbol of the OTRA

Both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded, leading to circuits that are insensitive to the stray capacitance as reported in [8].

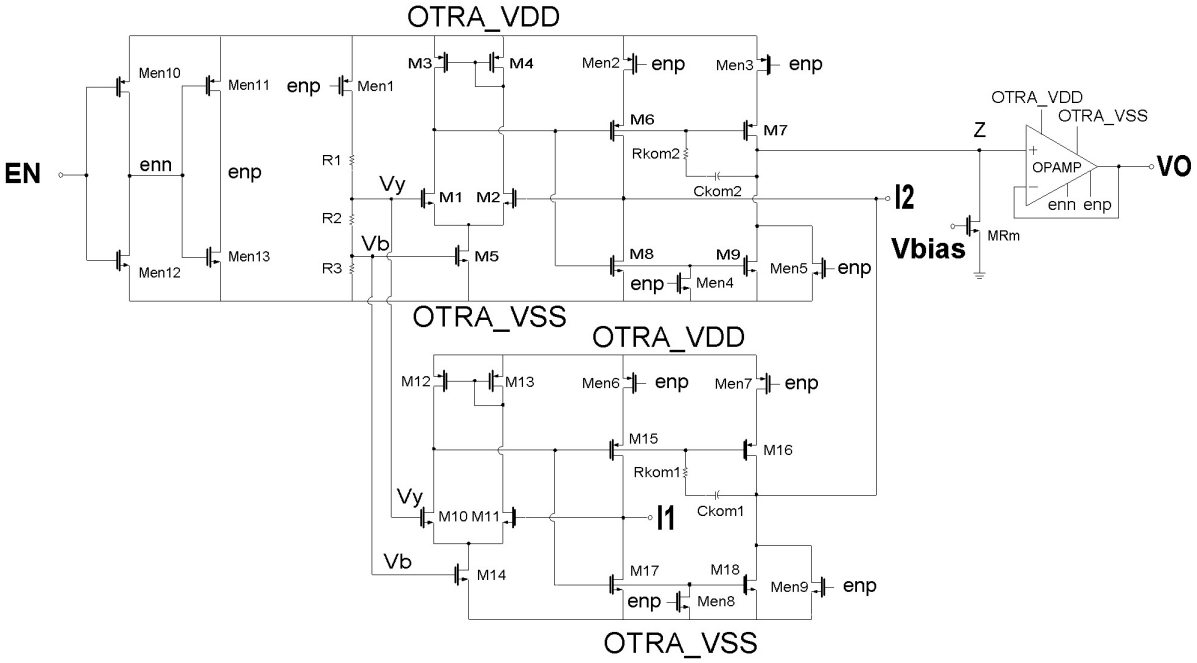

Figure 2: Proposed CMOS variable-Rm OTRA topology

For ideal operation, the transresistance gain, Rm approaches infinity forcing the input currents to be equal. Thus the OTRA must be used in a negative feedback configuration in a way that is similar to conventional op amps. OTRA has similar transmission properties to the current-feedback op-amp, but with two low-impedance inputs and one low-impedance output for the OTRA. Since the input terminals of these circuits are virtually grounded, they are suitable for cascade connection.

The proposed CMOS Rm-variable OTRA is illustrated in Figure 2. This circuitry also includes the power-down signal generator stage of the OTRA and the power-down transistors. OTRA is functional when the input "EN" is at the VSS voltage level. When the input "EN" is at the VDD voltage level, all the system is in the power-down mode and the output "VO" forms a high impedance output.

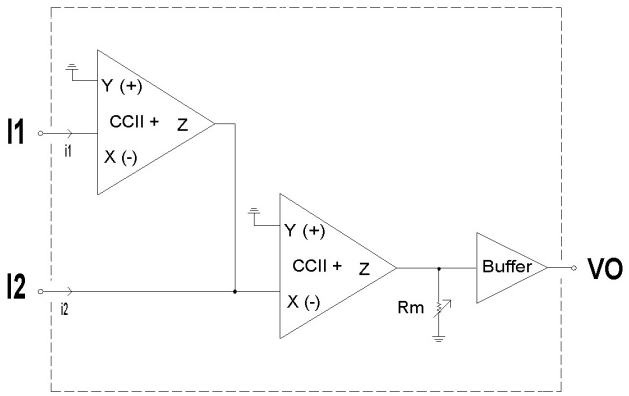

Figure 3: CCII+ based variable-Rm OTRA topology

This OTRA topology is based on the idea of using CCII+ blocks which is illustrated in Figure 3. The input currents named as i_1 and i_2 are applied to the low impedance inputs of the two CCII+. The current difference is mirrored to the "Z" node of the second CCII+. This current forms the unbuffered output voltage as $VO = Rm.(i_1 - i_2)$. Finally, the non-buffered output voltage over the Rm resistor, is applied to a unity-gain buffer composed with an OPAMP in order to have a low output impedance as illustrated in Figure 2. The CCII+ topology proposed in 2001 is used as the CCII+ in the OTRA [9].

Two differential amplifier generated with the NMOS transistors M1 - M4 and M10 – M13 are biased equally with the bias voltage V_y. Because of using two power supplies as ± 0.6 V, the bias voltage is selected as 0 V (ground voltage). The current mirror bias voltage V_b is generated in the bias stage as illustrated in Figure 2.

In the input stage, I_1 is the positive, I_2 is the negative node. The advantage of using Class AB structure in the CCI+ with the transistors M6 – M9 and M15 - M18 is capability of operating with very low voltage power supplies. The negative feedbacks in the input nodes generated with the transistors M2, M6 and M11, M15 forms low input impedances. Compensation capacitances and Ckom1, Ckom2 and resistors Rkom1, Rkom2 reduce the phase delay between the input currents i_1 and i_2, and the transferred current i_Z in the CCII+.

The mirrored current difference forms the output voltage on the (MRm) NMOS transistor used as resistor. The resistor value is variable and controlled by the external Vbias voltage.

III. OTRA Rm-C FILTER DESIGN

In this study, by using the proposed CMOS OTRA, a new OTRA Rm-C high-pass filter is also proposed. The OTRA Rm-C high-pass filter topology is illustrated in Figure 4. This filter is based on the current-mode operation. Its current transfer function equation is given by (2)

$$\frac{i_o}{i_{in}} = \frac{s^2 \dfrac{C_3}{C_1}}{\left(s + \dfrac{1}{C_1 R_{m1}}\right)\left(s + \dfrac{1}{C_2 R_{m2}}\right)} \qquad (2)$$

In this filter type, the maximum –3 dB gain frequency is achieved when the two poles of the filter have the same value. These two poles have the same value, if the capacitances and transresistances are chosen as $C_1 = C_2 = C$, and $R_{m1} = R_{m2} = R_m$. In this case -3dB gain frequency of the high-pass filter and the quality factor (Q) is given by (3),

$$f_{-3dB} = \frac{f_{pole}}{\sqrt{\sqrt{2}-1}} = 1.554 \times f_{pole}, \qquad f_{pole} = \frac{1}{2\pi C R_m}, \qquad Q = 0.5 \qquad (3)$$

The gain of the filter is defined with $K = C_3 / C_1$.

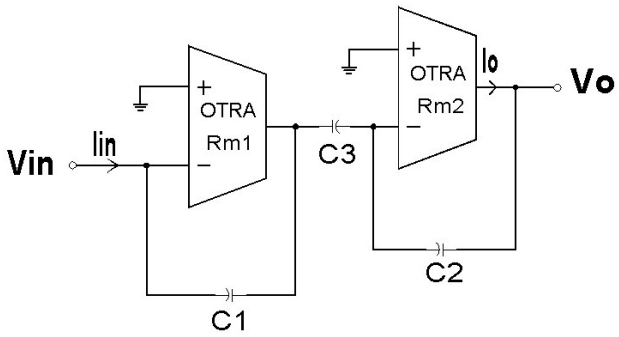

Figure 4: Proposed OTRA Rm-C high-pass filter

IV. SIMULATION RESULTS

The proposed CMOS variable-Rm OTRA and Rm-C filter, are simulated in the CADENCE simulation program, with the ST Microelectronics CMOS 0.13 µm technology *spectre* models by using the transistor and element values listed in Table 1 for OTRA. Power supplies are used as ± 0.6 V. The load capacitance used in the simulations for OTRA characterisation is 5pF.

The typical dc simulation results are shown in Figure 5, Figure 6. According to these results the maximum output voltages are reached with at least 200 µA of input difference current. The maximum output voltage in the dc analysis is 0.481 V, and the minimum output voltage is -0.475mV with 200µA input current. The normalized transresistance gain is shown in Figure 7. By selecting Vbias = 0.6 V, transresistance gain (Rm) as 7279 V/I, and the -3 dB bandwidth of the transresistance gain as 39.52 MHz are achieved which can be considered as a good range for the CMOS 0.13µm technology. Also the unity gain-bandwidth is 2.464 GHz. This bandwidth region gives the oppurtunity of designing high bandwidth filters and inductance simulators. The transresistance of the OTRA can be varied by the Vbias control voltage. The range of the Rm is between 3400 – 12000 for this topology. The variable range of the transresistance is shown in Figure 8.

The performance characteristics of the CMOS variable-Rm OTRA is shown at the Table 2.

For the high-pass filter illustrated in Figure 4, $C_1 = C_2 = C_3 = 5$pF, are selected. The dc transresistance gain (Rm) of the OTRA is 7279 V/I when Vbias = 0.6 V. The theoretical cut-off frequency of the high-pass filter is $f_{-3dB(teo)} = 6.796MHz$, and the simulated one is $f_{-3dB(sim)} = 6.695MHz$, the difference because of the non-idealities of the OTRA is about % 1.48. The theoretical current gain of the filter is 1 (0 dB), and the simulated one is 0.891 (–1 dB), the difference because of the non-idealities of the OTRA is about % 10.9. The performance of the ideal and the simulated high-pass filter is shown in Figure 9.

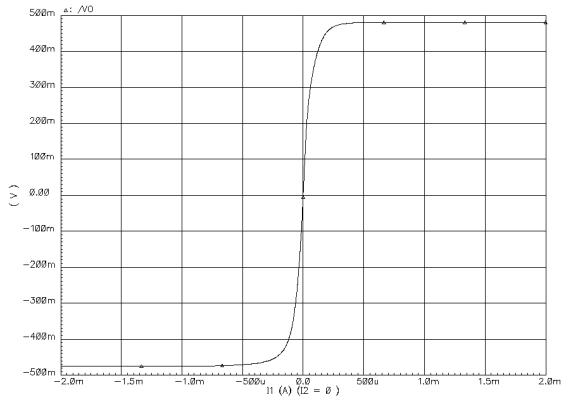

Figure 5: Typical dc simulation result of OTRA

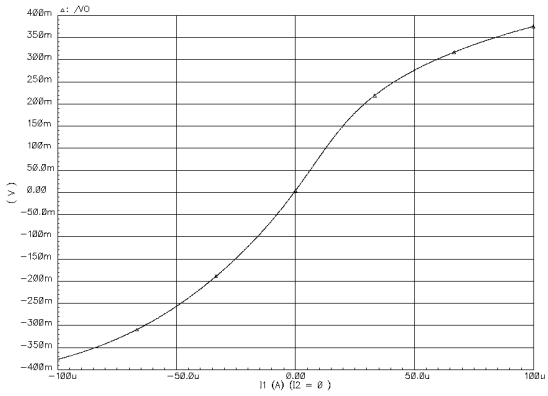

Figure 6: Zoomed typical dc simulation result of OTRA

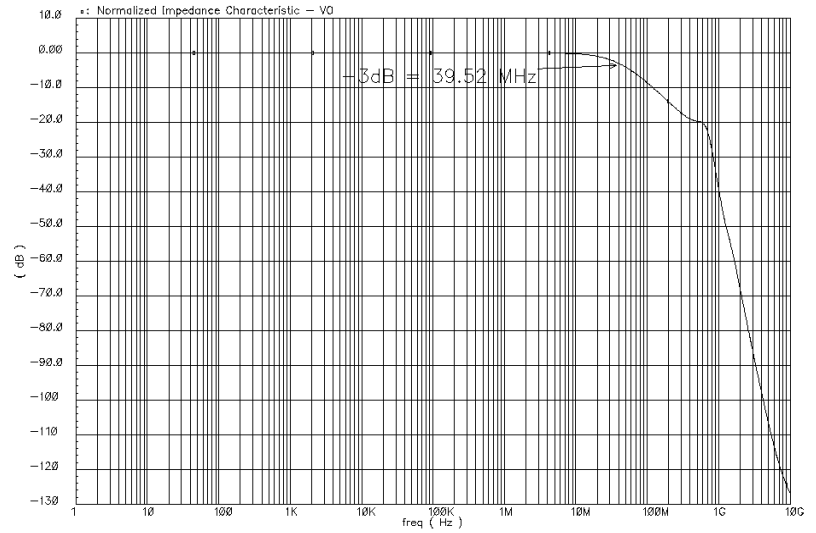

Figure 7: Typical ac simulation result, transresistance gain of the OTRA in a normalized axis with Vbias = 0.6 V

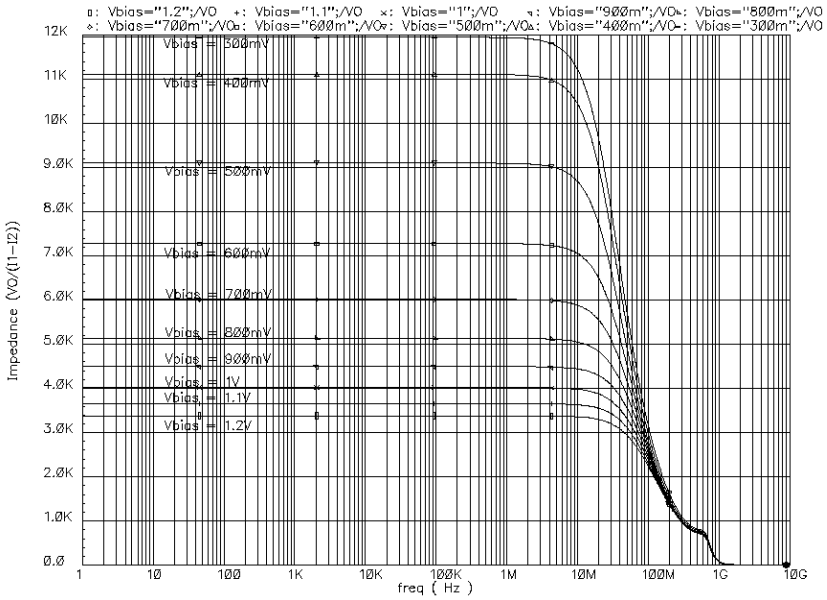

Figure 8: Typical ac simulation result, transresistance of the CMOS variable-Rm OTRA with Vbias = 0.3 V – 1.2 V

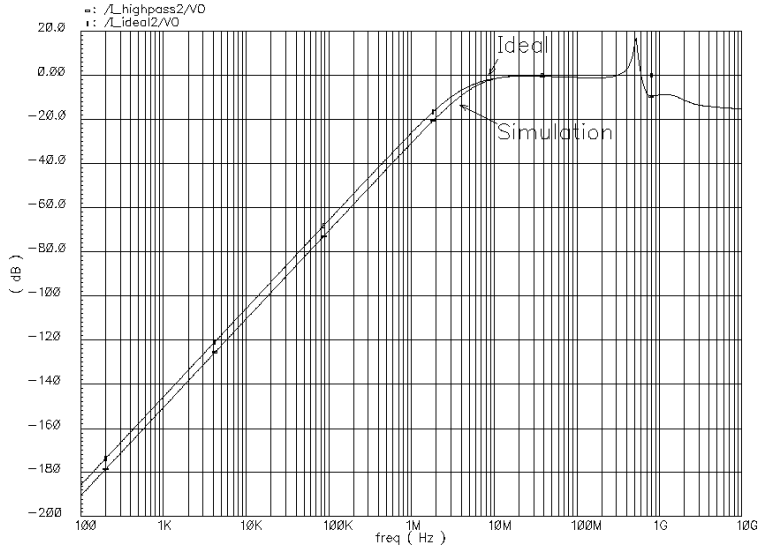

Figure 9: High-pass filter characterization of the ideal and the simulated CMOS OTRA with a typical ac simulation

Table 1: Transistor dimensions (W/L) in the proposed CMOS OTRA

Transistor name	W / L
M1, M2, M10, M11	108.8 µm / 0.3 µm
M3, M4, M12, M13	3.6 µm / 0.3µm
M5, M14	13.6 µm / 0.4 µm
M6, M15	9 µm / 0.36 µm
M7, M16	12.6 µm / 0.36 µm
M8, M17	8.5 µm / 0.36 µm
M9, M18	11.9 µm / 0.36 µm
MRm	6.8 µm / 4 µm
Men1, Men2, Men3, Men6, Men7	100.8 µm / 0.3 µm
Men4, Men5, Men8, Men9	3.4 µm / 0.13 µm
Men10, Men11	28.8 µm / 0.13 µm
Men12, Men13	13.6 µm / 0.13 µm
Other devices	**Value**
Ckom1, Ckom2	400 fF
Rkom1, Rkom2	1 KΩ
R1	6.4 KΩ
R2	1.6 KΩ
R3	4.8 KΩ

Table 2: Performance of the proposed CMOS OTRA

Power supply	± 0.6V
Maximum output voltage	0.481 V
Minimum output voltage	-0.475 V
Input resistance	$R\_I_1 = R\_I_2 = 18.6\ \Omega$
Output resistance	0.89 Ω
Input offset current	0.64 µA
Transresistance gain (Rm) (DC)	7279 V/I (Vbias = 0.6 V)
Transresistance gain range (Rm) (DC)	3400 - 12000 V/I
Transresistance gain bandwidth (-3dB)	39.52 MHz (Vbias = 0.6 V)
Transresistance unity gain-bandwidth	2.464 GHz (Vbias = 0.6 V)
Power consumption	6.89 mA, 8.27 mW (Vbias = 0.6 V)

IV. CONCLUSION

In this study, a new CMOS variable-Rm OTRA for the low voltage power supplies is proposed where the Rm is controlled with an external control voltage. This current-mode active element is suitable for high frequency applications, including filter, inductance simulator applications. Characterisation simulations of the OTRA are done with the CADENCE tool, and 39.52 MHz transresistance gain bandwidth (-3dB) is achieved. Using the proposed CMOS variable-Rm OTRA, a new OTRA Rm-C filter design approach is proposed giving a high-pass filter which have the simulation results confirming the theoretical analysis.

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