On the Modeling of Electron Devices: Concept, Accuracy Criterion With Application Examples, Importance in EE Education

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Abstract

In this work we investigate the accuracy criterion of the electron device models and give practical circuit examples. The analysis and design of integrated circuits depend heavily on the utilization of suitable models for integrated-circuit components. Since any analysis is only as accurate as the model used, it is essential that the circuit designer have a thorough understanding of the origin of the models commonly utilized and the degree of approximation involved in each. The subject investigated demonstrates clearly the importance of the modelling in EE education.

1. Introduction

Due to the advances in electronics, computer technologies and computer programs CAD gets an important role in the design of electronic circuits and systems. This makes simulation and modeling indispensable for the design of electronic devices [1-5]. Nowadays Computer simulation is one of the most important steps in the IC design. As semiconductor microelectronic devices become ever smaller approaching the physical limits, simulation and modeling becomes increasingly important for the research and development of electronics industry[6].
Computer-aided design enables the circuit designer to do things which are not possible with other techniques[1,2].

Using computer simulations the designer can

- Observe waveforms and frequency responses of voltages and currents without loading the circuit as a probe would in actual circuit.,
- Predict the performance of an IC at high frequencies without the parasitics a breadboard introduces.
- Use ideal devices
- Feed into circuit ideal waveforms such as extremely fast pulses or mixture of pulses and sinusoids.
- Open a feedback loop without disturbing the dc levels
- Determine the poles and zeros of transfer functions for even large circuits
- Do noise, sensitivity, worstcase and statistical analyses.

In other words, computer simulation is the best measurement method for the designer. The accuracy of the analysis and design of integrated circuits depends strongly on the precision of the model used to simulate the electron devices. This is valid for both the hand calculations with simple models and the computer simulations with more complex models. Since any analysis is only as accurate as the model used, it is clear that modelling plays an important factor in IC design [1-7].

The model of a nonlinear device must represent with sufficient accuracy the variations of the device characteristics with the terminal currents and voltages for every operating region. The general method is to determine the model parameters with optimization method to minimise the error between the calculated and measured values of device characteristics[1-5]. Since the small-signal low-frequency parameters are equal to the partial derivatives of the current/voltage relations, it is clear that a model will represent the device accurately if there is a good agreement between the measured and calculated variations of these parameters with the terminal currents and voltages. This is a further criterion for the model accuracy [8-19].

Furthermore, circuit models are also applicable on reliability analyses of electronic circuits. The importance of long term reliability in MOS VLSI circuits is becoming an important subject because of the increasing densities of VLSI chips. Hot carrier effects cause noncatastrophic failures which develop gradually over time and change the circuit performance.

Using adequate circuit models, the degradation in the threshold voltage and resulting change in the circuit behaviour can be estimated [20-30].

In summary, since any analysis is only as accurate as the model used, it is essential that the circuit designer have a thorough understanding of the origin of the models commonly utilized and the degree of approximation involved in each [1,7].

In this work we investigate the accuracy criterion of the models and giving practical circuit examples. Followed by a section on reliability of CMOS circuits. The subject investigated demonstrates clearly the importance of the modelling in circuit theory and circuit system education.

2. Modeling of Nonlinear N-port Active Device

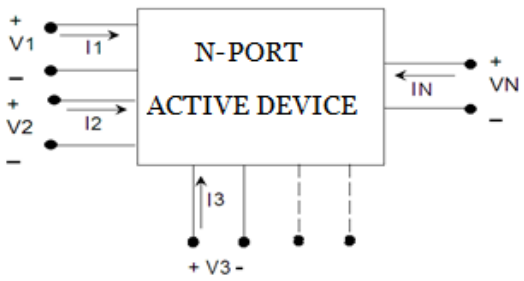

Fig. 1. Nonlinear N-port Active Device

Consider an N-port nonlinear active device illustrated in Fig.1. The current-voltage relations of the active device is given as

$$\begin{pmatrix} I_1 \\ I_2 \\ . \\ I_N \end{pmatrix} = \begin{pmatrix} f_1(V_1,V_2,...,V_N) \\ f_2(V_1,V_2,...,V_N) \\ . \\ f_N(V_1,V_2,...,V_N) \end{pmatrix} \quad (1)$$

where I_i and V_i are related terminal currents and voltages (i= 1…. N). Note that there are N nonlinear equations to describe the device behaviour. Another very important equation set is given by

$$J = \begin{pmatrix} \partial f_1/\partial V_1 & \partial f_1/\partial V_2 & . & \partial f_1/\partial V_N \\ \partial f_2/\partial V_1 & \partial f_2/\partial V_2 & . & \partial f_2/\partial V_N \\ . & . & . & . \\ \partial f_N/\partial V_1 & . & & \partial f_N/\partial V_N \end{pmatrix} \quad (2)$$

which yields the partial derivatives of the nonlinear functions to the terminal voltages. In fact, these partial derivatives correspond to the small signal parameters of the N-port device; in other words, they represent the port input conductances and the transconductances between the related ports. Since these partial derivatives are expressed in terms of nonlinear functions, they depend on the operating point of the device and their values change if the operating point is changed.

The general model of a nonlinear device must represent with sufficient accuracy the variations of the device characteristics with the terminal currents and voltages for every operating region. Since the small-signal low-frequency parameters are equal to the partial derivatives of the current/voltage relations, it is clear that a model will represent the device accurately if there is a good agreement between the measured and calculated variations of these small signal parameters with the terminal currents and voltages [8-13].

This can be used as a further accuracy criterion for a model; namely, a good agreement between the measured and calculated variations of these small signal parameters with the terminal currents and voltages [8-16].

3. Examples with Applications

BJT model, High-precision BJT model

A simple example is the BJT model. A BJT has four basic quantities, namely V_{BE}, I_B, V_{CE}, I_C. Choosing two of them as independent variable, the other two can be expressed as the function of these independent variables. The mostly used equantions are as

$$I_B = I_B(V_{BE}, V_{CE}) \quad (3)$$
$$I_C = I_C(V_{BE}, V_{CE})$$

$$V_{BE} = V_{BE}(I_B, V_{CE}) \quad (4)$$
$$I_C = I_C(I_B, V_{CE})$$

Equation set (3) represents the currents in terms of voltages, they give input and output characteristics for constant base-emitter voltage. Equation set (4) gives the input voltage and the output current in terms of the base current and collector-emitter voltage, this set yields the input and output characteristics for constant base current. Basic characteristics of the BJT are given below in Figs.2-9:

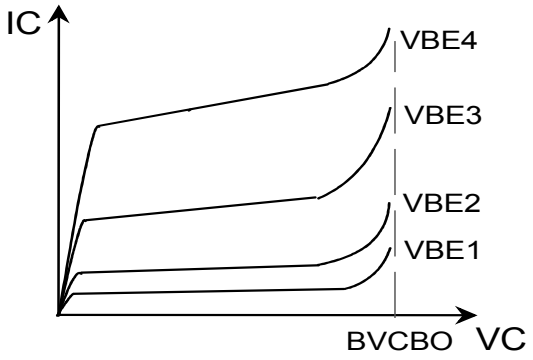

Fig. 2. Output characteristics for constant V_{BE}

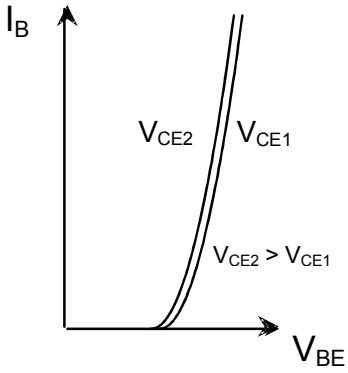

Fig.3. Input characteristics, $I_B = I_B(V_{BE}, V_{CE})$

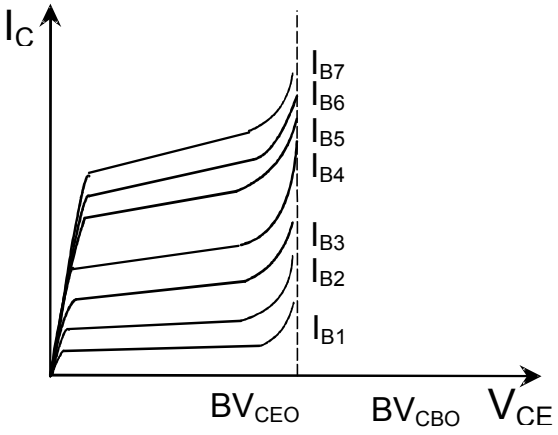

Fig.4. Output characteristics for constant I_B

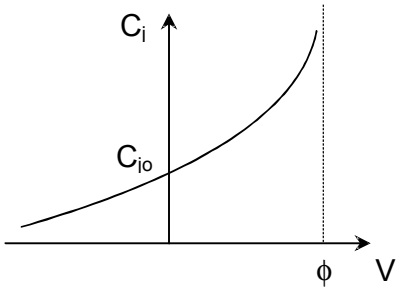

Fig.5. Dependence of junction capacitance on biasing voltage, $C_j=C_j(V)$.

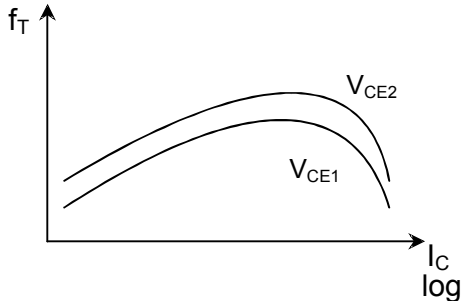

Fig.6. Dependence of the transistion frequency f_T on the collector current I_C for constant V_{CE}

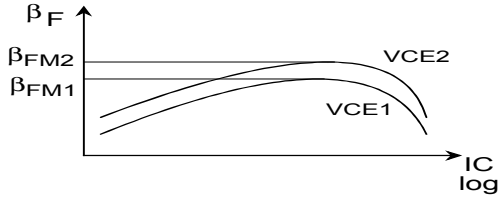

Fig.7. Dependence of β_F against I_C for constant V_{CE}

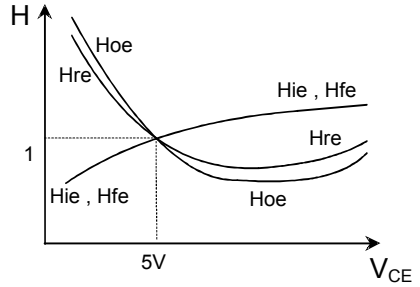

Fig.8. Dependence of the h parameters on V_{CE}. I_C = constant.

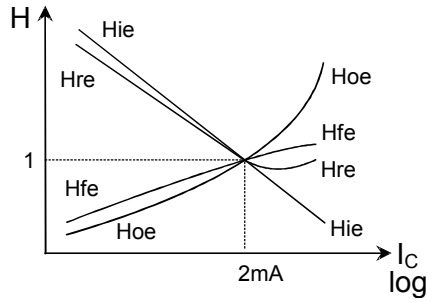

Fig.9. Dependence of the h parameters on I_C. V_{CE} = constant.

where

$$h_{ie}=\left.\frac{\partial V_{BE}}{\partial I_B}\right|_{V_{CE}=const.} \qquad h_{re}=\left.\frac{\partial V_{BE}}{\partial V_{CE}}\right|_{I_B=const.} \tag{5}$$

$$h_{fe}=\left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}=const.} \qquad h_{oe}=\left.\frac{\partial I_C}{\partial V_{CE}}\right|_{I_B=const.}$$

$$y_{ie}=\left.\frac{\partial I_B}{\partial V_{BE}}\right|_{V_{CE}=st} \qquad y_{re}=\left.\frac{\partial I_B}{\partial V_{CE}}\right|_{V_{BE}=st} \tag{6}$$

$$y_{fe}=\left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{CE}=st} \qquad y_{oe}=\left.\frac{\partial I_C}{\partial V_{CE}}\right|_{V_{BE}=st}$$

With the present nonlinear bipolar transistor models, these conditions cannot be achieved sufficiently. Using a high-precision model a good agreement between experiment and theory is provided. The model is based on the original Gummel-Poon model and the modified Ebers-Moll model by Leblebici and Kuntman, where the Early effect is represented in a different way to conventional models [8-10].

The variations of the small-signal *h and y* parameters with V_{CE} obtained by this model agree with the measured values. To increase the accuracy of the model for the forward active operating region, the following components are added:

a- To improve the variations of *hre* and *hoe* with *Ic* at low collector currents, the leakage resistance *RCB* of the collectorbase junction is added between the collector and base nodes,

b- To represent the avalanche multiplication, a controlled current source I_{GF} with three extra model parameters *k, n* and BV_{CBO} is incorporated into the model between the collector and base terminals (n is a coefficient, *k* is a constant multiplier and BV_{CB0} is the breakdown voltage of the transistor).

The new model obtained with these additions is shown in Fig.10.

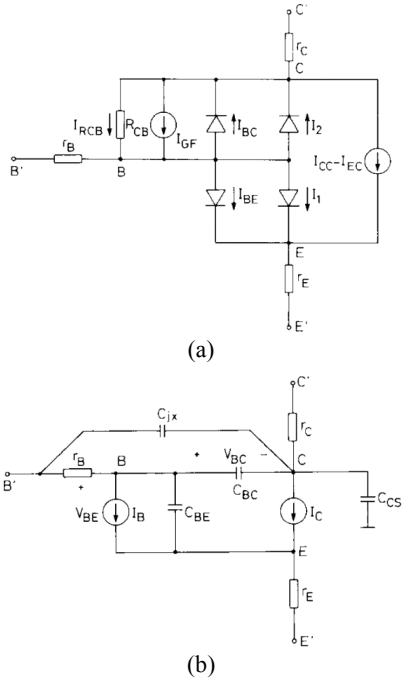

Fig.10. New model obtained with these additions: a) static model, b) dynamic model.

Calculated characteristics and experimental results are illustrated in Figs. 11-14. For comparison, SPICE model reults are also given in the figures. It is evident that theoretical and experimental plots of hoe against V_{CE} for I_C = constant agree with each other because of the physical modeling of Early effect and the incorporation of the collector avalanche multiplication. The conventional SPICE BJT model results in an approximately constant output conductance.

It can be observed that the plot of hoe against I_C for V_{CE} = constant obtained from the proposed model is in good agreement with experimental plot because of the inclusion of the collector-base junction leakage resistance RCB. The reults from the SPICE BJT model differ significantly from the measured values at low collector currents.

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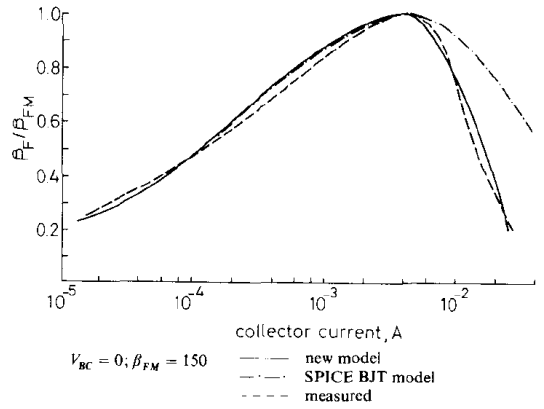

Fig.11. Measured and calculated variations of β_F against I_C

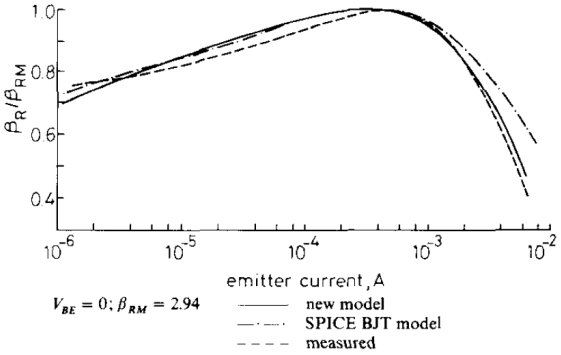

Fig.12. Measured and calculated variations of β_R against I_E

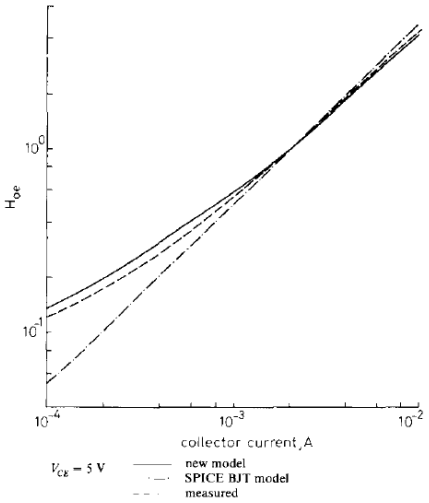

Fig.13. Measured and calculated variations of h_{oe} against I_C

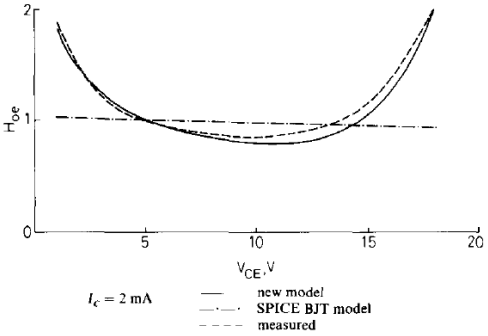

Fig.14. Measured and calculated variations of h_{oe} against V_{CE}

THD Properties of Active Loaded BJT Amplifier

The modeling of hoe-I_C and hoe-V_{CE} dependences is important for correct nonlinear distortion analysis of the BJT amplifiers. This is demonstrated on a typical example of active loaded BJT amplifier illustrated in Fig.15. The aim was to determine the optimum operating point of the active loaded BJT amplifier where the total harmonic distortion THD is minimum.

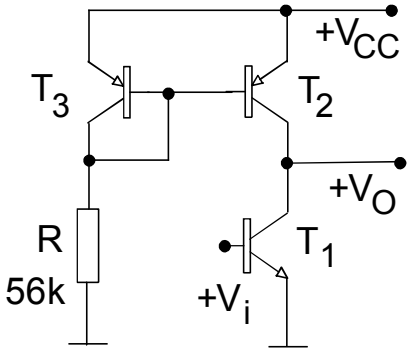

Fig. 15. Active loaded BJT amplifier

The input signal was a filtered 1 kHz sinusoidal voltage. For an output voltage of Vpp = 2V the measured and calculated variations of THD with VCE are shown in Fig.16. SPICE simulation results are also illustrated to compare models. Fig. 16

proves the accuracy provided by the proposed modification. Simulation yields at VCEQ = 4.35V and measurements at VCEQ = 4.5V an optimum operating point where the total harmonic distortion is minimum. SPICE simulations gives no minimum for THD. It is therefore impossible to determine the optimum operating conditions.

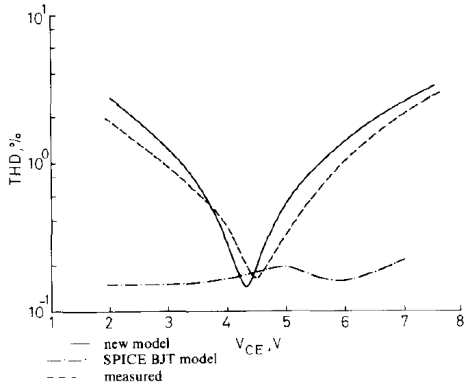

Fig.16. Optimum operating point of active loaded BJT amplifier where the total harmonic distortion THD is minimum.

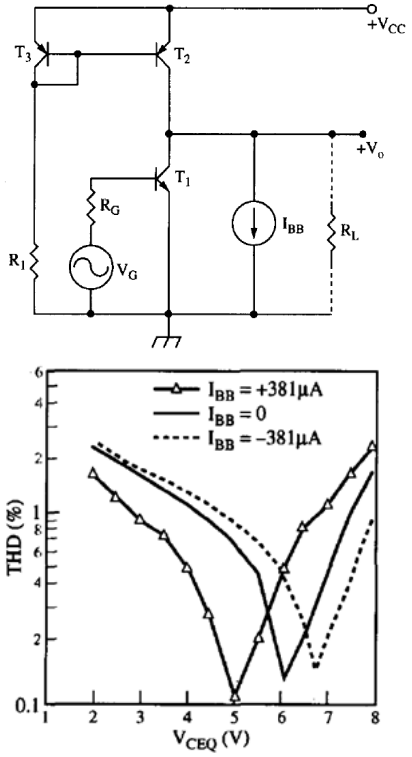

Fig.17. Shifting the optimum operating point for THD to any desired point on the dc transfer characteristic by incorporating an additional current source.

Furthermore, using this accurate model, a new method is proposed which renders possible shifting of the optimum operating point for THD to any desired point on the dc transfer characteristic, by incorporating an additional current source into the circuit to obtain different dc current levels in driver and load transistors as shown in Fig.17 [19]. The proposed method is based on the analytical expressions derived for the harmonic distortion coefficients of active-loaded amplifiers [8-16] using a high-precision BJT model [8-12]. The current I_{BB} can have both positive and negative values. Simulations and experiments were carried out, either drawing out or injecting current from or to the output node. The resulting curves of THD vs. VCE for an output voltage of Vop = 1 V, f = 1 KHz, Iref = 615μA, Vcc = 10V, related to the current values I_{BB} =-381μA, I_{BB}=0 and I_{BB} = +381μA are also shown in Fig.17. Simulation and experimental results are in good agreement with calculated results.

THD Properties of Active Loaded CMOS Amplifier

Similar investigations can be performed also for CMOS active loaded amplifier shown in Fig.18. Using an accurate model and performing similar step the optimum operating point from the point of view of THD can be specified as illustrated in Fig.19 [18,20].

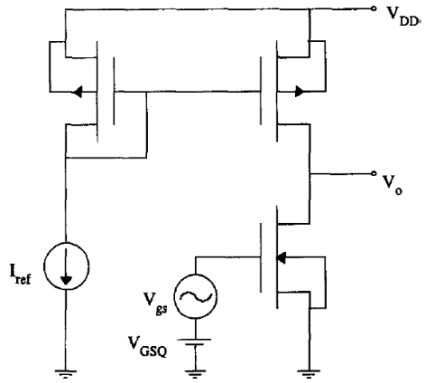

Fig.18. Active loaded CMOS amplifier stage.

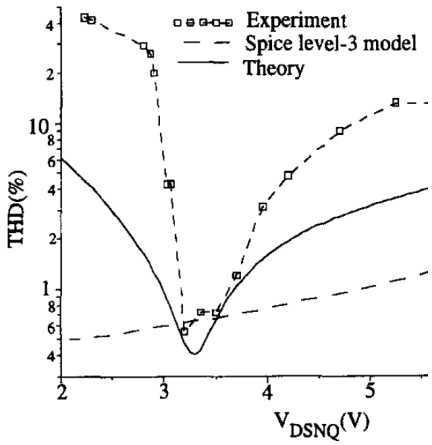

Fig.19. Optimum operating point of active loaded CMOS amplifier where the total harmonic distortion THD is minimum.

From the curves it can be observed that the theoretical results are in good agreement with experimental results. The total harmonic distortion (THD) shows a minimum at a special value of V_{DSNopt}=3.3V, where the second harmonic distortion HD2 has a zero crossing and theTHD is determined primarily by the third harmonic distortion HD3.

4. Circuit model of reliability estimation of MOS transistors

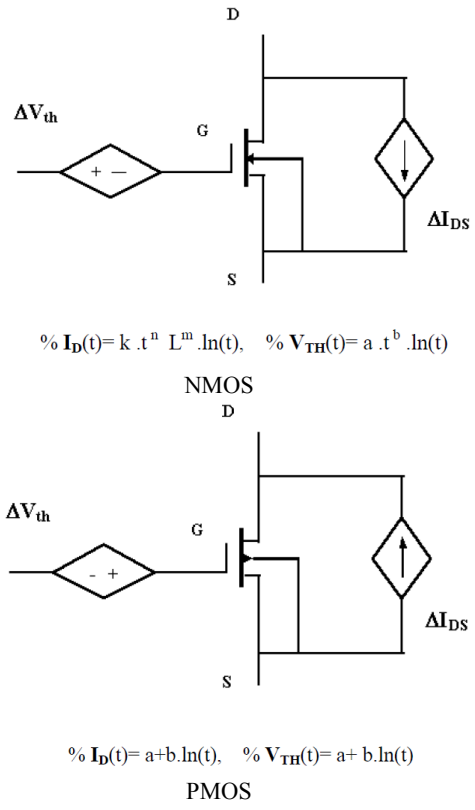

Fig.20. Degradation model for NMOS and PMOS transistors.

The importance of long term reliability in MOS VLSI circuits is becoming an important subject because of the increasing densities of VLSI chips. Hot carrier effects cause noncatastrophic failures which develop gradually over time and change the circuit performance. By the advances in VLSI fabrication technologies, the reduction of device dimensions such as the channel length, the junction depth and the gate oxide thickness without proportional scaling of the power supply voltage, results in significant increase of the horizontal and vertical electric field in the channel region. Hot carrier induced degradation of MOS transistors is caused by the injection of high-energy electrons and holes into the gate oxide. The oxide damage is in the form of charge trapping and/or interface trap generation which gradually builds up changes the current–voltage characteristics of the transistor. Hot carrier effects cause gradual changes in device characteristics during circuit operation [21–31].

Although the circuit performance is ultimately affected by these changes, the continuous nature of degradation mechanisms presents some special challenges in analysis and estimation of reliability. The damage caused by hot carrier injection affects the transistor characteristics by causing a degradation in transconductance, a shift in the threshold voltage and a change in the drain current capability. This degradation in the device leads to the degradation of circuit performance over time.

With the help of the obtained time-dependent functions, a solution was formed for the change in the drain current by connecting a dependent current source between the drain and source of the MOS transistor, and the change in the threshold voltage represented by connecting a dependent voltage source to the gate. The proposed model for the P-MOS and NMOS transistors can be seen with the related expressions in Figure 20 [22-25,27]. Experimental results and the calculated values for the %□change in the threshold voltage V_{TH} and in the drain current I_D of PMOS transistors for different channel lenghts are illustrated in Fig.21. It seems from the figures that there is good agreement between the experimental results and the calculated values.

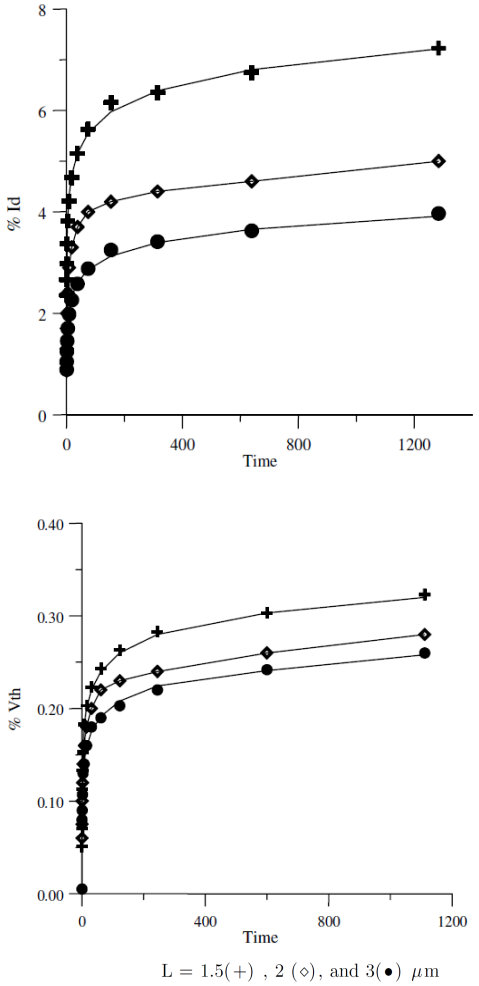

Fig.21. Experimental results and calculated values for the %□ change in the threshold voltage V_{TH} and in the drain current I_D of PMOS transistors for different channel lenghts

The advantages provided by the method proposed is demonstrated on an application example, namely on the properties of the current source-loaded single stage amplifier shown in Fig. 21 which is mostly used as an intermediate stage in operational amplifiers, OTAs, audio amplifiers. Furthermore, it was shown in recent works that the total harmonic distortion of the active-loaded single stage amplifier depends strongly on the operating point where the total harmonic distortion crosses through a minimum at a special biasing point [25]. Any shift in

operating point influences the harmonic distortion properties of the amplifier, The supply voltage was V_{DD} = 5 V and the biasing current was chosen as I_O = 200 µA. A sinusoidal voltage of 1kHz was applied to the input. Changing the input biasing voltage V_{IQ}, the operating point V_{OQ} is shifted along the dc curve. The output signal amplitude was kept constant at V_{OP} = 100mV at each operating point.

Simulation results obtained with accurate model show that the total harmonic distortion crosses through a minimum point of THDmin = 0,177% at V_{OQ} = 2.85 V where the input biasing voltage is V_{IQ} =1,43 V. From Table 3 it can be easily observed that the input biasing voltage providing a mid-point output voltage of V_{OQ} = 2,5 V decreases from V_{IQ} = 1, 44 V to V_{IQ} =1,36 V after a stress time of 20 h. This phenomena is caused by the reduction in MOS threshold voltage due to hot carrier degradation. For a constant input biasing voltage providing minimum total harmonic distortion the operating point is shifted then from V_{OQ} = 2,85 V to V_{OQ} = 0,9 V after the same stress time, therefore an increase in the total harmonic distortion is observed at the output from its minimum value 0.177% to a much higher value of THD=8.48%. It can be clearly seen from the results that the method proposed is useful to predict accurately the shift in the operating point caused by the change in the threshold voltage due to the hot carrier effect. Note that experimental results are obtained for a maximum stress time of 10h. Theoretical results are found to be in good agreement with experiments for this period. Starting from this good agreement and using the Weibull distribution, the circuit behaviour for longer stress times of 15 and 20 h can be also predicted, which demonstrates the prime importance of this work.

Note that the results can be applied easily to the design of analog building blocks [32,33].

Table 1. SPICE simulation results for the dependence of Vth, operating point and THD on stress time

Stress time (h)	V_{th} (V)	V_I for V_O = 2.5 V	THD for V_I = 1.43 V (%)
0	0.53	1.44	0.177
5	0.51449	1.425	1.318
10	0.49368	1.405	3.495
15	0.47094	1.38	6.01
20	0.44733	1.36	8.48

6. Conclusions

The aim of this work was to demonstrate the importance of accurate modeling in the design of electronic circuits. In this work we investigate firstly the accuracy criterion of the models demonstrating on practical circuit examples. The results show that computer-aided design enables the circuit designer to do things which are not possible with other techniques. In other words, computer simulation can be considered as a dry laboratory. Using accurate models the designer can predict several important properties of electronic circuits and systems. The only thing necessary is to use the adequate model with sufficient accuracy, suitable for the purpose. As a result, it is essential in electrical engineering education that the circuit designer have a thorough understanding of the origin of the models commonly utilized and the degree of approximation involved in each.

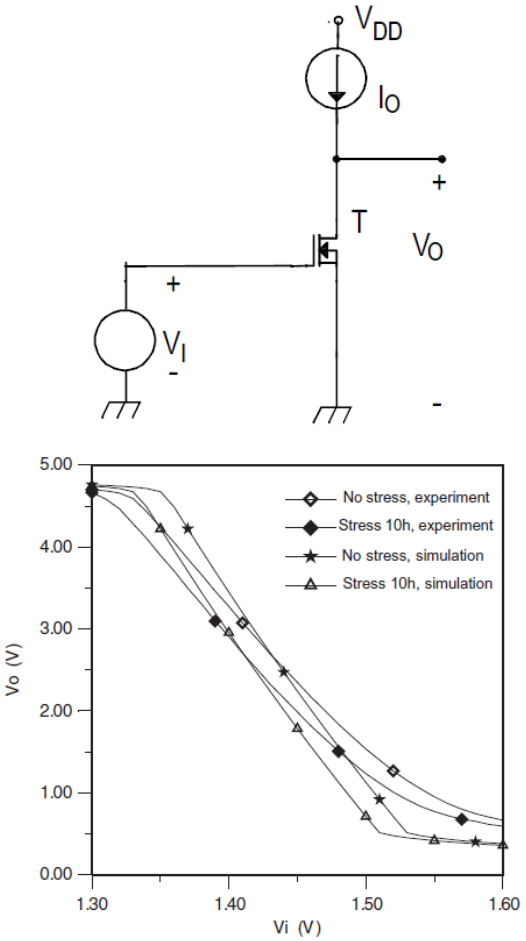

Fig.22. Single stage active-loaded MOS amplifier. Experimental and simulated dependence of dc transfer curve on stress time.

7. References

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