Energy Conversion Efficiency of Single-Phase Transformerless PV Inverters

Ziya Özkan, Ahmet M. Hava

Department of Electrical and Electronics Engineering
Middle East Technical University
ozziya@metu.edu.tr, hava@metu.edu.tr

Abstract

In grid-connected photovoltaic (PV) applications, power semiconductor energy conversion efficiency of PV inverters is one of the major figures of merits to evaluate and compare these systems as the payback ratio of the overall system is tightly related to the energy conversion efficiency and as semiconductor losses comprise the majority of energy losses. In order to wisely choose the PV inverter topology and associated semiconductors, analytic evaluation of semiconductor losses of topologies is required. Furthermore, the evaluation of these losses serves the purpose of designing PV inverters in terms of better thermal management and reliability. In this study, the analytical semiconductor efficiency evaluation of PV inverters promising high efficiency is performed for 3 kW and 10 kW power ratings based on selected semiconductor datasheets and average power per switching cycle (APPSC) method. A comparison of energy efficiency of topologies regarding power levels is provided.

1. Introduction

Transformerless inverters have experienced a major growth in the market recently with their energy conversion efficiency characteristics exceeding 95% [1] due to the absence of either low or a high frequency transformer and the associated losses such as core and copper losses. Another reason for the tendency to use transformerless inverters in PV applications is the reduction of excessive magnetic material, which results in reduced cost and weight. Despite the efficiency advantages of transformerless inverters, leakage currents caused by the capacitive behaviour of PV modules bring limitations to inverter topologies [2], thus, considerable research is put on grid-connected transformerless PV inverter topologies.

In a grid-connected PV system, payback period, reliability, and heatsink volume (therefore size) are in high correlation with the efficiency characteristic of the PV inverter. A common figure of merit for the energy conversion efficiency is the European (EU) efficiency as described in (1) as a function of efficiency at various loading levels with various weight factors.

$$\eta_{EU} = 0.03\cdot\eta_{5\%} + 0.06\cdot\eta_{10\%} + 0.13\cdot\eta_{20\%} + 0.10\cdot\eta_{30\%} + 0.48\cdot\eta_{50\%} + 0.20\cdot\eta_{100\%} \quad (1)$$

Peak thermal stresses of power semiconductor switches are of high interest as the lifetimes of the devices are highly correlated to these stresses [3]. In order to obtain optimal switch configuration for high efficiency, or to estimate junction, case, and heatsink temperature of a semiconductor at a given operating condition, or to choose a suitable converter topology, it is necessary to evaluate the switch losses and efficiency of a given topology before implementing the hardware.

Among the vast variety of PV system configurations, whatever the case or the PV inverter topology selected is, the overall losses in the conversion system are comprised of passive component losses (such as inductor core and copper losses or capacitor equivalent series resistance etc.) and semiconductor losses as shown in Fig. 1. Among these components of losses, power semiconductor switch losses are the focus of this paper as they are the major contributor to the overall losses and becoming an issue for the overall system reliability and lifetime. Moreover, for single-phase PV inverters considered in this paper, the passive component losses are equal for the same power, parameters and switching frequency level, thus the semiconductor efficiency characteristics of topologies define the overall efficiency characteristics of topologies.

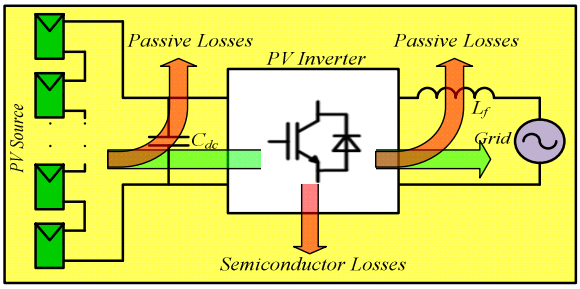

Fig. 1: Grid connected PV system power flow

In power semiconductor switches, total losses are composed of conduction losses, switching losses, and blocking losses. Among these, since they have very low levels of magnitude, blocking losses are generally neglected. Therefore, investigation of switch losses can be conducted under two basic components: conduction losses and switching losses. The major factors effecting conduction and switching losses are the switching stresses that each semiconductor is exposed to (voltage and current stresses), semiconductor parameters (on-state voltage drop, output capacitance, gate charge characteristics etc.), loading level of the converter, and the current duty cycle of each semiconductor.

In this paper, power semiconductor loss calculation using average power per switching cycle (APPSC) is introduced and then single-phase transformerless PV inverter topologies are investigated with their efficiency characterization. PV inverter efficiency characterization with respect to loading is performed by making use of the semiconductor datasheet parameters and individual stresses of semiconductors coupled with the APPSC method proposed in [4], [5]. Based on the results obtained, topology recommendation is made.

“

2. Power Converter Efficiency Calculation

In PV inverters, sizing of power semiconductors should be performed by taking into consideration that, current and voltage stresses that each semiconductor is subject to and that the switching frequency of each semiconductor. In low voltage (<1kV), low power (<5 kW) and high frequency applications (>20kHz) MOSFETs are preferred as active switches whereas IGBTs stand out for higher voltage and lower switching frequency applications [6]. Another difference between these two active semiconductors is in the built-in diodes. In MOSFETs the built-in diode is the parasitic body diode of the semiconductor, thus the reverse recovery characteristic of this diode is not favourable. However, in IGBTs, the built-in diode can be embodied as a fast diode or depending on the application; the diode may be totally omitted. The diodes experiencing rapid turn-off should be fast diodes such that the reverse recovery current has negligible effects.

2.1 Power Semiconductor Loss Formulization

In the selection of power semiconductors, the on-state resistance (R_{DS-ON}) of MOSFETs should be taken into account whereas the on-state resistance and voltage drops of IGBTs and diodes should be considered for better efficiency by decreasing conduction losses. The instantaneous conduction losses of these semiconductors are given in (2)-(4) where they are used in the evaluation of conduction losses by APPSC method. Conversely, the evaluation of switching losses is based on turn-on turn-off switching energies of the semiconductors.

The switching energy loss of a MOSFET is comprised of three basic components. The first component is proportional to the semiconductor on-state current and off-state voltage, and their rise/fall times in the switching cycle under interest. It should be noted that the rise and fall times should be calculated for the designed gate drive characteristics, so that more accurate switching losses can be obtained. Another component of the MOSFET switching losses is the one due the output capacitance of the MOSFET, which is proportional to the square of off-state voltage in a switching period and the MOSFET output capacitance. The last component of MOSFET losses is due to accompanying diode losses on MOSFET that is proportional to diode reverse recovery charge and MOSFET blocking voltage. The total of these MOSFET losses can be formulated as in (5).

In the case of IGBTs, the switching losses are usually given in datasheets for a specific gate drive and blocking voltage. If the IGBT under interest has a built-in diode, the reverse recovery losses may also be included in the given datasheet collector current (I_C) vs. turn-on switching energy (E_{ON}) curve. Similarly, collector current (I_C) vs. turn-off switching energy (E_{OFF}) curves are usually provided in datasheets. These curves are provided for a specific gate resistor, temperature and blocking voltage in datasheets, which can be accurately interpolated with usual methods like least squares polynomial interpolation. These energy loss curves should be scaled accordingly depending on the specific switching conditions such as different blocking voltage, different collector current, and different gate resistor values. Since the semiconductor datasheets neither cover four-dimensional (E_{ON}, I_C, T_j, R_G) curves, nor do they provide this dataset, extrapolation should be used when the required data is missing in semiconductor datasheets. With reasonable approximations, IGBT switching losses can be simply written as in (6).

Diode switching losses are usually neglected, however depending on the reverse recovery charge characteristics and the blocking voltage; they can be taken into account as formulated in (7). Besides, the reverse recovery current may induce considerable amount of additional losses on the accompanying active semiconductor; thus, its effects should not be underestimated. Further information on power semiconductor loss formulization is available in [7] and [8].

$$P_{M-C}(t) = {i_D}^2(t) \cdot R_{DS-ON}(i_D(t), V_{GS}, T_j) \tag{2}$$

$$P_{IGBT-C}(t) = i_C(t) \cdot V_{CE-ON} + {i_C}^2(t) \cdot R_{CE-ON} \tag{3}$$

$$P_{D-C}(t) = i_F(t) \cdot V_{D-ON} + {i_F}^2(t) \cdot R_{D-ON} \tag{4}$$

$$E_{M-SW} = V_{block} I_O \cdot (t_{r-i} + t_{r-v} + t_{f-i} + t_{f-v})/2 + (C_{oss} {V_{block}}^2)/2 + V_{block} Q_{rr} \tag{5}$$

$$E_{IGBT-SW} = E_{ON}(V_{block}, I_C, R_{G-ON}, Q_{rr}) + E_{OFF}(V_{block}, I_C, R_{G-OFF}) \tag{6}$$

$$E_{D-SW} = V_{D-block} \cdot Q_{rr}(I_{F-ON}, \frac{dI_F}{dt})/4 \tag{7}$$

2.2 APPSC Method for Energy Efficiency Calculation

In the APPSC method, the instantaneous conduction loss and the total of turn-on and turn-off switching losses of a specific semiconductor of a power converter topology under the operating constraints (blocking voltage, device current etc.) at a switching cycle are integrated/summed and averaged with respect to time to yield the average power loss of the semiconductor under interest per switching cycle as described in (8)-(9). The evaluation of conduction losses is based on the integration (as in (8)) of instantaneous values of conduction losses given in (2)-(4) whereas the evaluation of switching losses is based on the summation (as in (9)) of the switching energy losses given in (5)-(7).

$$\mathbf{P_{C\text{-}T_s}}[k] = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} P_C(t)dt \tag{8}$$

$$\mathbf{P_{S\text{-}T_s}}[k] = \frac{1}{T_s} \sum E_{SW}\Big|_{kT_s}^{(k+1)T_s} \tag{9}$$

For dc-dc converters, the duty cycle of each semiconductor is constant at steady state, thus the evaluation of the conduction and switching losses is straightforward. In the case of voltage-source inverters (such as the PV inverters investigated in this paper), the duty cycle of each semiconductor is time varying. Furthermore, the duty cycle of a semiconductor switch and the duty cycle of current flowing through the switch may not be same so that the definition of current duty cycle function (CDF) [4] is useful in evaluating (8) and (9). The CDF of a switch is dependent on where the switch is located in a converter topology, how the output current is modulated, and leads to evaluation of average and RMS values of semiconductor current at each switching cycle. For example the evaluation of IGBT conduction losses are formulated at k^{th} switching cycle by making use of CDF (d_i) in (10). In switching loss calculations, a function of CDF as given in (11) appears as '1' or '0' in the evaluation of switching losses. In (12), IGBT switching losses are given based on the function of CDF. This function brings the switching losses to zero at a switching cycle when the semiconductor is totally on or off. Having the average power loss per switching cycle of each semiconductor calculated,

"

semiconductor efficiency characterization of a PV inverter topology can be achieved for the set of chosen semiconductors.

$$\mathbf{P}_{\mathbf{I\text{-}C\text{-}T_x}}[k] = d_i(k\omega T_s)\cdot\left[\, i_C(k\omega T_s)\cdot V_{CE-ON} + i_C{}^2(k\omega T_s)\cdot R_{CE-ON}(T_j)\right] \quad (10)$$

$$f(d_i(k\omega T_s)) \triangleq \operatorname{sgn}(d_i(k\omega T_s))\cdot\operatorname{sgn}(1-d_i(k\omega T_s)) \quad (11)$$

$$\mathbf{P}_{\mathbf{I\text{-}S\text{-}T_x}}[k] = f(d_i(k\omega T_s))\cdot\frac{1}{T_s}\left[\mathbf{Z}_{\mathbf{E\text{-}ON}}(i_C(k\omega T_s)) + \mathbf{Z}_{\mathbf{E\text{-}OFF}}(i_C(k\omega T_s))\right] \quad (12)$$

In Fig. 2, the algorithm for the semiconductor efficiency characterization of a power electronic converter is summarized. In the algorithm, full grid cycle is divided into the switching events and for all the switching events, average power loss per switching cycle is calculated by taking into consideration that the switching constraints and the semiconductor parameters of the semiconductor under evaluation. For all percent loading levels, the total energy loss is stored and the procedure continues until the losses for all semiconductors in a given PV inverter topology are calculated. With the summation of each switch losses at each percent loading level, total loss of the converter at each loading level can be found. Thus, with this method, semiconductor efficiency with respect to loading level can be obtained.

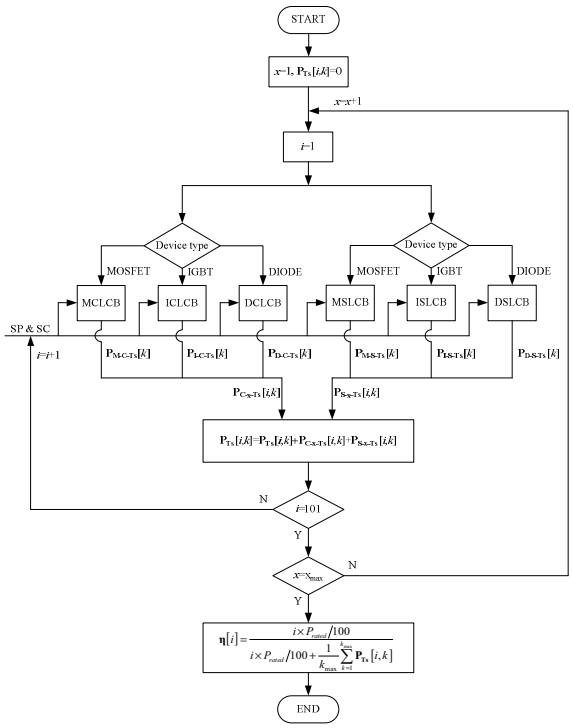

Fig. 2 Semiconductor efficiency characterization algorithm f a PEC for various loading levels (i:loading index, x: device index)

3. Transformerless PV Inverters and Their Semiconductor Efficiency Characterization

In the range of a few kW up to tens of kW, PV inverters can be implemented without a transformer (transformerless). As compared to transformer based counterparts, transformerless systems have lower cost, higher reliability and higher energy conversion efficiency advantages [6], so that transformerless PV inverters have a higher market share. In spite of the benefits of transformerless PV inverters, these inverters may suffer from the leakage currents caused by the capacitive structure of PV modules constituting a current flow path when grounded. Therefore, engineering efforts put on the research on low leakage current PV inverter topologies uniting the high efficiency, low cost, lightweight benefits with the low leakage current characteristics.

Among grid connected transformerless PV inverter topologies, zero-state decoupled topologies are developed both having high efficiency and low leakage current characteristics. The low leakage current characteristic of these topologies is due to the decoupling mechanism at zero states as suggested in [9]. With three-level output voltage characteristics resulting in lower filter inductor current ripple, passive losses are reduced, thus these topologies become favourable for PV applications.

In Fig. 3, generic gate drive signals for zero-state decoupling class of transformerless PV inverters are depicted for unity power factor (PF) operation. In Fig. 4(a)-(f) the zero-state decoupled topologies [9] are depicted. The gate drive signals in Fig. 3 are assigned nearby each active semiconductor of each topology to clarify the modulation of output voltage.

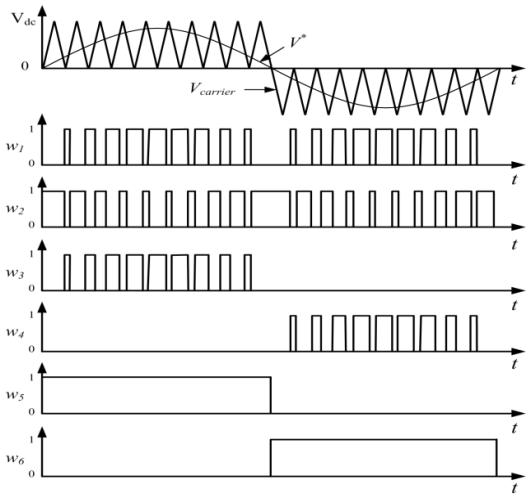

Fig. 3 Generic gate logic signals of controlled switches of investigated topologies for PF=1

In Fig. 4(a), the commercial H5 topology is depicted. From the gate signals assigned nearby from Fig. 3, the active semiconductors S1, S2, and S4 are clocked in high frequency so that they can be realized as MOSFETs, especially up to 5 kW power rating. The semiconductors S1 and S3 are low frequency switches and their anti-parallel diodes have high frequency currents so that these switches can be implemented as IGBTs with their fast diodes. In Fig. 4(b), the HERIC topology is shown which has two semiconductors only on current path during active and zero states. Based on the gate drive signals, the switches S1-S4 are high frequency switches, so that they can be embodied as MOSFETs. The switches S5, S6 are preferably IGBTs as they require anti-parallel fast diodes. The H6 topology, shown in Fig. 4(c), has low frequency clocked bridge switches (S1-S4) such that they freewheel the line current at grid frequency. However, since the diodes of these switches do not carry current at unity PF operation, these active switches can be implemented as MOSFETs also. It should be noted that, the freewheeling diode (D7) should be selected as a high frequency diode since during the operation of the converter this diode is exposed to rapid and high frequency turn-off.

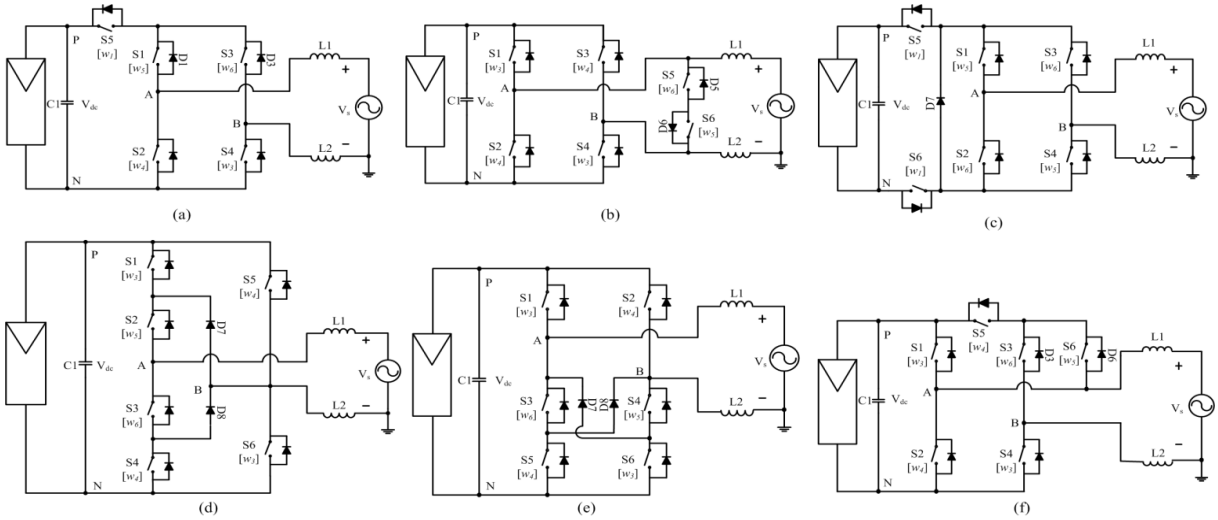

Fig. 4 Evaluated single-phase transformerless PV inverters; (a) H5, (b) Heric, (c) H6, (d) NPC+HB, (e) H6V, (f) P6

In Fig. 4(d), another H6 type converter consisting of a single neutral point clamped (NPC) topology leg and a half bridge (HB) topology leg (thus called NPC+HB in this paper) is illustrated. This converter is invented to avoid the usage of IGBTs and their excessive conduction losses. With MOSFETs, the conduction losses are aimed to be reduced. However, since the number of semiconductors on the current path at active vectors is three, this advantage may be lost at high loading levels. For unity PF operation, only the diodes D7 and D8 should be fast diodes. In Fig. 4(e), H6V topology is depicted. In this topology, similar to NPC+HB topology, active switches may be realized as MOSFETs at low power levels (<5 kW) as the freewheeling of the line current at zero states is provided through external fast diodes (D7, D8). The active switches S3 and S4 are clocked at grid frequency and the rest of active switches are clocked at high frequency as the gate signals are assigned nearby the switches from Fig. 3. The switches S1, S2, S4, and S5 shown in topology in Fig. 4(f) are clocked at high frequency so that they can be preferably implemented as MOSFETs, whereas the switches S3 and S6 are grid frequency switches wherein their diodes are exposed to sudden high frequency zero state currents. Thus, the switches S3 and S6 should be realized as IGBTs.

To apply the power semiconductor efficiency characterization approach described in the foregoing section on single-phase transformerless PV inverters, two case studies are performed. The semiconductor efficiencies of transformerless PV inverters with respect to loading are characterized for 3 kW and 10 kW power ratings (PF=1) at 20 kHz switching frequency. For 3 kW case, MOSFETs are assumed as active switches as described in previous paragraphs and IGBTs with fast diodes are assumed for grid frequency active switches. In Table-1 and Table-2, the semiconductor parameters for the efficiency characterization are given for the selected MOSFET, IGBT, and IGBT's anti-parallel diode. For 10 kW case, all of the semiconductors are assumed as IGBTs (parameters provided in Table-3).

In Fig. 5, the power semiconductor efficiency characteristics of the single-phase transformerless PV inverters are illustrated with respect to loading both for 3 kW (Fig. 5(a)) and 10 kW (Fig. 5(b)) designs. In both designs, the efficiency characteristics of each topology peak around 0.5 kW and then decrease as the loading increases. The decrease is due to the conduction losses as they increase with the square of the output current (or loading). Among the topologies, the Heric topology exhibits the highest efficiency characteristics, as its number of semiconductors on the output current path is two both in active states and zero states.

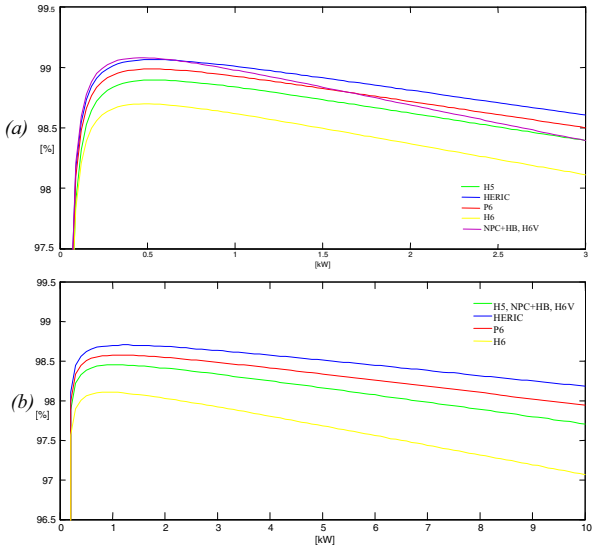

Fig. 5 Semiconductor efficiency characteristics of the single-phase topologies with respect to loading for 3 kW (a) and 10 kW (b)

In the 3 kW case, the NPC+HB and the H6V topologies have better efficiency than the P6 topology at light load as only MOSFETs are utilized as controlled switches in these topologies. Due to their high number of switches on the line current path at active states (three), their efficiency characteristics deteriorate as the loading increases whereas P6 topology keeps flat efficiency curve. Due to number of switches on the current path and the active switch embodiments as IGBTs, H5 and H6 topologies have lower efficiency as compared to Heric, P6, NPC+HB, and H6V topologies. In the 10 kW case, there are clear efficiency differences among the topologies as all the active switches are selected as IGBTs. This difference is due to the number of switches on the current path increasing the total conduction losses of the converter.

"

In Table-4, EU efficiencies of the investigated PV inverter topologies are tabulated for both 3 and 10 kW cases based on power semiconductor efficiency characteristics obtained. Among all, Heric topology yields the highest EU efficiency, whereas H6 topology is found to have the worst. For 3 kW, the differences among topologies are in the order of 0.1%, however, in the 10 kW case, the EU efficiencies of topologies may differ in the order of 1%. Although it appears small, 1% increase in efficiency will yield quite considerable decrease in the payback period of a PV inverter. Another conclusion involves the trade off between cost and efficiency. In low kW ratings using all MOSFET inverter yields higher efficiency but costs more, while at high power the IGBT inverter provides higher efficiency and lower cost solution.

Table-4 Semiconductor loss based EU efficiencies of topologies

Prated	H5	HERIC	H6	NPC+HB	H6V	P6
3 kW	98.65	98.88	98.47	98.78	98.78	98.77
10 kW	98.14	98.47	98.31	98.15	98.15	97.63

4. Conclusion

In this paper, efficiency characterizations of single-phase grid-connected transformerless PV inverter topologies based on semiconductor datasheets are performed, as they are vital for the design and the optimization issues. First, MOSFET, IGBT, and diode losses are modelled. For each device type, the conduction losses are formulated based on the instantaneous power, whereas the switching losses are formulated based on switching energies of the semiconductors, where the necessary parameters are extracted from datasheets and extrapolated when they are absent. After the investigation of device loss characterization, the APPSC method for power converter loss calculation is given. Two case studies for 3 kW (IGBT+MOSFET based) and 10 kW (IGBT based) are performed and the transformerless PV inverters are characterized in terms of efficiency. Based on these studies, it is observed that MOSFET based implementations may have higher efficiency whereas IGBT based implementations have lower price. When the power rating of a PV inverter topology increases (beyond 5 kW), the choice of active semiconductors turns out to be IGBTs rather than MOSFETs due to current carrying capabilities. Under such circumstances, the number of switches of a PV inverter topology on the line current defines the overall efficiency characteristics. When the power level is increased efficiency gaps between topologies become distinctive, therefore the right selection of inverter topology for larger power ratings gains higher importance.

5. References

[1] Photon Laboratory Inverter Test, available on: http://www.photon.info/upload/Inverter_TestInfo_EN_971.pdf/, last access on 17/07/2013.

[2] J.M.A. Myrzik, M. Calais, "String and module integrated inverters for single-phase grid-connected photovoltaic systems—A review" in Proc. IEEE Bologna Power Tech Conf., vol. 2, pp. 8, Jun. 2003.

[3] S. Young and W. Choi, "Switching loss estimation of high voltage power MOSFET in power factor correction pre-regulator", Applied Power Electronics Conference and Exposition (APEC), pp. 463-467, March 2011.

[4] Z. Özkan, "Leakage Current and Energy Efficiency Analyses of Single Phase Grid Connected Multi-kVA Transformerless Photovoltaic Inverters," M.Sc. Thesis, Middle East Technical University, Dept. of Electrical and Electronics Eng., Ankara, February 2012.

[5] Z. Özkan, A.M. Hava, "Güç Elektroniği Dönüştürücülerinin Yarıiletken Veriyapraklarına Dayalı Verim Hesaplama Yöntemi", ELECO 2012, Bursa, pp. 460-464, Dec. 2012.

[6] Carl Blake, Chris Bull, "IGBT or MOSFET: Choose Wisely", International Rectifier App. Note, available on: http://www.irf.com/technical-info/whitepaper/choosewisely.pdf, last access on 17/07/2013.

[7] D. Graovac, M. Pürschel ve A. Kiep, "MOSFET Power Losses Calculation Using the Data-Sheet Parameters", Infenion Uygulama Notu, V1.1, Temmuz 2006.

[8] D. Graovac ve M. Pürschel, "IGBT Power Losses Calculation Using the Data-Sheet Parameters", Infineon Uygulama Notu, V1.1, Ocak 2009.

[9] Z. Özkan and A. M. Hava, "Leakage Current Analysis of Grid Connected Transformerless Solar Inverters with Zero Vector Isolation," IEEE-ECCE 2011 Conference, September 2011, Phoenix, Arizona, USA, pp. 2460-2466.

6. Appendix

Table-1 MOSFET parameters for semiconductor efficiency characterization of 3 kW design

MOSFET	$R_{D\text{-}ON}$ @ 10A	T_{coeff} @100 C	V_{plateu} (V)	T_{ri} (ns)	T_{fi} (ns)	$R_{g\text{-}test}$ (Ω)	C_{oss} (pF)	Q_{gate} (nC)
FCA76N60N	0.028	1.75	4.7	24	32	4.7	914	218

Table-2 IGBT and anti-parallel diode parameters for semiconductor efficiency characterization of 3 kW design

IGBT+DIODE	$V_{CE\text{-}ON}$ (V)	R_{on} @10A	T_{coeff} @ 125 C	$V_{D\text{-}ON}$ (V)	$R_{D\text{-}ON}$ (Ω)	Q_{rr} (nC)	$I_{Qrr\text{-}test}$ (A)	$-di_F/dt$ (A/μsec)
APT150GN60LDQ4(G)	0.5	0.015	1	0.5	0.015	1000	50	200

Table-3 IGBT and anti-parallel diode parameters for semiconductor efficiency characterization of 10 kW design

IGBT+DIODE	$V_{CE\text{-}ON}$ (V)	R_{on} @10A	$V_{D\text{-}ON}$ (V)	$R_{D\text{-}ON}$ (Ω)	$\begin{bmatrix}\mathbf{Z}_{E\text{-}ON\text{-}t}[2]\\ \mathbf{Z}_{E\text{-}ON\text{-}t}[1]\\ \mathbf{Z}_{E\text{-}ON\text{-}t}[0]\end{bmatrix}$	$\begin{bmatrix}\mathbf{Z}_{E\text{-}OFF\text{-}t}[2]\\ \mathbf{Z}_{E\text{-}OFF\text{-}t}[1]\\ \mathbf{Z}_{E\text{-}OFF\text{-}t}[0]\end{bmatrix}$	$s_{f\text{-}ON}$	$s_{f\text{-}OFF}$
IXXK100N60C3H1	0.8	0.017	0.8	0.01	$\begin{bmatrix}0.002\\ 0.0297\\ 0.0132\end{bmatrix}$	$\begin{bmatrix}-0.0001\\ 0.0277\\ 0.0172\end{bmatrix}$	0.91	0.9

"