Reduced Diode Clamped Multilevel Converter with a Modified Control Method

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Abstract

This paper presents a new configuration of Neutral-point-clamped (NPC) or Diode Clamped converters called Reduced Diode Clamped Multilevel (RDCM) Converter. In this topology, the number of clamping diodes and high frequency switches are decreased while the voltage ratings of them during a full cycle are kept constant. Compared with conventional NPC or Diode Clamped converters, The main advantages of the proposed converter are increasing the effective value and the number of output voltage levels up to twice, improving the output voltage frequency spectrum and lowering the number of components which can result in the decreasment of the converter's size and cost. These improvements are achieved by adding only two low-frequency switches to a Half-bridge Diode-Clamped Multilevel converter configuration. Also, This converter is controlled by a modified pulse width modulation PWM based control method. The circuit is simulated using PSCAD/EMTDC software and simulation results are presented to validate the effectiveness and advantages of the proposed configuration.

1. Introduction

Multilevel converters are very absorbing alternative in medium and high voltage applications due to their better harmonic performance and lower switching losses and voltage stress. As a result, multilevel converters improvement can enhance the application of high power AC motor drives, active power filters, reactive power compensation and FACTS devices [1-6].

A multilevel converter, which includes an array of power semiconductors and capacitor voltage sources, can synthesize a desired output voltage from several levels of dc voltages as inputs. The term multilevel was introduced by Nabae et al and the first topology presented was the series H-bridge design with three-levels. The H-bridge topology was followed by the diode-clamped converter, presented in the early 80's, that utilized a bank of series capacitors. The well-known multilevel topologies are diode-clamped or neutral-point-clamped (NPC) type [2, 3], capacitor-clamped or flying capacitor type [1, 4], and cascaded H-bridge type [5-7] with separate dc inputs.

Among the conventional multilevel inverters, the Diode Clamped multilevel converter is the original multilevel invention and probably the most widely used topology especially in high power applications. Therefore, the Diode Clamped multilevel converter becomes the most widely used topology in the motor drives and utility applications [7-9]. However, there still have some challenges to implement the multilevel converters when the number of levels used is increased. This topology is well defined but cumbersome to implement for levels beyond five because of the dc capacitor voltage unbalance problem, and the excessive number of the clamping diodes [10]. Therefore, there is a need to simplify the circuit topology to facilitate a higher level realization. Consequently, in this paper, a new configuration of Diode-Clamped converter has been proposed to reduce the number and rating of the converter components specially clamping diodes while the output voltage levels and its RMS are increased.

In the following section a brief overview of conventional Diode Clamped multilevel converter and some of it's recently derivatives and their properties are presented. Then, the new Diode-Clamped Multilevel converter based configuration which is achieved by adding only two low-frequency switches to a Half-bridge NPC converter configuration and its modified control strategy based on the Pulse Width Modulation (PWM) technique are proposed. The main advantages of the proposed converter are increasing the RMS and the number of output voltage levels up to twice, improving the output voltage frequency spectrum, and reducing installation area and converter cost, especially in higher number of cells and voltage levels, due to decreasing the number of components. In this topology, the number of high frequency switches and capacitors are decreased to half and the number of clamping diodes is decreased more while the voltage ratings of capacitors and switches during a full cycle are kept constant. Finally, Simulation results are proposed for a single phase 9 level Reduced Diode-Clamp multilevel converter to confirm the effectiveness and advantages of the proposed configuration and its control method.

2. Diode Clamped based multilevel converters

The Diode Clamped multilevel converter, which came from the Neutral-Point Clamped converter, was invented in 1979 [2]. This converter is now a standard topology in industry [1-4] on its 3-level version and is based on clamping diodes dc used to connect the neutral point to the midpoint of the switches.

A three-level Diode Clamped converter is shown in Fig. 1(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors N can be defined as the neutral point. The output voltage has three states: $-E/2$, 0 and $E/2$. For voltage level $E/2$, switches S_1 and S_2 need to be turned on; for $-E/2$, switches $\overline{S_1}$ and $\overline{S_2}$ need to be turned on; and for the 0 level, S_2 and $\bar{S}_1$ need to be turned on. The main components make this circuit distinguished from a conventional two-level converter are the diodes (D_1 and $\bar{D}_1$). These two diodes clamp the switch voltage in order to half the level of the dc-bus voltage. When both turn on, the voltage across A and 0 is E , i.e.$V_{A0} = E$. In this case, $\bar{D}_1$ balances out the voltage sharing between $\bar{S}_1$ and $\bar{S}_2$ with $\bar{S}_1$ blocking the voltage across C_1 and $\bar{S}_2$ blocking the voltage across C_2 . Notice that output voltage V_{AN} is ac, and V_{A0} is dc.

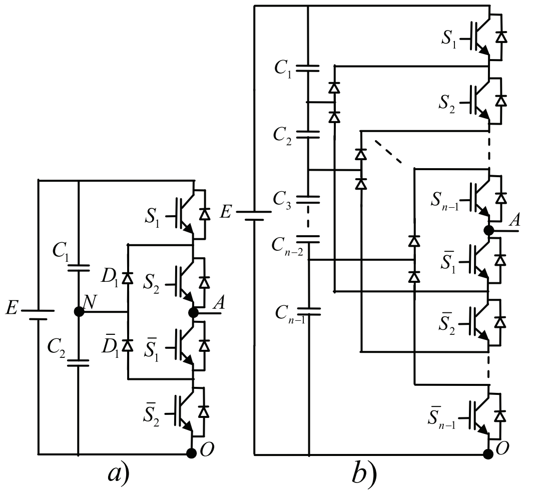


Fig. 1. a) Three-level and b) $n-level$ single phase half-bridge Diode-Clamped converter

The diode-clamped converter can be easily extended to more levels. Fig. 1(b) shows the $n-level$ versions of single phase Diode-Clamped converter, where $2n-2$ high frequency switches with $n-1$ capacitors in the dc link are required. Additional diodes are then used to clamp the extra inter-switch voltage nodes. The maximum reverse blocking voltage of each clamping diode depends on its position in the circuit, and therefore the number of the diodes required for each phase will be $(n-1)\times(n-2)$.

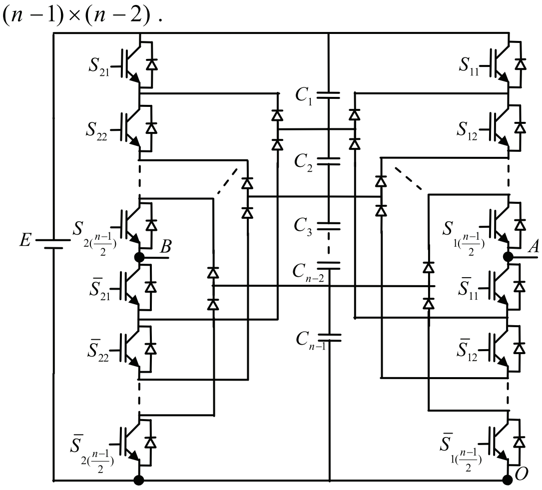


Fig. 2. $n-level$ single phase full-bridge Diode-Clamped converter

In the following a brief summary of some recently presented derivative topologies of Diode-Clamped converter are provided.

One of main alternative topology based on the Diode Clamped converter is the Full-Bridge topology of this converter. Fig. 2 shows an $n-level$ Full-Bridge Diode Clamped topology. This structure uses two parallel arrays of switches to increase the number of output voltage levels. The main advantages of this configuration are that the number of capacitors and clamping diodes are reduced [10].

Diode-clamp cascade converter is Another configuration of NPC converter which is based on the connection of several three-level diode-clamp converter modules, and the multilevel waveform is synthesized by adding each converter output voltage [11]. Also, in [12], a hybrid diode-clamp cascade multilevel converter (HDCMC) has been presented where the concept of the converter is based on the connection of multiple diode-clamp converter modules with different dc bus voltages. Furthermore, in [13] a hybrid cascade multilevel converter that is the series-connection of a diode-clamp converter and several H-bridge converters with equal dc bus voltage have been introduced to improve the operation of higher voltage devices and faster devices in synergism.

Also, in [4] an improved new topology for multilevel converters based on the mixture of the two most popular multilevel topologies, Diode Clamped Multilevel converter and Cascaded Multicell converter called Mixed Cascaded Diode Clamped Multilevel has been intoduced. This topology is achieved by adding four low-frequency switches to a series of cascaded Half-bridge Diode-Clamped Multilevel converters configuration and presents some advantages especially for high power applications. An example of the $n-level$ converter is shown in Fig. 3.

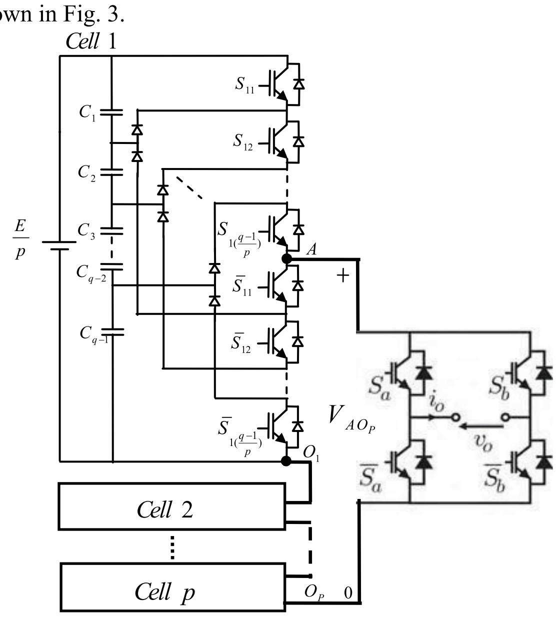


Fig. 3. $n=[2p\times(q-1)+1]-level$ single phase Mixed Cascaded Diode-Clamped converter

In [9] a diode-clamped multilevel converter topology with reduced number of clamping diodes has been presented. The topology uses a combination of multilevel converter cells with different number of levels. Assuming that the number of levels of the middle cell is n_1, and the number of the two other cells are n_2. The number of output voltage levels (n), is given by [9]:

$$n = n_1 + 2(n_2 - 1) \quad (1)$$

3. Proposed Reduced Diode Clamped Multilevel converter

In this section, the proposed configuration of RDCM converter with its associated modified control method is explained.

3.1. Proposed Configuration

As it was mentioned, considering Fig. 1.b for a $n-level$ single phase half-bridge Diode-Clamped converter, if V_{A0} is selected as output voltage, this converter can generate a multilevel positive output voltage with $n-level$. Consequently, in order to generate the negative part of output voltage, two low-frequency switches (T, $\bar{T}$) are added to the conventional configuration of half-bridge Diode Clamped converter. This new proposed Reduced Diode Clamped multilevel converter can generate $(2n+1)-level$ for output voltage. Two additional switches work with low-switching frequency, and generally, are switched twice during a full cycle of the fundamental output voltage. switch $\bar{T}$ will be on for positive output voltage and the switch T will be on for negative output voltage. Fig. 4 shows a $2(n-1)$ switch $(2n-1)-level$ configuration of proposed RDCM converter.

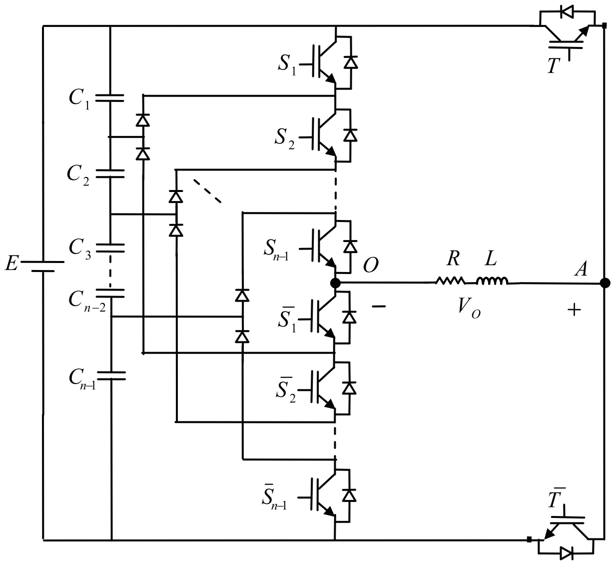
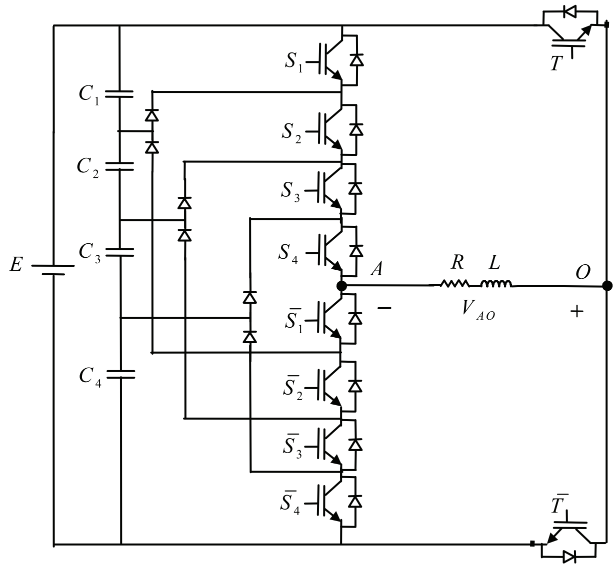


Fig. 4. $2(n-1)$ switch $(2n-1)-level$ single phase Reduced Diode Clamped multilevel converter

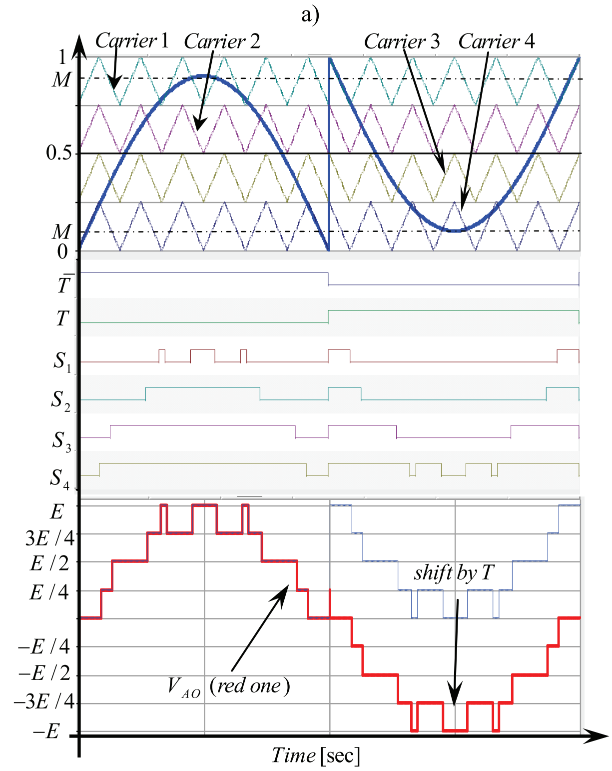
3.2. Modified PWM Based Control Method

A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM). Level-shifted PWM is widely used in Diode clamped inverters. In [14], it is shown that this modulation technique is applied to a five-level inverter. This modulation technique produces an uneven distribution of power among cells, which produces a high harmonic content in the input current. In [14], this drawback is avoided using a rotating carrier, which balances the power of each cell.

İn order to verify the modified control method of proposed RDCM converter, a 9-level configuration of the proposed topology, its modified control method based on level shfted PWM and the obtained output voltage waveform are shown in Fig. 5. Also, the output voltage levels and switching states of this 9-level RDCM converter are shown in Table I.



a)



b)

Fig. 5. Proposed 9-level RDCM converter's a) configuration, b) modified Level-shifted carrier-based SPWM control strategy, switching states and generated voltage

Table 2. Comparison of conventional Diode Clamped and Cascaded multilevel converters with proposed RDCM converter for the identical output voltage (n level)

(n : No. of *generated levels*)	Cascade Multicll	Diode Clamped		Proposed Reduced Diode Clamped Converter
		Half bridge	*Full bridge*	
No. of High Frequency Switches	$2n-2$	$2n-2$	$2n-2$	$n-1$
No. of Low Frequency Switches	0	0	0	2
No. of Capacitors	0	$\frac{2n-4}{2}$	$\frac{n-1}{2}$	$\frac{n-1}{2}$
No. of Diodes	0	$(n-1)(n-2)$	$\frac{(n-1)(n-3)}{2}$	$\frac{(n-1)(n-3)}{4}$
No. of dc Sources	$2n-4$	1	1	1

In order to obtain the full value of the DC source voltage, i.e. $\pm E$, for both positive and negative peaks of output voltage of the proposed RDCM converter, switches T and $\overline{T}$ play an important role. As shown in Fig. 5.b, this achievement makes it possible to double the RMS value of the output voltage and the number of output voltage levels. The effect of switch T is a negative shift of the voltage, equal to $-E$, in the second half cycle to form the output voltage, V_{AO} . As a result, the reference signal must be shifted one positive unit in the second half cycle to offset negative shift of the voltage made by switch T , as shown in Fig. 5.b.

Table 1. Switching states of Proposed 9-level RDCM converter

Output Voltage Level	States		
	$\overline{T}$	T	(S1,S2,S3,S4)
$+E$	1	0	(1,1,1,1)
$+\frac{3}{4}E$	1	0	(1,1,1,0)
$+\frac{2}{4}E$	1	0	(1,1,0,0)
$+\frac{1}{4}E$	1	0	(1,0,0,0)
0	1	0	(0,0,0,0)
	0	1	(1,1,1,1)
$-\frac{1}{4}E$	0	1	(1,1,1,0)
$-\frac{2}{4}E$	0	1	(1,1,0,0)
$-\frac{3}{4}E$	0	1	(1,0,0,0)
$-E$	0	1	(0,0,0,0)

Also, Tabel 2 shows the comparison of the main properties of proposed RDCM converter with conventional Diode Clamped converters.

Considering Fig. 5 and Table 2, the main advantages of the proposed converter are increasing the RMS and the number of output voltage levels up to twice, improving the output voltage frequency spectrum, and reducing installation area and converter cost, especially in higher number of cells and voltage levels, due to decreasing the number of components. Consequently, in this topology, the number of high frequency switches and capacitors are decreased to half and the number of clamping diodes is decreased more while the voltage ratings of capacitors and switches during a full cycle are kept constant.

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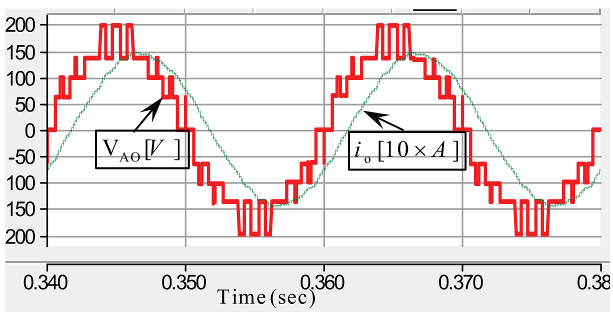
4. Simulation Results

To verify the good performance and effectiveness of the proposed RDCM converter, a single-phase 9-level Reduced Diode Clamped Multilevel converter is simulated and implemented based on the proposed configuration shown in Fig. 5.a. The PSCAD/EMTDC software has been used for simulation. The main converter and load parameters used in simulations are defined in Table 3.

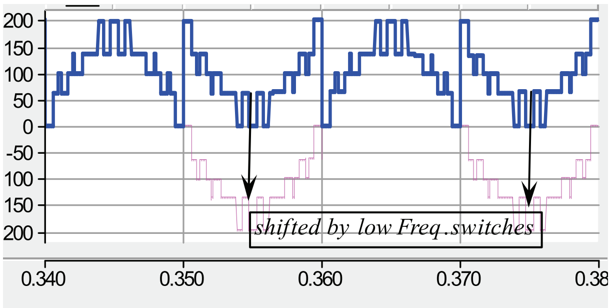
Table 3. Main parameters of converters and loads used in simulations

Parameters	Values
DC voltage (E)	200 V
capacitors (C)	10mF
Fundamental output voltage frequency	50 Hz
Switching frequency ($f_{switching}$)	1000Hz
Resistive-Inductive load (R_L ; L_L)	10Ω; 30mH

The simulation results of the output voltage and current of a resistive-inductive load and the voltage of half bridge Diode Clamped part of the proposed converter and its negative part shift, for the 9-level RDCM are shown in Figs. 6. a and b, respectively. The proposed modified level shifted PWM control scheme with switching frequency of 1000 Hz ($f_{switching}=1000Hz$) and a modulation index equal to 0.9 ($M=0.9$) has been used to control the converter.



a)



b)

Fig. 6. Proposed 9-level RDCM converter's a) output voltage and current, b) half bridge Diode Clamped part voltage and the of its negative part shift

Also, the main generated harmonics are around 3000*Hz* with THD of 17% that demonstrates the improvements of output waveform and reduction of distortions

5. Conclusions

In recent years, the development of multicell converters has been extensively considered due to their capability of handling medium voltage and high power industrial applications with improving the output signal frequency spectrum. In this paper a new topology of Diode Clamped Multilevel converters with fewer number of power electronic switches called Reduced Diode Clamped Multilevel (RDCM) converter has been introduced. Compared with conventional Diode Clamped based converters, the progress of doubling the rms of output voltage and the number of output voltage levels in the proposed RDCM converter makes it possible to decrease the number of clamping diodes, high-frequency switches and dc capacitors by 50%, at least. Consequently, the installation area and total cost of converter, especially in higher number of cells and voltage levels, due to decreasing the number of components can be decreased.

Also, the simulation results verified the good performance of the proposed configuration and its associated control scheme. The authors believe that the proposed configuration has a good potential for high-power/high-voltage applications

6. References

[1] J. Rodríguez, J. S. Lai, F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 49, pp. 724–738, August 2002.

[2] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," IEEE Transactions on Industry Applications, vol. 17, no. 5, pp. 518–523, 1981.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2219–2230, July 2010.

[4] S.H. Hosseini, M. Sadeghi, "A New Mixed Cascaded Diode Clamped Multilevel Converter for High Power Applications," in progress, IEEE Electrical Power and Energy Conference (EPEC 2011), Winnipeg, MB, Canada, October 3-5, 2011.

[5] E. Babaei, "A Cascade multilevel converter topology with reduced number of switches", IEEE Transactions on. PowerElectronics, vol. 23, no. 6, pp. 2657-2664, Nov. 2008.

[6] M. Malinowski K. Gopakumar, J. Rodriguez, M. A. Pérez,, "A survey on cascaded multilevel inverters," IEEE Transactions on Industrial Electronics., vol. 57, no. 7, pp. 1-10, July 2010

[7] F. Z. Peng, W. Qian, D. Cao, "Recent Advances in Multilevel Converter/Inverter Topologies and Applications," International Power Electronics Conference (IPEC), 2010, pp 492-501.

[8] L.M. Tolbert, F.Z. Peng, and T.G. Habetler, "Multilevel Converter for Large Electric Drives," IEEE Transactions on Industry Applications,volume 35, number 1, pages 36-44, January/February 1999.

[9] Z. Pan, F. Z. Peng, V. Stefanovic, M. Leuthen, "A Diode-Clamped Multilevel Converter with Reduced Number of Clamping Diodes," IEEE Nineteenth Annual Applied Power Electronics Conference and Exposition, APEC '04, vol.2, pp 820-824.

[10] Y. Xue, M. ManjrekarA, "A New Class of Single-Phase Multilevel Inverters," 2nd IEEE International Symposium on Power Electronics for DG Systems, PEDG '10, pp 565-571.

[11] M. D. Manjrekar, P. K. Steimer, T. A. Lipo, "Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications," IEEE Transactions on Industrial Electronics, vol. 36, no. 3, pp. 834–841, June 2000.

[12] K. Ding, Y. Zou, Z. Wang, Z. Wu, Y. Zhang, " A Novel Hybrid Diode-clamp Cascade Multilevel Converter for High Power application," IEEE Industry Applications Conference, 39th IAS Annual Meeting. 2004, vol.2, pp 820-827.

[13] Y. Xu, Y. Zou, "Spectral Analysis of an Improved Hybrid Cascade Multilevel Converter," IEEE 6th International Power Electronics and Motion Control Conference, IPEMC '09. vol.2, pp 1430-1434.

[14] M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, "Level-shifted PWM for cascaded multilevel inverters with even power distribution," IEEE Power Electron. Spec. Conf., Jun. 2007, pp. 2373–2378.