A Novel Switching Signals Generation Method for Hybrid Multilevel Inverters

M. Emin MERAL, Lütfü SARIBULUT, Ahmet TEKE and Mehmet TÜMAY

Çukurova University, Department of Electrical and Electronics Engineering, Balcalı /Adana, TURKEY
emeral@cu.edu.tr, lsaribulut@cu.edu.tr, ahmetteke@cu.edu.tr, mtumay@cu.edu.tr

Abstract

Use of multilevel inverters is becoming more popular in the recent years. Various topologies and modulation methods have been reported for utility and drive applications in the recent literature. Hybrid multilevel structures are the new multilevel inverter topologies where the cascaded series inverters have different internal DC bus voltages and/or modulated quite differently. This paper introduces a novel switching signals generation (modulation) method for hybrid multilevel inverters. This method is new and based on reference signal tracking. The structure of modeled hybrid multilevel inverter and operating principles of the proposed method are presented. The proposed method is verified by computer simulations using PSCAD/EMTDC. The waveform and THD values are presented and analyzed, which prove the validity of the proposed method.

1. Introduction

Inverters are used in both single-phase and three-phase AC systems. A half-bridge inverter is the simplest topology, which is used to produce a two-level square-wave output waveform. A center-tapped voltage source is needed in such a topology. The full-bridge topology is used to synthesize both two-level and three-level output waveforms. However, there are many limitations for these conventional two-level and three-level inverters in handling high voltage and reduction in harmonic distortion [1].

Multilevel inverter concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps for higher voltage and reduction in harmonic distortion. Such multilevel inverter topology permits a significant reduction of the output filter and an improvement of the efficiency greater than 98% for loads greater than 40% of its rated output power [2]. Some applications for these new inverters include large industrial drives, flexible AC transmission systems (FACTS), vehicle propulsion, multilevel rectifier, interface with distributed generation resources, custom power and power quality applications [3]. Multilevel topology has even been applied to low-voltage applications [4].

For multilevel inverters, there are several well-known Pulse Width Modulation (PWM) methods, which can be classified as follows: selective harmonic elimination PWM (SHEPWM) [5], space vector PWM (SVPWM) [6] and sinusoidal PWM (SPWM) [7]. These multilevel modulation strategies are adapted from the well-established two-level PWM. Among the above methods, the SPWM is the most popular one and its popularity is partly due to its simplicity [8]. The SPWM for a multilevel inverter are categorized into two methods: Single-Carrier SPWM (SCSPWM) and Sub-Harmonic SPWM (SHPWM) [9]. SHPWM is an exclusive control strategy for multilevel inverters and has further classifications that are Carrier Disposition PWM methods (Phase Disposition-PDPWM, Phase Opposition Disposition-PODPWM, Alternative Phase Opposition Disposition-APODPWM, and Phase Shifted Carrier PWM method (PSPWM) [9, 10].

Hybrid topologies are the new structures, where the cascaded series inverters have different internal DC bus voltages or use different switching devices and/or are modulated quite differently. In this paper, a novel control algorithm based on Reference Signal Tracking for hybrid cascaded multilevel inverter is presented. The presented method is verified through simulation studies.

2. Topology of the Hybrid Multilevel Inverter

In this paper, a 27 level hybrid multilevel inverter is used [11] as shown in Fig. 1. The inverter consists of three H-bridge cells and the DC link voltage among the stages has the relationship of $1V_{dc}$, $3V_{dc}$ and $9V_{dc}$.

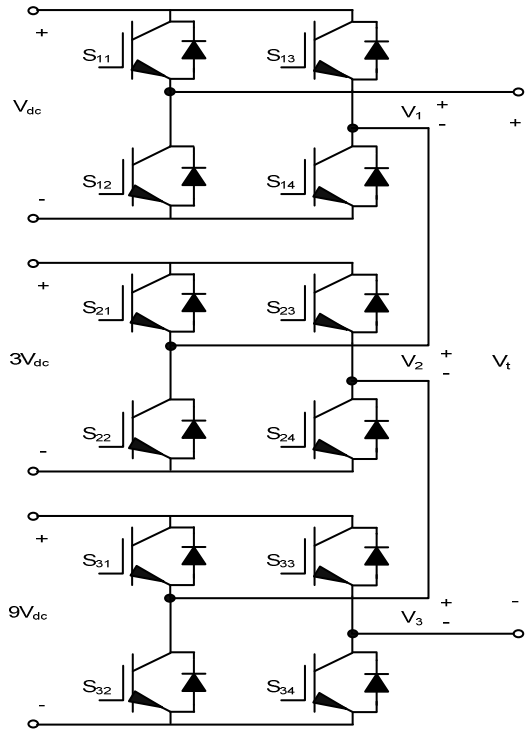

Fig.1. Hybrid multilevel inverter topology

Some of the remarkable features of the proposed multilevel inverter topology are summarized as follows [11].

- This topology has the greatest level number for a given number of stages.
- The inverter switching losses for the stage with the higher DC-link voltage is significantly reduced compared with those for the stage with the lower DC-link voltage.

Fig.2 illustrates the details of switching states for the first h-bridge cell. As shown, three unique output voltages (P, N and Z) are possible. 'P' and 'N' denote the output voltage of the stages of $1V_{dc}$, $3V_{dc}$, and $9V_{dc}$, with positive and negative voltage polarities, respectively. 'Z' indicates that the associated stage is in a freewheeling state, which means that terminals of the output are both connected to the positive terminal of (or negative) DC-link.

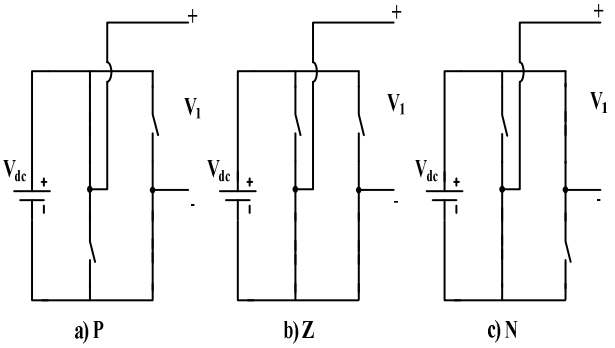

Fig. 2. Switching states for the first h-bridge cell

Table 1 shows the positive and negative voltage levels and corresponding polarity states of hybrid multilevel inverter resulted in the relationship between the output voltage of each cell and output voltage of the inverter as shown in Fig. 1.

Table 1. Voltage levels of hybrid multilevel inverter according to polarities

V_t	V_1	V_2	V_3	V_t	V_1	V_2	V_3
-13 V_{dc}	N	N	N	+13 V_{dc}	P	P	P
-12 V_{dc}	Z	N	N	+12 V_{dc}	Z	P	P
-11 V_{dc}	P	N	N	+11 V_{dc}	N	P	P
-10 V_{dc}	N	Z	N	+10 V_{dc}	P	Z	P
-9 V_{dc}	Z	Z	N	+9 V_{dc}	Z	Z	P
-8 V_{dc}	P	Z	N	+8 V_{dc}	N	Z	P
-7 V_{dc}	N	P	N	+7 V_{dc}	P	N	P
-6 V_{dc}	Z	P	N	+6 V_{dc}	Z	N	P
-5 V_{dc}	P	P	N	+5 V_{dc}	N	N	P
-4 V_{dc}	N	N	Z	+4 V_{dc}	P	P	Z
-3 V_{dc}	Z	N	Z	+3 V_{dc}	Z	P	Z
-2 V_{dc}	P	N	Z	+2 V_{dc}	N	P	Z
-1 V_{dc}	N	Z	Z	+1 V_{dc}	P	Z	Z
0 V_{dc}	Z	Z	Z				

As shown in Table 1, the output waveform has 27 levels; -13 V_{dc}, -12 V_{dc}… -1V_{dc}, 0V_{dc}, +1V_{dc}… +12V_{dc}, +13 V_{dc}. All of the 27 different output levels are obtained using three numbers of stages.

3. New Control Method for Hybrid Multilevel Inverter

In conventionally used PWM methods, the reference signals are always compared with carrier signals. There is no need to compare the carrier signal with reference signal in the new method. The phase angle (θ) of the three phase system is critical for this method. It can be found via two ways: One of them is using the phase locked loop (PLL) and the other is Clarke transformation (α-β) method.

In the new proposed method, PLL is not used. The chancing situations of the reference phase voltage are rapidly perceived by using Clarke transformation shown in Fig 3. The three-phase coordinate system is transformed into the two-phase α-β stationary reference frame by using Equation (1).

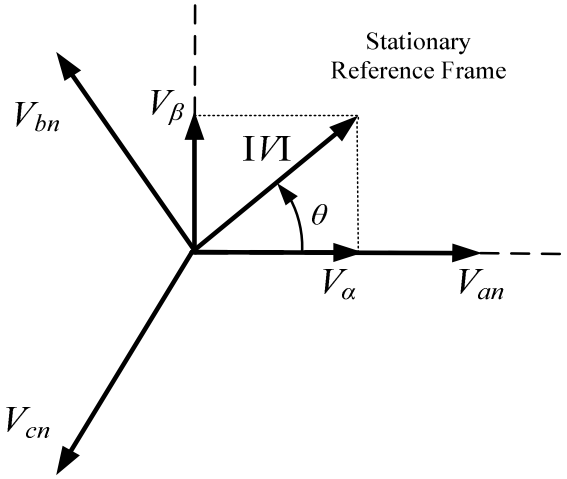

Fig. 3. Vector representation of proposed method

$$\begin{bmatrix} V_\alpha & V_\beta \end{bmatrix}^T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} & V_{bn} & V_{cn} \end{bmatrix} \quad (1)$$

where; V_{an} , V_{bn} , V_{cn} are the reference phase voltages of the three phase system.

After the calculation of the α-β components, the phase angle of the three phase system (also phase A) can be found by using (2).

$$\theta = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \quad (2)$$

Normally the angle θ changes from π/2 to –π/2. But with the use of special arc tangent function (as "atan2" in programming languages), the θ is changes between π and –π. The amplitude for the reference signal is calculated by (3).

$$|V| = \sqrt{V_\alpha^2 + V_\beta^2} \quad (3)$$

The amplitude and angle for the reference signal obtained in reference frame is shown in Fig. 3. So, the reference signal can be obtained by (4) and this signal is used for tracking of phase A.

$$V_{refA} = |V|\cos(\theta) \quad (4)$$

Likewise, (5) can be used for tracking phase B.

$$V_{refB} = |V|\cos(\theta + 2\pi/3) \quad (5)$$

After the determination of the reference signal V_{ref}, the maximum value of reference signal is divided to the levels as stated in previous methods. The amplitude of reference signal is divided by 13 and the one of these levels is called unit amplitude (E_u). The positive cycle of reference signal and some of the unit amplitudes are shown in Fig.4.

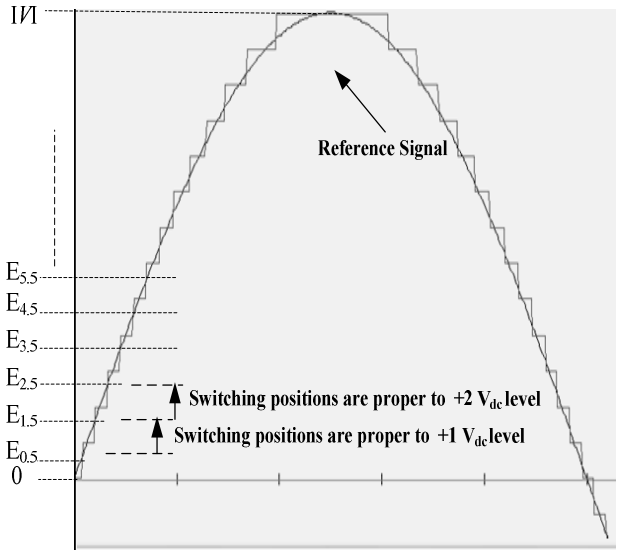

Fig. 4. Positive cycle of reference signal and some levels of output voltage

In the Fig. 4, the voltage levels are shown. Such as, the output is zero before $E_{0.5}$ voltage level. For the second interval, the start point is that the amplitude of the reference is reach $E_{1.5}$ voltage level. At that time, the required switching positions are assigned by the control unit and IGBTs are fired according to switching positions proper to +2 V_{dc} level. That is, the first H-bridge cell is operated at negative state the second h-bridge cell is operated at positive state. The end point of the first interval is that the amplitude of the reference is reach $E_{2.5}$ voltage level. The start and the end points of other levels are defined with same way of the second interval. Thus, the 27 voltage levels are obtained.

4. Simulation Results and Discussions

Fig. 5 shows the output voltages of each cell and reference voltage for the first 14 level (positive levels +1V_{dc}…+12V_{dc}, +13 V_{dc} and zero level). V_1, V_2, V_3 and V_{an} are the waveforms of the first H-bridge cell, the second H-bridge cell, the third H-bridge cell and the reference voltages, respectively.

The value of interval between levels is 0.024 kV. Because the desired amplitude is A_m=311 V, total positive level number n=13 and Am/n is 24 V. The operation principles of proposed method mentioned above may be examined from the Fig. 5. The total output voltage is also shown in Fig.5.

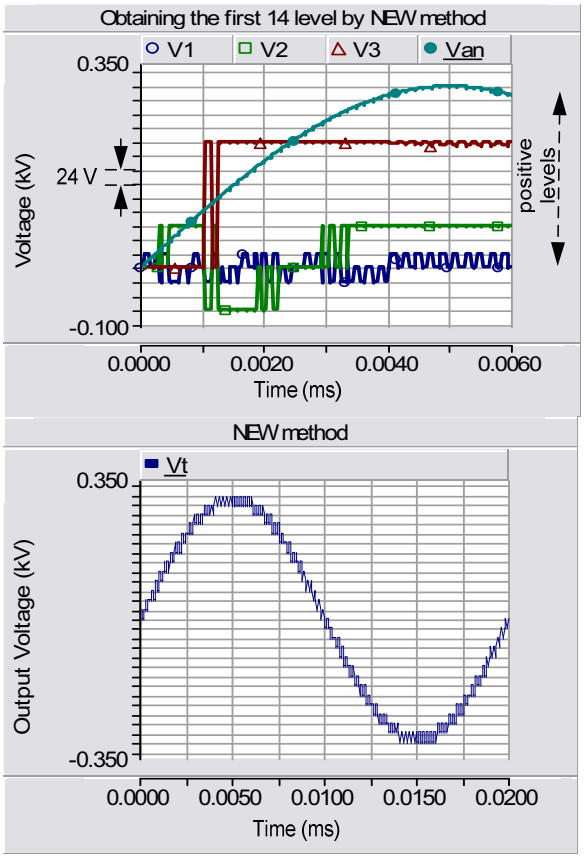

Fig.5. (a) Output voltages of each h-bridge cell and **(b)** Total Output Voltage

The THD values of total output voltage are shown in Table 2 for different modulation indices. As shown from Table 2, THD values are kept below the voltage distortion limits stated in [12] between modulation indices 0.5-1.0 for all methods.

Table 2. THD values of output voltage for modulation indices

Modulation Indices	THD
1.0	1.20
0.75	2.26
0.5	3.93

5. Conclusions

In this paper, a novel proposed method is introduced for hybrid multilevel inverters. The proposed method is based on reference signal tracking. There is no need to compare the carrier signal with reference signal in this new method.

The performance of presented method is verified through simulation studies. According to the results, the proposed method gives acceptable THD and output voltage waveform the control algorithm of the proposed method has also simple

software for control unit, because it does not require PWM comparison.

6. References

[1] N.A. Azli, Y.C. Choong, "Analysis on the Performance of a Three-phase Cascaded H-Bridge Multilevel Inverter", *PECON '06 IEEE International Conference, pp. 405-410, 2006.*

[2] H. Patangia, D. Gregory, "Implementation of a multilevel SPWM inverter for capacitive loads", *Industrial Technology' 06 IEEE International Conference, pp.283-287, 2006.*

[3] Timothy, L.: "The Power Electronics Handbook" (CRC Press Industrial Electronics Series Press, 2002)

[4] K. Yamanaka, , A.M. Hava, , H. Kirino, Y. Tanaka, N. Koga, T. Kume, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector". *IEEE Transactions on Industry Applications, 38, pp.1572-1580, 2002.*

[5] L. Li, "Optimal surplus harmonic distribution in selected harmonic elimination PWM technique for multilevel inverters", *The 25th Annual Conference of Industrial Electronic Society*, *pp.589-594, 1999.*

[6] H. Zhang, "Multilevel Inverter Modulation Schemes to eliminate Common-Mode Voltages", *IEEE Transactions on Industry Applications, pp.1645-1653, 2000.*

[7] Y.M. Chen, C.H. Hsieh, Y.M. Cheng, "Modified SPWM control schemes for three-phase inverters", *IEEE International Conference on Power Electronics and Drive Systems, 2001, 2, pp.651-656*

[8] Z. Salam, J. Aziz, S.S. Ahmed, "Single carrier PWM scheme for cascaded multilevel voltage source inverter", *Power Electronics and Drive Systems PEDS'03, 1, pp.406-410, 2003*

[9] K.D. Babu, "Performance evaluation of three phase cascaded h-bridge multilevel inverter based on multi carrier PWM techniques", *Available at http:// www.ese.iitb.ac.in/ ~icaer2007/ Latest % 20PPT%20File/ 71236TS9%20A. pdf, 2008*

[10] A. Radan, A.H. Shahirinia, M. Falahi, "Evaluation of carrier-based pwm methods for multi-level inverters", *IEEE Industrial Electronics 2007 International Symposium, pp.389-394, 2007*

[11] Y. S. Lai, F.S. Shyu, " 'Topology for hybrid multilevel inverter", *IEE Proceedings on Electric Power Applications, 149, pp.449- 458, 2002.*

[12] IEEE, "Recommended practices and requirements for harmonic control in electrical power systems", *(IEEE Standard), pp.519-1992, 1993.*