A New Rom-Less Pulse Shaper for 2.4 GHz ZigBee Application

Ali Sahafi, Jafar Sobhi, Mahdi Sahafi, and Omid Farhanieh

Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran

Ali.Sahafi88@ms.tabrizu.ac.ir, sobhi@tabrizu.ac.ir
ms.mahdi@gmail.com, o.farhanieh@gmail.com

Abstract

This paper presents a special automatic pulse shaper for 2.4 GHz ZigBee transmitters. To implement half sine shape needed for OQPSK pulse shaping used in ZigBee, a circuit was designed that consists of a clock generator, a customized current-steering digital to analog converter (DAC) and a low-pass filter (LPF). Every point of a sine shape is produced by adding or subtracting current sources. Clock generator produces required logical bits for the DAC. A customized fully differential quadrature current mode DAC produces 4 half sine outputs (I+, I- , Q+, Q-). This topology does not need any ROM or counter and is independent from digital section and results in reduced power consumption and die size. Furthermore, eliminating the binary DAC eliminates glitch effect too; so linearity of total system is improved. Simulation results show -36db THD at output signal by using 5-point for every quadrant. All of circuits are designed based on 0.18µm TSMC CMOS technology with a single 1.8 volt power supply.

Keywords: DAC, Signal shaper, OQPSK, ZigBee

1. Introduction

Increasing demands in wireless communication make this field of technology attractive for institutes to produce new protocols. The recent developments and advanced scaling in CMOS technology have made it more attractive to produce a single chip, multipurpose and low power products.

Present transmitter sections for telecom standards consist of the cascade of a DAC, the mixers and power amplifiers (PA) (Fig. 1). In this structure, DAC works as a digital filter to limit data bandwidth before mixing with local oscillator (LO) in mixer. In OQPSK, digital ONE and ZERO is replaced by an up and down half sine waveform (Fig. 2). Majority of present modulators [1 - 4], employ a binary DAC in the pulse shaping path. Fig. 3 describes a conventional pulse shaper that uses DDS (Direct Digital Synthesis) structure that has counter, ROM, binary DAC and a low-pass filter [5]. The counter produces streams of numbers and ROM sends predefined quantities to DAC. Generated signal is filtered by a low pass filter to gain a smooth signal at the input of mixers. This topology has some disadvantages:

- Existence of ROM is essential to keep predefined magnitudes but this block occupies large area for high resolution DACs and consumes a large portion of power.

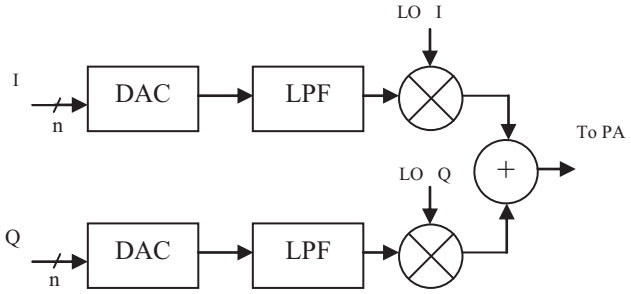

Fig. 1. Transmitter

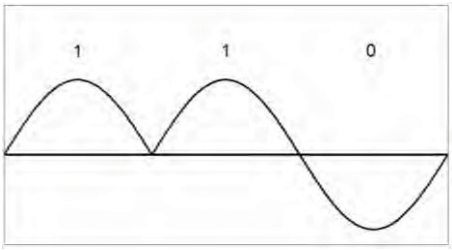

Fig. 2. Output of ideal half sine pulse shaper

- Mismatches in the binary DAC, produces glitches at the output of the DAC, which make the system to put a high order low-pass filter to keep the smoothness of signal.
- Because of limited numbers of quantities for binary DAC, it's necessary to use high resolution DAC to have a proper approximation of the shape.

In this paper a new complete pulse shaping architecture has been introduced to solve the problems associated with the conventional ones. The performance of the pulse shaper has been enhanced by combining the digital section and designing a new modified DAC that made it suitable for low-cost and low-power wireless solutions. All of the circuits have been designed and implemented in 0.18µm CMOS TSMC technology.

The rest of paper is organized as follows: In section II, the proposed architecture will be described and section III describes each block of the proposed circuit. At section IV, the simulation results which prove our theoretical work are presented. Section V concludes this paper.

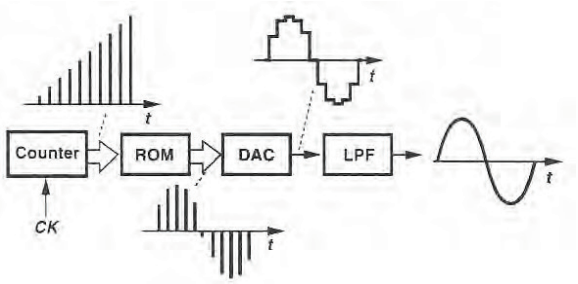

Fig. 3. Simple pulse shaper with a binary DAC

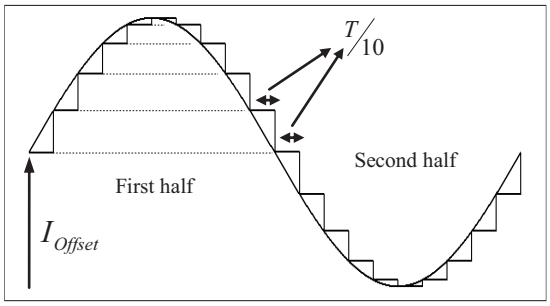

Fig. 5. Approximation of a sine shape

2. Main Architecture for Transmitter Pulse Shaper

Fig. 4 illustrates a simple block diagram of designed pulse shaper. As it is apparent this block has 3 inputs; clock pulse, I channel's data and Q channel's data, and it doesn't have any other input, so all of the required signals are generated inside the pulse shaper. Consider the sine waveform shown in Fig. 5 is to be generated. In proposed topology, we have assigned a current for every point and produce these points by adding or subtracting a current source. With two sets of current sources and switches, we are able to approximate this waveform. If we approximate a half sine shape by 10 samples, with amplitude of 20, the value of samples will be: {0, 6, 12, 16, 19, 20, 19, 16, 12 and 6}.

The arrangement of current sources and switches has been shown in Fig. 6. At the beginning, all $\{b_i\}$ switches are open and control signal $\overline{Up}(Down)$ is low, so according to Fig. 7, all $\{c_i\}$ switches are closed and total output current produces $\{I_{offset}\}$ ($\{I_{offset}=(6+6+4+3+1)*I_{ref}\}$). $\{I_{ref}\}$ is the value of a reference current which is multiplied by the required factor using current mirrors (Fig. 8). To generate next point, a current source of $\{6*I_{ref}\}$ is added to the output using switch $\{b_0\}$ and the current of $\{I_{offset}+ 6*I_{ref}\}$ is produced. For the second point, another current source of $\{6*I_{ref}\}$ is added to the output by switch $\{b_1\}$ and the current of $\{I_{offset}+ 12*I_{ref}\}$ is produced. For the third point, a current source of $\{4*I_{ref}\}$ is added to the total current by $\{b_2\}$ and the current of $\{I_{offset}+ 16*I_{ref}\}$ is generated. To continue, other $\{b_i\}$ switches are closed one by one and first quadrant is made point by point. Now for the second quadrant, the same switches are opened in reverse order and current sources are subtracted from the output current.

For the second half, the control signal $\overline{Up}(Down)$ is high. As it can be seen from Fig. 7, the state of $\{c_i\}$ switches will be the complement of $\{b_i\}$ switches. Now they start to open in the same order as first quadrant but this time the value of current source will be subtracted from the output current. For example in the first point of second half of sine shape, turning off $\{c_0\}$ switch subtracts $\{6*I_{ref}\}$ current from output and $\{I_{offset} - 6*I_{ref}\}$ is produced. Finally, they start to close one by one in reverse order and add to the output to make the last quadrant. This process will be repeated to generate a periodic (up/down) half sine wave. As this process continues periodically, a clock generator can produce clocks automatically for DAC. At the end of the block a second-order RC low-pass filter, smoothes the output signals.

As described above, we have used a couple of {6, 6, 4, 3, 1} current sources. So the total number of transistors is 40 transistors same to reference transistor. If we want to implement this resolution by a binary DAC we needed a binary number of 20. This number is produced by a 4 bit binary DAC. To distinguish second half, another bit is required. So in binary DAC we have these numbers: {32, 16, 8, 4, 2, and 1}. Total number of transistors in binary DAC is 63. This shows reduction in quantity of transistors in presented architecture (63 transistors to 40 transistors).

In binary DAC, sometimes with only one LSB change in code all switches have to be turned on or off simultaneously (e.g. 0111⟶ 1000). Because of the mismatch in switches, it is

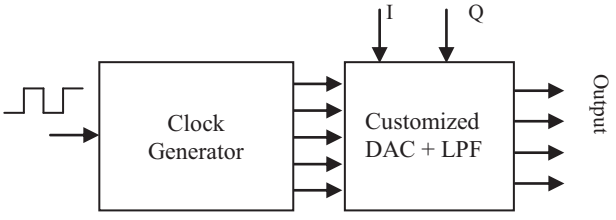

Fig. 4. Main diagram of pulse shaper

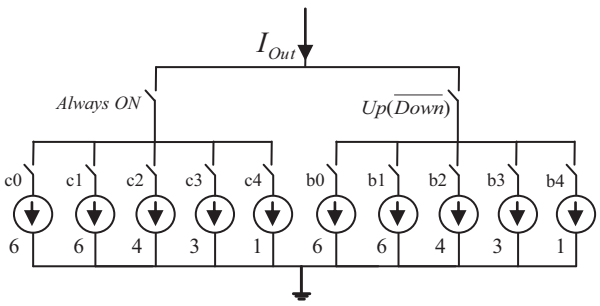

Fig 6. Customized DAC current sources

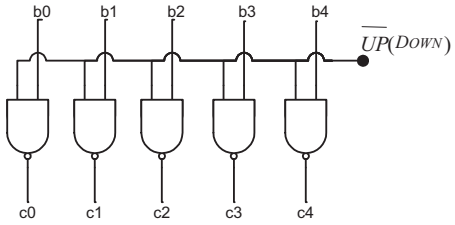

Fig. 7. Nand Block

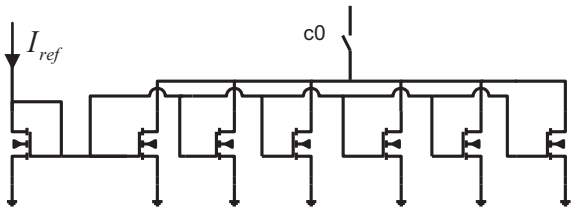

Fig. 8. Current mirror used to generate 6 times of reference current.

possible to have wrong output 1111 for a short time that produces glitch at output and results undesirable harmonics. As described earlier, in proposed architecture to generate each point of the waveform only a single current source is turned on or off and this eliminates the glitch problem associated with binary DAC's used in pervious works. This process is similar to Gray code that has been changed to use for a special purpose.

This topology eliminates counter and ROM (The function of ROM has been placed in the quantity of transistors); so digital block that produces clock is simpler and power consumption is repressed and die size is reduced.

One of the important characteristic of this topology is the ability to implement fractional values. For example if we want to produce a $\{4.4*I_{ref}\}$, we can use 3 transistors same to reference transistor and an additional transistor that its width is equal to 1.4 times of reference transistor. If we want to have this magnitude in binary DAC, we need a high-resolution DAC to have a good approximation of this magnitude.

3. Building Blocks

3.1. Customized DAC and LPF

As mentioned before, customized DAC has been composed of $\{I_{ref}\}$ and current mirrors with different numbers of transistors to obtain required currents.

Fig. 6 depicts the arrangement of current sources. In up-half sine shape, *Up* (that is equal to input bit in I or Q channel) is binary 1 so $\{c_0\text{-}c_4\}$ switches are turned on by NAND gates shown in Fig. 7. These current sources generate $\{I_{offset}\}$. Switches $\{b_0\text{-}b_4\}$ are driven by wave forms illustrated in Fig. 9. Currents related to these switches with $\{I_{offset}\}$ produce required output currents.

In down-half sine shape, *Up* is 0 and *Down* is 1. So all of the current sources related to $\{b_0\text{-}b_4\}$ switches are turned 0ff. Output of NAND gates send complementary of clocks showed in Fig. 9 to $\{c_0\text{-}c_4\}$ switches. This sequence of current switching generates needed currents for down-half sine. The *Always ON* switch has been placed to keep balance of two current blocks.

Finally, output currents drive 10KΩ resistor and produce output voltage.

A second-order RC low-pass filter has been added to smooth the sine shape. Because of elimination of glitch effect and choosing proper sizes for current sources, second order low-pass filter is adequate to have an appropriate approximation of sine wave.

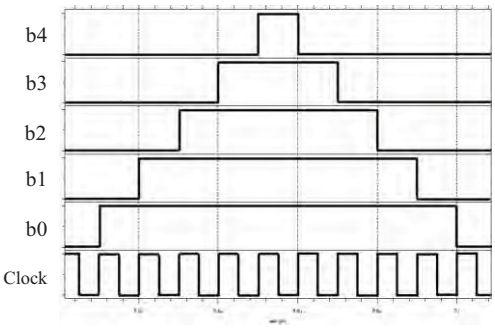

Fig. 9. Output signals of clock generator

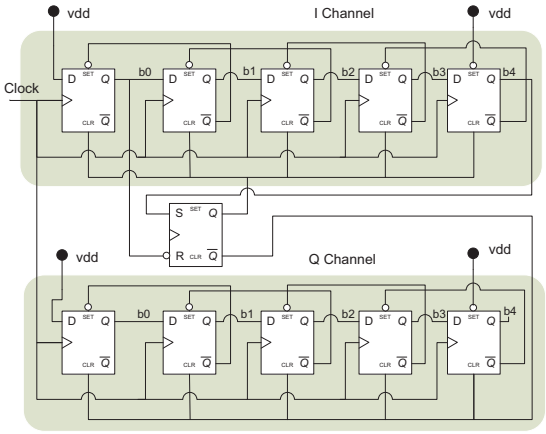

Fig. 10. Clock generator

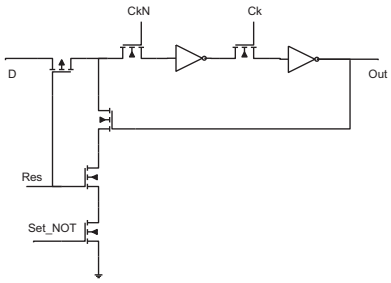

Fig. 11. Specialized DFF

3.2. Clock generator

The clocks shown in Fig. 9 are necessary for generating half sine shape, independent from value of input data. Fig. 10 shows inner parts of clock generator. Clock generator is a bit shifter that shifts ONE from left to right at rising quadrant and ZERO from right to left at falling quadrant. The 5-point clock generator has 5 specialized D Flip-Flop (DFF) for every channel and 1 Reset-Set Flip-Flop (RSFF). Output of RSFF changes quadrant (falling or rising) for I channel and sends its complement to Q channel. When I channel's DAC is in first quadrant, DAC of Q channel works in second quadrant. By this method 90 deg. phase difference between two channels is produced.

Fig. 11 shows internal elements of specialized DFF. When CLR, SET_NOT and Q of DFF are logically one, output of DFF is reset at next clock.

The required signals are obtained from the outputs of DFFs.

4. Simulation Results

The proposed pulse shaper has been designed to be used in 2.4 GHz ZigBee transmitter with the system clock of 20 MHz. Period of one bit is 1µs. By using 5-point DAC for every quadrant, a 10 MHz clock is required that can be generated by a divid-by-2 from system clock.

All of the circuits are designed and tested by Cadence spectre in 0.18µm TSMC CMOS technology.

Fig. 12 shows output of pulse shaper with random inputs. Total power consumption of fully differential quadrature pulse shaper is 420µW. Fig. 13 shows FFT diagram for a sine wave produced by pulse shaper. THD of a complete sine is -36db.

5. Conclusion

A new half sine pulse shaper for OQPSK modulator has been proposed. Two set of switches and current source are used to approximate the waveform with 20 points in a cycle. To generate each point, a single current source is turned on or off which eliminates the glitch problem associated with binary DAC's used in previous works. Also, currents with fractional values could be generated with sizing of transistors. Elimination of ROM and counter required in conventional methods, results in reduced power consumption and silicon area. All of the circuits are designed and tested by Cadence Spectre in 0.18µm TSMC CMOS technology. Simulation results show -36 dB THD at output signal by using 5-point for every quadrant.

6. References

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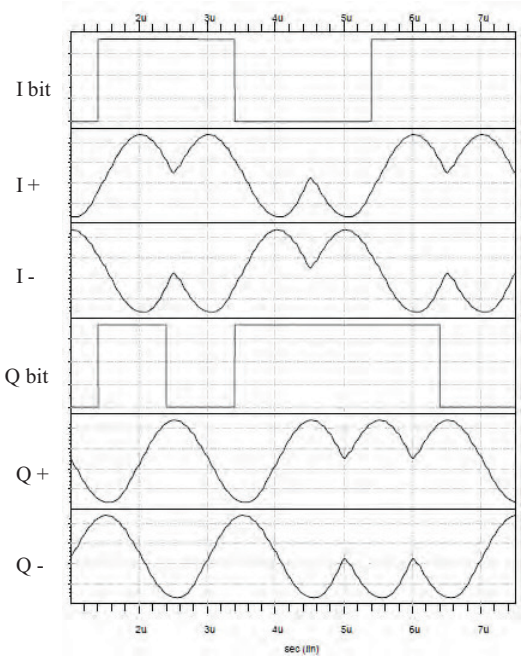

Fig. 12. Output signals of differential DAC

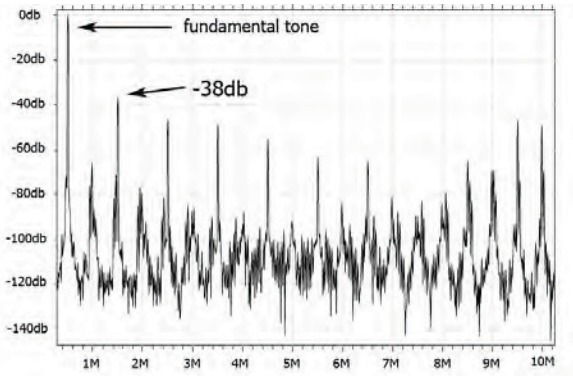

Fig. 13. FFT diagram of sine shape produced by signal shaper