A 10-BIT 1.2-GS/s NYQUIST CURRENT-STEERING CMOS D/A CONVERTER USING A NOVEL 3-D DECODER

Paymun Aliparast
e-mail: peyman.aliparast@elec.tct.ac.ir

Nasser Nasirzadeh
e-mail: nnasirzadeh@elec.tct.ac.ir

Tabriz College of Technology, Institute of Electrical & Electronics Engineering, Tabriz, IRAN

Key words: Current-steering DAC, Integrated Circuit, Thermometer decoder

ABSTRACT

A 10-bit 1.2-GSample/s current-steering DAC is presented. 90% segmentation has been used to get the best DNL and reduce glitch energy. A novel method in designing thermometer decoder reduces the area and power consumption. The chip has been processed in a standard 0.35µm CMOS technology. Active area of chip is 1.97 mm^2**.**

I. INTRODUCTION

Currents-steering DACs are based on a array of matched current sources which are unity decoded or binary weighted [7]. Figure 1 shows a typical block diagram of an n-bit current-steering DAC. Input word is segmented between b less significant bits that switch a binary weighted array, and m = n-b most significant bits that control switching of a unary current source array. The m input bits are thermometer decoded to switch individually each of the 2^{m-1} unary sources [13-15]. A dummy decoder is placed in the binary weighted input path to equalize the delay. A latch is placed just before the switch transistors of each current source to minimize any timing error [5].

The performance of the DAC is specified through static parameters: Integral Non-Linearity (INL), Differential Non-Linearity (DNL), and parametric yield; and dynamic parameters: glitch energy, settling time and SFDR [2]. Static performance is mainly dominated by systematic and random errors. Systematic errors caused by process, temperature and electrical slow variation gradients are almost cancelled by proper layout techniques [3]. Random errors are determined solely by mismatch due to fast variation gradients. The design of current-steering DAC starts with an architectural selection to find the optimum segmentation ratio (*m* over *n*) that minimizes the overall digital and analog area [4 - 6]. The INL is independent of the segmentation ratio and depends only on the mismatch if the output impedance is made large enough [7]. The DNL specification depends on the segmentation ratio but it is always satisfied provided that the INL is below 0.5 LSB for reasonable segmentation ratios. The glitch energy is determined by the number of binary bits *b*, being the optimum architecture in this sense a totally unary DAC. However this is unfeasible in practice due to the large area and delay that the thermometer decoder would exhibit. The minimization of the glitch energy is then done in circuit level design and layout of the switch & latch array and current source cell [1].

II. BINARY WEIGHTED ARCHITECTURE VS. UNARY DECODED ARCHITECTURE

Current-steering architectures differ from current dividing architectures in that they replicate a reference current source rather than divide it. As shown in Figure 2, the reference source is simply replicated in each branch of the DAC, and each branch current is switched on or off based on the input code. For the binary version, the reference current is multiplied by a power of two, creating larger currents to represent higher magnitude digital signals. In the unit-element version, each current branch produces an equal amount of current, and thus 2N current source elements are needed. In overall for binary weighted architecture versus unary decoded architecture we can summarize:

Thermometer:

Positive

- Low glitch energy
- Monotonicity
- Small DNL errors

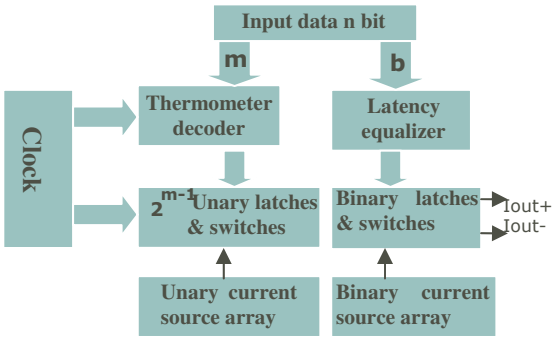
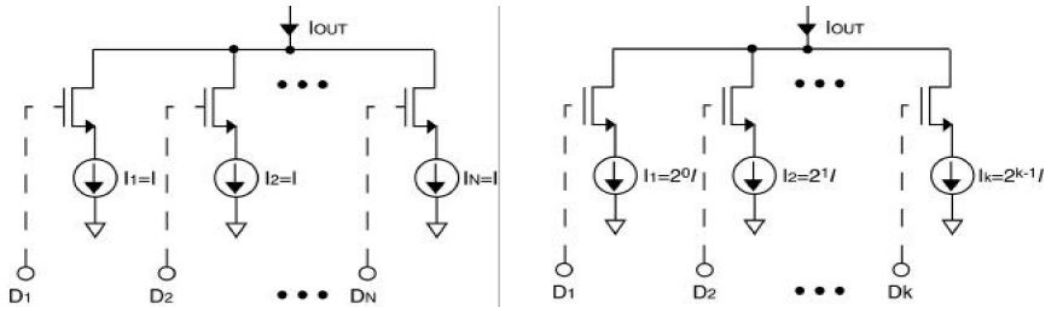


Figure 1. Current-steering DAC architecture.



(a) (b)

Figure 2. **(a)** Unit-element current-steering DAC **(b)** binary current-steering DAC.

Negative
- Digital decoding with more area and power consumption
- Increased number of control signals

Binary:

Positive
- Low digital power consumption
- Small number of control signals

Negative
- Monotonicity not guaranteed
- Larger DNL errors
- Large glitch energy

Usually, to leverage the clear advantages of the thermometer-coded architecture and to obtain a small area simultaneously, a compromise is found by using segmentation [5]. The DAC is divided into two sub-DACs, one for the MSBs and one for the LSBs. Thermometer coding is used in the MSB where the accuracy is needed most. Because of the reduced number of bits in this section, the size is considerably smaller than a true thermometer coded design. The LSB section can either be done using the binary-weighted or the thermometer-coded approach. We will refer to a fully binary-weighted design as 0% segmented, whereas a fully thermometer-coded design is referred to as 100% segmented. Thus we have used 90% segmentation to achieve the best performance in high-speed design and tried to improve digital area and power consumption with improved digital section of the DAC.

III. IMPROVED THERMOMETER DECODER ARCHITECTURE

Figure 3 shows a block diagram of a conventional row and column decoded 10-bit current-steering DAC. In this block diagram, the lowest significant bit is applied to a dummy decoder [11]. This decoder creates a delay proportional to the Binary to Thermometer decoder and causes the signal to arrive at the switches synchronously. The five LSB bits are column decoded and the four MSB bits are row decoded. Column decoder is a 5-input 31-output Binary to Thermometer Decoder and row decoder is a 4- input 15-output Binary to Thermometer Decoder. the

But if we think about Binary to Thermometer Decoder structure we understand that with β-bit increase of the input of decoder, area, complexity, number of control signal and power consumption of decoder increase with 2^{β}. In fact power and area are doubled with only one bit increase in the input of decoder and we can write:

$$\mathcal{P}(\text{4to15 BTD}) = 2*\mathcal{P}(\text{3to7 BTD})$$
$$\mathcal{A}(\text{4to15 BTD}) = 2*\mathcal{A}(\text{3to7 BTD})$$

Thus:

$$\mathcal{P}(\text{5to31 BTD}) = 4*\mathcal{P}(\text{3to7 BTD})$$
$$\mathcal{A}(\text{5to31 BTD}) = 4*\mathcal{A}(\text{3to7 BTD})$$

where BTD is Binary to Thermometer Decoder, $\mathcal{P}$ is the power consumption of the decoder and $\mathcal{A}$ is active area that the decoder uses. Now consider Figure 4 that shows a 3D D/A converter. In this block diagram three BTD have been used. Three bits for height, three bits for row and three bits for column and every cell is selected with 3 parameters (R, C and H). In fact we have only used three (3to7 BTD) instead of two (5to31 BTD) and (4to15 BTD) thus power consumption and area of the circuit have been improved two times because :

$$\begin{array}{rl} & \mathcal{P}(\text{4to15 BTD}) = 2*\mathcal{P}(\text{3to7 BTD}) \\ + & \mathcal{P}(\text{5to31 BTD}) = 4*\mathcal{P}(\text{3to7 BTD}) \\ \hline \end{array}$$

$$\mathcal{P}(\text{4to15 BTD}) + \mathcal{P}(\text{5to31 BTD}) = 6*\mathcal{P}(\text{3to7 BTD})$$

And for area we have:

$$\begin{array}{rl} & \mathcal{A}(\text{4to15 BTD}) = 2*\mathcal{A}(\text{3to7 BTD}) \\ + & \mathcal{A}(\text{5to31 BTD}) = 4*\mathcal{A}(\text{3to7 BTD}) \\ \hline \end{array}$$

$$\mathcal{A}(\text{4to15 BTD}) + \mathcal{A}(\text{5to31 BTD}) = 6*\mathcal{A}(\text{3to7BTD})$$

In this structure 3 LSB bits are column decoded, 3 middle bits are row decoded and 3 MSB bits are height decoded. On the other hand we have only used 21 control signals instead of 46 control signals thus the number of control

signals has been decreased by 55 percent so we can achieve the best speed and performance.

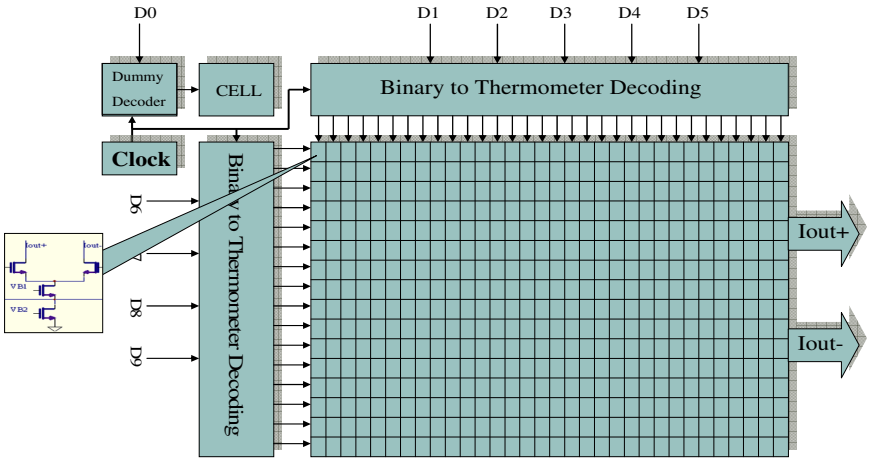


Figure 3. Block diagram of a conventional row and column decoded 10-bit current-steering DAC.

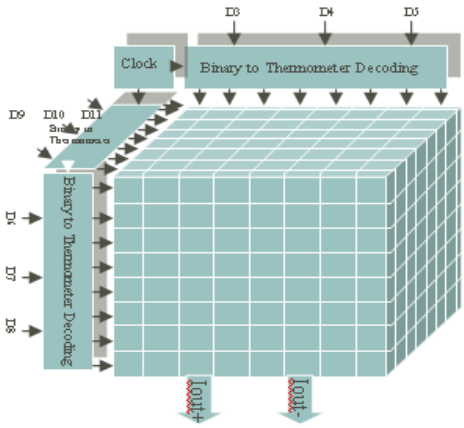


Figure 4. Block diagram of a novel method row and column and height decoded 9-bit 3D DAC.

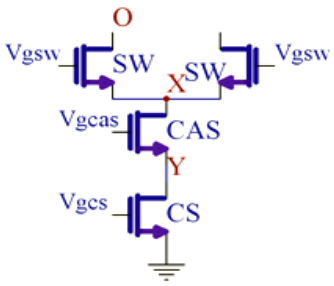


Figure 5. Current source cell topology.

IV. THE CURRENT CELL, LATCH AND DRIVER

DAC performance is specified both through static parameters, namely Integral Non-Linearity (INL), Differential Non-Linearity (DNL), and parametric yield, as well as dynamic parameters, namely glitch energy, settling time and spurious-free dynamic range (SFDR) [2]. Static and dynamic performance of current-steering DACs is mostly determined by the current sources accuracy, finite output impedance, and switching time. Figure 5 shows a current source (CS) transistor, an additional cascode transistor (CAS) that increases the output impedance and two complementary switch (SW) transistors. Since two D/A converters processed in the same technology do not necessarily have the same specifications due to technological variations, it is of the utmost importance to know the relationship that exists between the specifications of the circuit and the matching properties of used technology. For a current-steering D/A converter, the INL is mainly determined by the matching behavior of the current sources. A parameter that is well suited for expressing this technology versus DAC specification relation is the INL yield [15]. This INL yield is defined as the ratio of the number of D/A converters with an INL smaller than LSB to the total number of tested D/A converters. As defined by Pelgrom, mismatch "is the process that causes time-independent random variations in physical quantities of identically designed devices" [9]. Pelgrom's paper has become the de facto standard for analysis of transistor matching, and thus his formula for the standard deviation of saturation current for two identically sized devices has been used for the design. This formula is:

$$\frac{\sigma^2(I)}{I^2} = \frac{4\sigma^2(V_T)}{(V_{GS} - V_T)^2} + \frac{\sigma^2(\beta)}{\beta^2} \qquad \textbf{(1)}$$

where

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} + S_{VT}^2 D^2$$

and

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \cdot$$

Most of these variables are process-dependent constants. Using these results, an equation for the minimum size device that still provides a reasonable current standard deviation can be determined [10]:

$$\frac{\sigma I^2}{I^2} = \frac{1}{2WL_{cs\ \min}}\left(A_\beta^2 + \frac{4A_{VT}^2}{\Delta V^2}\right) \qquad \textbf{(2)}$$

where A_β, A_{VT}, V_{GS} and V_T are process parameters, while I is the current generated by a given source and σI is *the* relative standard deviation of one current source. The same aspect ratio can be obtained for different areas $W \times L$, except for the CS transistor, because the usual INL-mismatch specification eliminates one degree of freedom. The relative standard deviation of a unit current source $\sigma I/I$ has to be small enough to fulfill the INL < 0.5 LSB specification given a parametric *yield* [11]:

$$\frac{\sigma I^2}{I^2} \le \frac{INL_{\ upper\ -bound}}{inv\ \_\ normal\ \ (0.5+\frac{yield}{2}).\sqrt{2^{N-1}}} \qquad \textbf{(3)}$$

where **inv_normal** is the inverse cumulative normal distribution.

The CS transistor size is found by:

$$W^2 = \frac{I}{\mu_n C_{ox}\left(\frac{\sigma I}{I}\right)^2}\left[\frac{A_\beta^2}{\Delta V^2} + \frac{4A_{VT}^2}{\Delta V^4}\right] \qquad \textbf{(4)}$$

$$L^2 = \frac{\mu_n C_{ox}}{4I.\left(\frac{\sigma I}{I}\right)^2}\left[A_\beta^2.\Delta V^2 + 4A_{VT}^2\right] \qquad \textbf{(5)}$$

where $\mu_n C_{ox}$ is the MOS transistor gain factor, V_T is the threshold voltage, and A_{VT} and A_β are their technology matching parameters, respectively and $\Delta V = (V_{GS} - V_T)$. But if we use (4) and (5) for current cell sizing we will face a problem because we are trying to design very high speed cascode but if we use this equation, W_{CS} will be different from W_{CAS} and we must use contact in the node Y in Figure 5 and this decreases the speed of cascode but we can improve this problem with fixed W_{CS} in the same size with W_{CAS} and change L_{CS} and *I*. Thus we don't use this equation and use only mismatch equation (2) to reach a minimum sizing of current cell.

The small-signal output impedance for the current source topology of Figure 5 is given by:

$$R_{out} \approx gm_{SW}.gm_{CAS}.r_{dsSW}.r_{dsCAS}.r_{dsCS}$$

The optimum SW and CAS gate bias voltages concerning the output impedance are found by differentiating R_{out} with respect to V_{gsw} and V_{scas}. For the SW and CAS gate bias voltages that maximize output impedance are found as:

$$V_{gCAS} = V_T + \frac{1}{3}(V_{o\min} + 2\Delta V_{CS} + 2\Delta V_{CAS} - \Delta V_{SW})$$

$$V_{gSW} = V_T + \frac{1}{3}(2V_{o\min} + \Delta V_{CS} + \Delta V_{CAS} + \Delta V_{SW})$$

A driver circuit with a reduced swing placed between the latch and the switch reduces the clock feedthrough to the output node as well [12], [16]. The latch circuit complementary output levels and crossing point are designed to minimize glitches [1]. The circuit for control waveform generation is shown in Figure 6. The unsynchronized digital input is fed in from the left and the cascode current source and the current switch are shown on the right. The capacitive coupling to the analog output is minimized by limiting the amplitude of the control signals just high enough to switch the tail current completely to the desired output branch of the differential pair. In addition the switch transistors are kept relatively small in order to avoid large parasitic capacitances.
Clock distribution for 1.2GHz is very difficult and getting data in this speed is very hard thus we have used 2 channels for digital section. Every channel works at 600MHz and then results of two channels are combined to get 1.2GHz. Figure 7 shows the structure used for digital section of the DAC. Channel 1 samples input data with clock and channel 2 samples input data with clock-not. In fact in one period of clock we take 2 samples of input code and in the output it seems that the circuit works at 1.2 GHz.

V. LAYOUT AND SIMULATION RESULTS

Figure 8 shows the complete layout of the DAC, latches and switches which are grouped in a separated array placed between the decoders and the current source arrays to isolate these noisy digital circuits from the sensitive analog circuits that generate the current. A guard ring has been used to separate analog section from digital section. Current cells are divided into two current sources and a common-centroid layout has been used to reduce the effects of gradients.

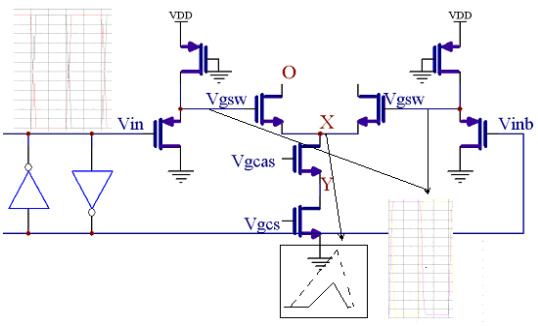


Figure 6. Non symmetrical crossing point reduces current source drain spike and clock feedthrough.

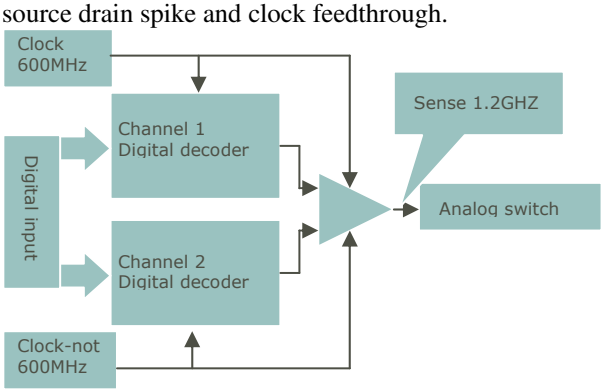


Figure 7. Using two 600MHz digital channels to achieve 1.2Gsample/s.

Layout of the decoder circuit has been drawn manually and pipelining used to reach the maximum speed and improve the parasitic capacitance and sizing of transistors with simulation. Measurements have been performed on a differential 50Ω load. The internal node interconnection capacitance has been estimated to be 400fF, and the output capacitance 1pF. The analog voltage supply is 3.3V while the digital part of the chip operates at only 2.4V. Total power consumption in the nyquist rate measurement is 149mW. The technology used is a 0.35µm, single-poly four-metal, 3.3V, standard digital CMOS process. The active area of the DAC, as shown in Figure 8, is 1850µm*1070µm. SFDR is better than 57dB in nyquist rate. Figure 9 shows differential output spectrum where DAC worked with 1.2 GSample/s speed and input code near to nyquist rate (594MHz).

REFERENCES

1. J. Bastos, M. Steyaert, W. Sansen," A high yield 12-bit 250-MS/s CMOS D/A converter", Proc. IEEE 1996 Custom Integrated Circuits Conf. (CICC), May 1996, pp. 20.6.1-20.6.4
2. P. Hendriks, "Specifying Communication DACs", IEEE Spectrum, July 1997, pp. 58-69.
3. Y. Cong, R. L. Geiger, "Switching Sequence Optimization for Gradient Error Compensation in Thermometer-Decoded DAC Arrays", IEEE Tr. on Circuits and Systems-II, Vol. 47, No. 7, 2000, pp. 585-595.
4. J. Vandenbussche et al, "Systematic Design of High-Accuracy Current-Steering D/A Converter Macrocell for Integrated VLSI Systems", IEEE Tr. on Circuits and Systems-II, Vol. 48, No. 3, 2001, pp. 300-309.
5. C. H. Lin, K. Bult, "A 10-bit, 500-MS/s CMOS DAC in 0.6 mm2", IEEE J. of Solid-State Circuits, Vol. 33, No. 2, 1998, pp. 1948-1958.
6. J. L. Gonzalez, E. Alarcon, "Clock-Jitter Induced Distortion in High-Speed CMOS Switched-Current Segmented Digital-to-Analog Converters", Proc. of IEEE Intl. Symposium on Circuits and Systems (ISCAS'01), May 2001, pp. 1512-1515.

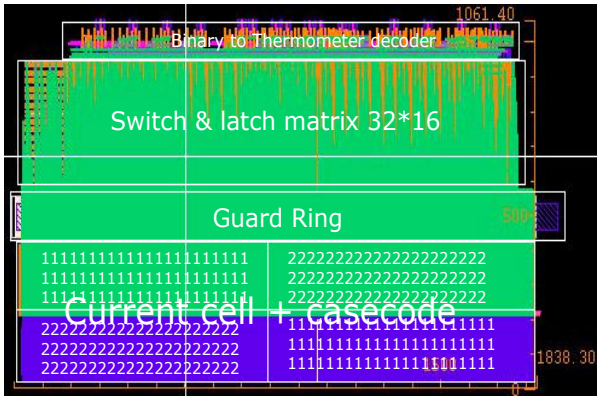


Figure 8. Layout of designed 10-bit DAC.

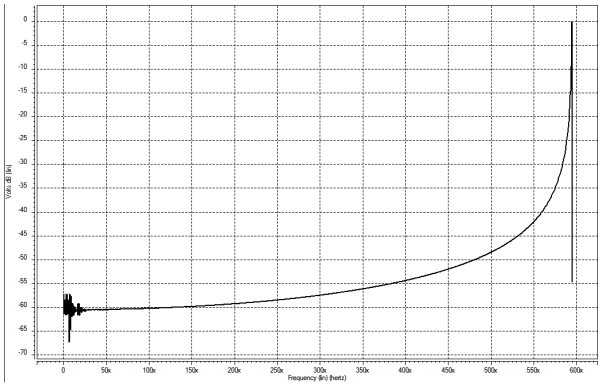


Figure 9. Sinewave spectrum for Fs = 1.2 GSample/s Fsig = 594 MHz.

7. B. Razavi, "Principles of Data Conversion Systems", IEEE Press, New Jersey, 1995.
8. Chi-Hung Lin, Klaas Bult, "A 10-bit 500-MS/s CMOS DAC in 0.6 mm2", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998.
9. M. J. M. Pelgrom, A. C. J. Duinmaijer, P.G. Welbers, "Matching properties of MOS transistors", IEEE Journal of Solid-State Circuits, Vol.24, No. 5, October 1989.
10. J. Bastos, A. Marques, M. Steyaert, W. Sansen, "A 12-bit Intrinsic Accuracy High-Speed CMOS DAC", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998.
11. A. V. Bosch, M. A. F. Borremans, M. S. J. Steyaert, W. Sansen, "A 10-bit 1-GS/s Nyquist Current-Steering CMOS D/A Converter", IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, 2001, pp. 315-324.
12. H. Khono et al, "A 350-MS/s 3.3-v 8-bit CMOS D/A Converter Using a Delayed Driving Scheme", Proc. of CICC, 1995.

13. L. Sumanen et al, “A 10-bit High-Speed Low-Power CMOS D/A Converter in 0.2 mm2”, Proc. of ICECS, 1998.
14. Y. Nakamura et al, “A 10-b 70-MS/s CMOS D/A converter”, JSSC, Vol. 26, No. 4, 1991.
15. M. Albiol, J. L. Gonzalez, E. Alarcon, “Mismatch and Dynamic modelling of Current Sources in Current-Steering CMOS D/A Converters: An Extended Design Procedure”, IEEE Transaction on Circuits and Systems –I: Regular Papers, Vol. 51, No. 1, January 2004.
16. L. Luh, Y. Choma, and J. Draper, “A High-Speed Fully Differential Current Switch”, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 47, No.4, April 2000.