AN APPLICATION OF WEIBULL DISTRIBUTION TO HOT CARRIER DEGRADATION IN THRESHOLD VOLTAGE AND DRAIN CURRENT OF MOS TRANSISTORS

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ABSTRACT

The importance of long term reliability in MOS VLSI circuits is becoming an important subject because of the increasing densities of VLSI chips. Hot carrier effects cause noncatastrophic failures which develop gradually over time and change the circuit performance.

The Weibull distribution is often used to describe the life times of parts and widely applied to characterize the breakdown statistics of solid dielectric samples.

In this study the degradation in the threshold voltage and the drain current is observed by operating the MOSFET under voltage stress conditions. The linear regression method is used to estimate the Weibull parameters and the correlation coefficient is used to confirm the results. The observed and the estimated values of the degradation are compared with each other.

I. INTRODUCTION

The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time. Because of the increasing densities of VLSI chips, the importance of long term reliability in MOS VLSI circuits is becoming an important issue. The reliability on the circuit level is directly related to the observed physical failure mechanisms. Some of physical degradation mechanisms such as electromigration and electrostatic discharge manifest themselves by abrupt and catastrophic changes in the device characteristics and the circuit operation. Other mechanisms such as hot carrier effects cause noncatastrophic failures which develop gradually over time and change the circuit performance. For most failure mechanisms concerning

MOS VLSI circuits, the system can not be repaired and returned to normal use once a failure occurs.

In most systems the failure pattern changes over time. Depending on the causes of failure, the failure rate can be classified as decreasing constant or increasing with time. Decreasing failure rates are observed when a certain percentage of chips under consideration contain weaknessses introduced by undetected manufacturing defects which cause a number of early failures and eliminate the weak chips. Screening of early failures will substantially increase the overall reliability of the system. A constant failure rate is typical for failures caused by accidental over stress or over loads, occuring randomly over the useful life time of the system [1-12].

A number of different techniques can be used to reveal the early failures. These techniques usually attempt to provoke the mechanisms that cause early failures without excessively aging the remaining hardware. Typical methods would include operating the chip under voltage and/or temperature stress conditions for a time.

II. HOT CARRIER EFFECTS

By the advances in VLSI fabrication technologies, the reduction of device dimensions such as the channel length, the junction depth and the gate oxide thickness without proportional scaling of the power supply voltage, results in significant increase of the horizontal and vertical electric field in the channel region. Hot carrier induced degradation of MOS transistors is caused by the injection of high-energy electrons and holes into the gate oxide [2-4,10-12]. The oxide damage is in the form of charge trapping and/or interface trap generation which gradually builds up changes the current-voltage characteristics of the transistor. Hot carrier effects cause gradual changes in device characteristics during circuit operation. Although the circuit performance is ultimately affected by these changes, the continious nature of degradation mechanisms presents some special

challenges in analysis and estimation of reliability. The damage caused by hot carrier injection affects the transistor characteristics by causing a degradation in transconductance, a shift in the threshold voltage and a change in the drain current capability. This degradation in the device leads to the degradation of circuit performance over time.

III. WEIBULL DISTRIBUTION

The Weibull distribution is often used to describe the life times of parts [5]. When a number of parts are put on a test, they don't all fail at the same time. If parts fail according to a Weibull distribution, the probability that any single part will fail at a particular time, t is

$$F(t) = 1 - \exp\left[-\left(\frac{t}{a}\right)^b\right] \quad (1)$$

where "a" is called the scale parameter, "b" is called the shape parameter and F is called the cumulative disribution function. The values of a and b are estimated from the data by using linear regression [7]. By plugging a and b into the formula we can calculate F (the probability of failure) at any time, t.

The equation for F(t) can be turned into a regression equation as follows;

$$\ln[1 - F(t)] = -\left(\frac{t}{a}\right)^b \quad (2)$$

The reliability function is calculated by the formula;

$$R(t) = 1 - F(t) = \exp\left[-\left(\frac{t}{a}\right)^b\right] \quad (3)$$

When we perform a regression fit of a straight line to a set of (x,y) data points we typically minimize the sum of squares of the "vertical" distance between the data points and the line.

The correlation coefficient shows the statistical dependence of a non-functional relation between two variables. The value of the correlation coefficient (ρ) changes between –1 and +1 extremums ($-1 \leq \rho \leq +1$). If the correlation coefficient ρ has a value near ±1, it defines a strong and linear relation. If ρ=0 it means that the variables are statistically independent. Suppose that we observe an event with two variables. If we change the values of one variable which can be controlled, the another variable will have an interval of "possible values". The variable which can be controlled is called the independent variable and the other one which can not be controlled is called the dependent variable. [6,8,9]

In this study we accept time as independent variable and the measured current and voltage % changes as dependent variable.

IV. EXPERIMENTS AND APPLICATION EXAMPLE

Experiments were performed on two types of transistors with different dimensions; namely, CD4007 NMOS transistors (W=305µm, L=14µm) and NMOS transistors produced by TÜBİTAK with 3µ technology (W=27µm, L=3µm) From the experimental results for different stress conditions it is observed that the threshold voltage decreases and the drain current increases with time [10-11]. The experiments were realized with *semiconductor parameter analyser* HP 4155 at ITU Electronic Laboratory. The parameters found by using linear regression method, are used in the Weibull distribution to calculate the estimated values. The test circuit to apply a stress on the MOS transistors is illustrated in Fig.1.

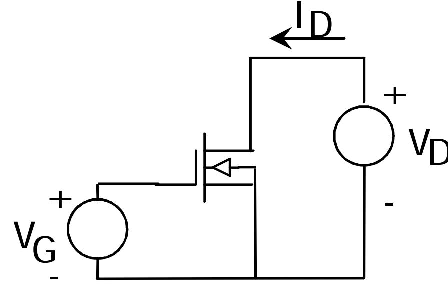

Figure 1. Test circuit to apply a stress on the MOS transistor realized with *semiconductor parameter analyser* HP4155

By using experimental data and the linear regression method, the Weibull parameters are calculated and illustrated in Table 1.

Table 1. The correlation coefficients and the Weibull parameters which are used to calculate the estimated values of I_d and V_{th} variations of long and short channel transistors.

Long channel Id	shape parameter	scale parameter	correlation coefficient
Vd=10V Vg=1V	0,30134	1,01E+12	0,79323
Vd=10V Vg=3V	0,33256	3,30E+08	0,918642
Vd=10V Vg=5V	0,10143	1,88E+23	0,83834

Long channel Vth	shape parameter	scale parameter	correlation coefficient
Vd=10V Vg=1V	0,73003	1,84E+04	0,956304
Vd=10V Vg=3V	0,962096	1,97E+03	0,956901
Vd=10V Vg=5V	1,01323	1,37E+03	0,945853

Short channel Id	shape parameter	scale parameter	correlation coefficient
Vd=5V Vg=1V	0,643323	3,95E+04	0,966958
Vd=5V Vg=1,5V	0,66694	8,84E+04	0,859875
Vd=5V Vg=2V	0,42557	1,72E+06	0,941363

Short channel Vth	shape parameter	scale parameter	correlation coefficient
Vd=5V Vg=1V	1,0727	1,48E+02	0,811241
Vd=5V Vg=1,5V	1,45316	8,92E+01	0,978418
Vd=5V Vg=2V	1,2567	8,21E+01	0,969851

The changes in the threshold voltage V_{th} and the relative variations in the drain current ΔI_d / I_d are estimated for short and long channel transistors by the use of Weibull distribution and are given with experimental values in Figs. 2,3,4,5.

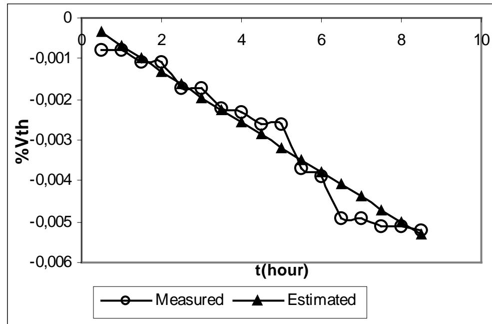

Figure 2. The estimated and the measured $\%V_{th}$ variation values of long channel transistor (V_d=10V, V_g=3V)

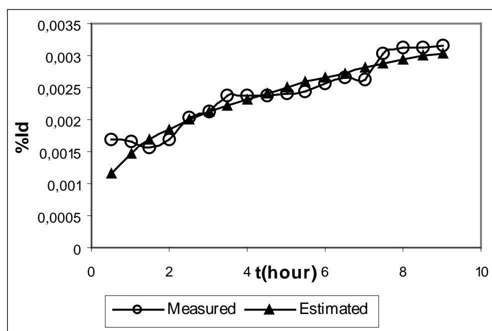

Figure 3. The estimated and the measured $\%I_d$ variation values of long channel transistor (V_d=10V, V_g=3V)

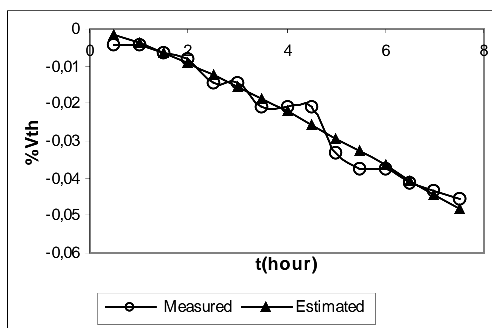

Figure 4. The estimated and the measured $\%V_{th}$ variation values of short channel transistor (V_d=5V, V_g=2V)

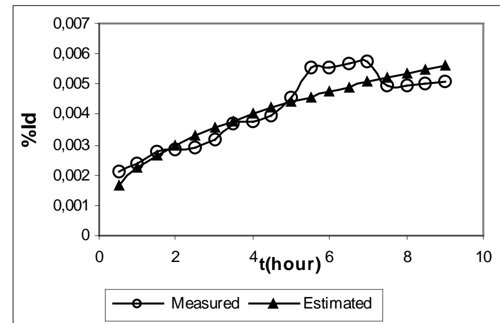

Figure 5. The estimated and the measured $\%I_d$ variation values of short channel transistor (V_d=5V, V_g=2V)

The estimated values are calculated by the Weibull distribution equations. The reliability curves of V_{th} and I_d variations at three different operating points are obtained and are shown in Figs. 6,7,8.

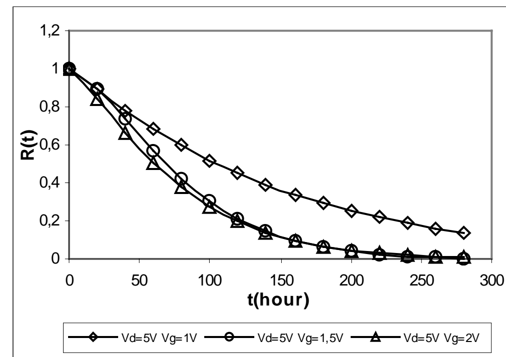

Figure 6. The V_{th} variation reliability curves of short channel transistor at three different operating points.

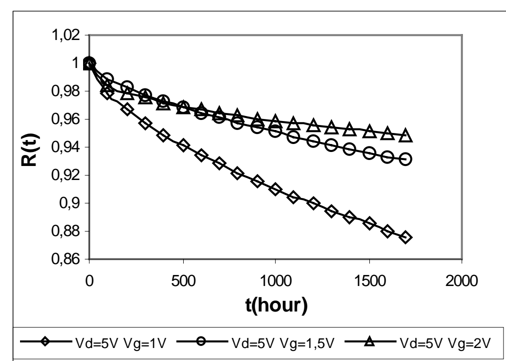

Figure 7. The I_d variation reliability curves of short channel transistor at three different operating points.

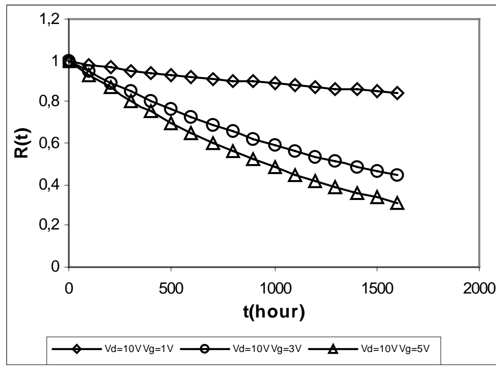

Figure 8. The V_{th} variation reliability curves of long channel transistor at three different operating points.

In Figures 2, 3, 4, 5, 6, 7 and 8; it can be easily seen that the estimated and the measured values are in good agreement.

The advantages provided by the method proposed is demonstrated on an application example, namely on the properties of the current source-loaded single stage amplifier shown in Fig.9 which is mostly used as an intermediate stage in operational amplifiers, OTAs, audio amplifiers. Furthermore it was shown in recent works that the total harmonic distortion of the active-loaded single stage amplifier depends strongly on the operating point where the total harmonic distortion crosses through a minimum at a special biasing point. [13, 14].

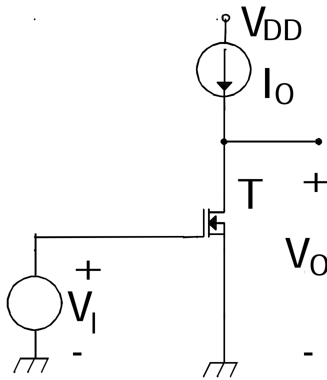

Figure 9. Single stage active-loaded MOS amplifier

Any shift in operating point influences the harmonic distortion properties of the amplifier, which is demonstrated by SPICE simulations using an accurate MOSFET model intended especially for accurate simulation of analogue building blocks [13,14]. The supply voltage was V_{DD}=5V. The operating point of the amplifier was chosen at V_O=2.85V and I_O=200μA. Simulation results obtained for the case of non-stressed operation yield the plot of THD against V_{OQ} illustrated in Fig.10.

V_{OQ} is the operating drain-source voltage of the NMOS driver transistor. Simulation results show that the total harmonic distortion crosses through a minimum point of THD_{min} = 0.177% at V_{OQ} = 2.85V.

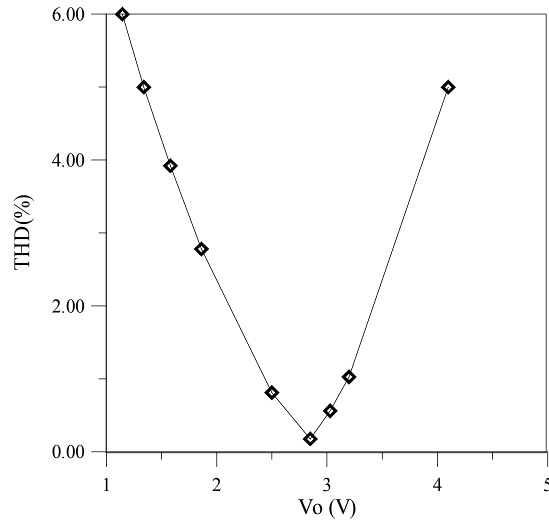

Figure 10. Dependence of total harmonic distortion of active-loaded amplifier stage on operating point.

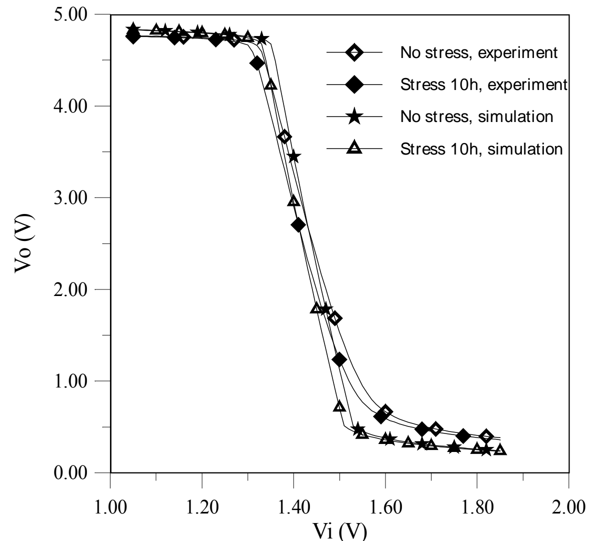

Figure 11. Experimental and simulated dependence of dc transfer curve on stress time

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The aim is to predict the changes in dc transfer curve and in the total harmonic distortion properties of the amplifier caused by hot-carrier degradation in the threshold voltage. For experiments, the load transistors were chosen as bipolar transistors to avoid any additional hot-carrier effect caused by PMOS load transistors. Measurements were performed by using HP 4155 Parameter Analyzer. The threshold voltage before the stress is specified as V_{th}=0.53V. The value of V_{th} decreases to V_{th}=0.5V after a stress of 10 hours which can be also predicted by using the proposed method. The dependence of dc transfer curve on stress time is obtained experimentally and given in Fig.11. Note that the operating point of the amplifier will be shifted on the dc transfer curve because of the hot carrier degradation which causes a change in the minimum point of the total harmonic distortion. The

mid-point of the transfer characteristic is specified as V_I=1.44V and V_O=2.5V. SPICE simulations result in a mid-point of V_I=1.44V, V_O=2.51V. After applying a stress of 10 hours the experimentally determined V_O is shifted to V_O=2.15V for V_I=1.44V. With the predicted threshold voltage of 0.493V SPICE simulations result in V_O=2.01V for V_I=1.44V. Using the method proposed, the change in the MOS threshold voltage is calculated for stress times of 5, 10, 15, 20, 30, 40 and 50 hours, respectively. The predicted values are illustrated in Table 2. For each of these predicted values the shift in the operating point of the amplifier and the total harmonic distortion THD for constant input biasing of V_I=1.43V (input biasing at minimum point for non-stressed operation) are obtained by SPICE simulations and given in Table 2. It can be clearly observed from the results that the method proposed is useful to predict accurately the shift in the operating point caused by the change in the threshold voltage due to the hot-carrier effect. Note that experimental results are obtained for a maximum stress time of 10h. Theoretical results are found to be in good agreement with experiments for this period. Starting from this good agreement and using the Weibull distribution the circuit behaviour for longer stress time periods can be also predicted which demonstrates the prime importance of this work.

Table 2. Prediction and SPICE simulation results for the dependence of V_{th} , operating point and THD on stress time

Stress time (h)	V_{th} (V)	V_I for V_O = 2.5V	THD for V_I = 1.43V
0	0.53	1.44	0.177%
5	0.51449	1.425	1.318%
10	0.49368	1.405	3.495%
15	0.47094	1.38	6.01%
20	0.44733	1.36	8.48%
30	0.399964	1.31	-
40	0.35340	1.265	-
50	0.30995	1.22	-

It can be observed from Fig.11 that the operating point is shifted to V_{OQ} = 1.68V after a stress of 10 hours. SPICE simulations with accurate model result in that the total harmonic distortion is increased to a much higher value of THD = 3.495% compared to the minimum. Results in Table 1 demonstrate clearly the degradation in the amplifier performance and the advantage provided by the proposed approximation.

V. CONCLUSION

In this study the variations of threshold voltage and drain current caused by the influence of hot-carrier effects are examined. The estimated values calculated by the Weibull distribution are compared with the measured values. High correlation coefficients and accomodated results are obtained in most of the samples. The suggested method can be suitable for PMOS and NMOS transistors with different dimensions because it depends on the measured values. By the results of a SPICE simulation using this knowledge, it is possible to determine the influence of hot-carrier effects to the circuit performance in the course of time. This will supply facility in working for the integrated circuit designers.

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