Design Considerations of MOS-Only Allpass Filters

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Abstract

In this paper, a simple filter topology that can be used to implement first-order MOS-only allpass filter is proposed. The proposed MOS-only allpass filter offers inherently very accurate magnitude and phase characteristics at very high frequencies. However, MOS-only active filter suffers from an inherent low frequency limitation. In order to address this issue, the modification technique allowing the derivation of MOS-only filter which allow extension of the operating frequency towards lower frequency region is proposed. Detailed simulations results of the filter modified according to the proposed technique are also provided in order to verify the usefulness of the theoretical approach.

1. Introduction

In this paper, filters called as MOS-only filters, which do not employ any external passive components, neither capacitors nor inductors, but rather which exploit the intrinsic capacitors of the MOS transistors are studied [1-8]. These circuits provide very useful advantages from IC realization viewpoint such as: *i*) low occupied chip area as a result of using as reactive component MOS capacitances with higher capacitance density compared to those of intentional, external capacitors. *ii*) operating at high frequencies since most significant parasitic capacitances are taken into account during the synthesis procedure. *iii*) electronic tuning property of the important filter parameters, since the design of these circuits relies on the device transconductances, which can be controlled by bias currents. In this paper, a simple filter topology that can be used to implement first-order MOS-only allpass filter is proposed.

On the other hand, MOS-only active filters suffer from an inherent low frequency limitation. This fact can be intuitively justified by noting that filters' natural frequencies are proportional to g_m/C_{gs}, where g_m is the device transconductance and C_{gs} is the gate-source capacitance. Therefore, for achieving low natural frequencies, either the value of g_m, i.e. MOS biasing current, should be decreased or the value of C_{gs} should be increased. However, MOS biasing current cannot be decreased below a specific value at which the transistor enters the subthreshold region where filter suffers from large distortion due to the governing transistor's exponential nonlinearity. On the other hand, to increase the value of C_{gs} implies the use of large devices that increase the chip area occupied by the circuits. In order to address this issue, the modification technique allowing the derivation of MOS-only filter, which allows extension of the operating frequency towards lower frequency region is proposed.

Simulation results performed using Spectre simulator in Cadence design environment verifying the proper operations of the allpass circuit are provided. The second-order effects, as well as some remedies for these are also discussed.

2. General Allpass Filter Topology

Throughout this paper, unless otherwise noted explicitly, *i*) all MOS transistors are assumed to operate in saturation region, *ii*) transistors' bulks and sources are interconnected so that transconductances from the body, g_{mb}, are neglected, *iii*) only the gate source capacitances, C_{gs} are considered, *iv*) the gate drain capacitances, C_{gd}, and parasitic junction capacitances, C_{sb} and C_{db}, are neglected. After these considerations, the MOS small-signal model used in the synthesis procedure becomes as in Fig. 1a.

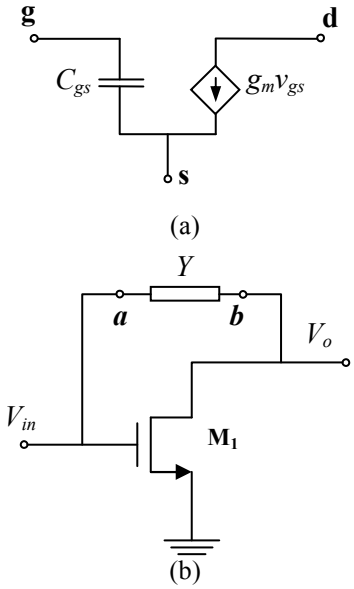

Fig. 1. a) Simplified small-signal device model used in the filter synthesis. b) General allpass filter topology

The proposed general allpass topology is given in Fig. 1(b). The circuit (small-signal) transfer function is given by:

$$T(s)=\frac{V_0}{V_{in}}=1-\frac{g_{m1}}{Y} \tag{1}$$

where g_{m1} is the transconductance of the NMOS transistor and Y is the admittance of the floating two-terminal. From this expression, it can easily be shown that the circuit realizes first-order allpass function when the floating two-terminal is chosen as a parallel RC circuit ($Y=sC+G$). Thus, the obtained circuit realizes the following first-order allpass function, provided that $g_{m1}=2G$.

$$T_1(s)=\frac{sC-G}{sC+G} \tag{2}$$

In order to complete the synthesis of the MOS-only allpass filter, the circuit simulating parallel RC impedance is to be obtained. The MOS-only simulators of the parallel RC and the unilateral floating parallel RC circuits are depicted in Fig. 2. It is easy to verify that these active-only circuits realize the desired functions with $R=1/g_{m2}$, $C=C_{gs2}$.

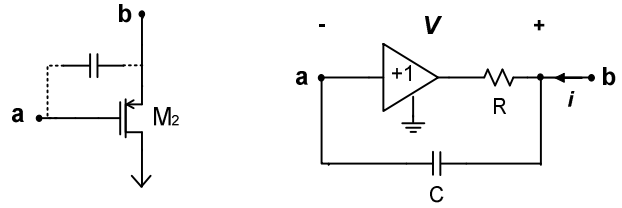

Fig. 2. Simulator of a parallel RC circuit

Now, using the simulator in Fig. 2 in the general filter topology of Fig. 1b, one can readily obtain active-only allpass filter as in Fig. 3 for the first-order case. Note that, the circuit is given in differential-mode; hence it also enjoys all the advantages of differential-mode of operation. The transfer function of the circuit in Fig. 3 is given by:

$$\frac{V_0^+-V_0^-}{V_{in}^+-V_{in}^-}=T_1(s)=\frac{sC-(g_{m1}-g_{m2})}{sC+g_{m2}} \tag{3}$$

Assuming that all transistors operate in saturation and the corresponding pair of transistors, i.e. M_{ia} and M_{ib} are perfectly matched, the circuit in Fig. 3 realizes the first-order allpass function, provided that

$$g_{m1}=2g_{m2} \tag{4}$$

In the proposed circuit, the DC drain currents of the transistors can be expressed in terms of the biasing currents as $I_{D1a,b}=I_{01}$, $I_{D2,ab}=I_{02}$ for the circuit in Fig. 3.

Given that device transconductances are given by $g_{mi}=\sqrt{\mu C_{ox}\, I_{Di}\, W/L}$, i=1, 2 where I_{Di} is the drain current of transistor pairs $M_{ia,b}$ and provided that transistors' aspect ratios are equal, this condition can also be met by setting $I_{01}=4I_{02}$.

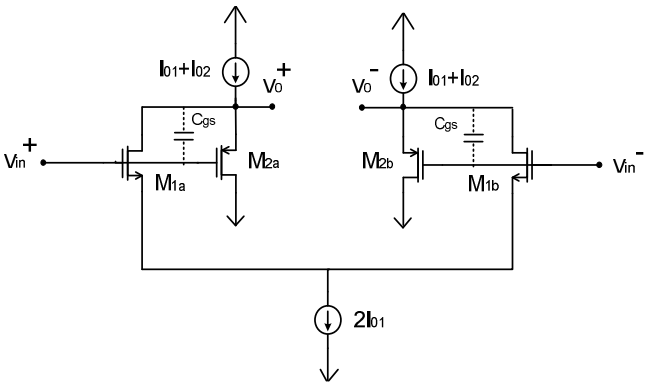

Fig. 3. Proposed MOS-only first order allpass filter

3. Simulation Results

To verify the theoretical study, the allpass filter was simulated using Spectre simulation tool in Cadence design environment using the parameters of a standard CMOS 0.35µm twin-well process. The filter was biased with ±1.65V DC power supply and all the current sources shown in Fig. 3 were realized using simple CMOS current mirrors.

The values of the biasing currents are chosen as I_{01}=64 µA and I_{02}=16 µA. With these biasing values, transconductances of the transistors are measured as g_{m1}=343 µA/V and g_{m2}=170 µA/V. For this biasing value, the gate-source capacitances of the transistors $M_{2a,b}$ were 1.6pF. The simulated magnitude and phase responses as well as the ideal characteristics are shown in Fig. 4. Using the parameter values in the transfer function of Eqn. (3), the pole frequency, f_0, is found as 16.6MHz, which agrees well with the value obtained from the simulation results as 16.9MHz. In general, these simulation results also verify the proper operation of the MOS-only first-order circuit.

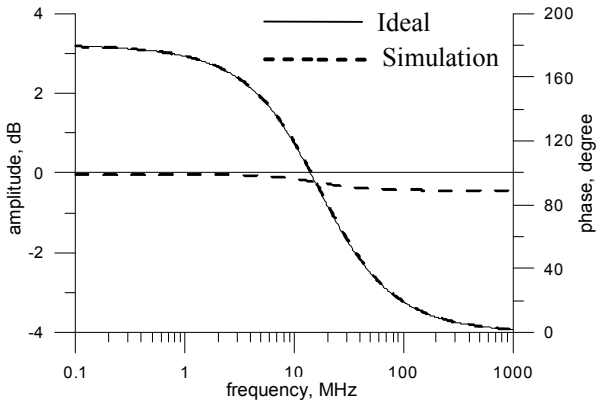

Fig. 4. Simulation results of the first-order allpass filter

4. Second-Order Effects

In this section, the effects of body transconductances, gate-drain capacitance and parasitic junction capacitances to the allpass filter characteristics are studied (see Fig. 5). Taking into account all these second-order non-idealities, routine analysis of the first-order allpass filter in Fig. 3 yields the following transfer function:

$$\frac{V_0^+ - V_0^-}{V_{in}^+ - V_{in}^-} = \frac{C_a}{C_b} \frac{s - \frac{g_{m1} - g_{m2}}{C_a}}{s + \frac{g_{m2} + g_{mb2}}{C_b}} \tag{5}$$

where $C_a=C_{gs2}+C_{gd1}$ and $C_b=C_a+C_{sb2}$.

From this expression, it is clearly seen that the second-order effects are almost fully compensated by modifying the allpass condition in Eqn. (4) as $g_{m1} = (1+\frac{C_a}{C_b})g_{m2} + \frac{C_a}{C_b} g_{mb2}$, except for the fact that the filter has a constant magnitude slightly lower than unity. It should be also noted that the circuit is sensitive to the body transconductance, g_{mb}.

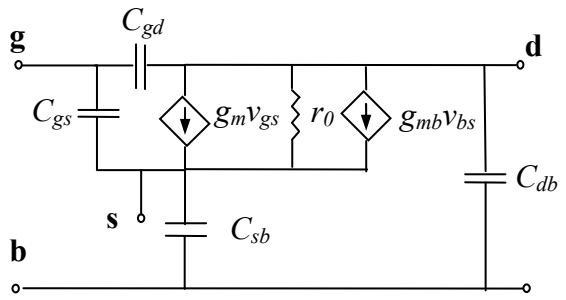

Fig. 5. Small-signal device model

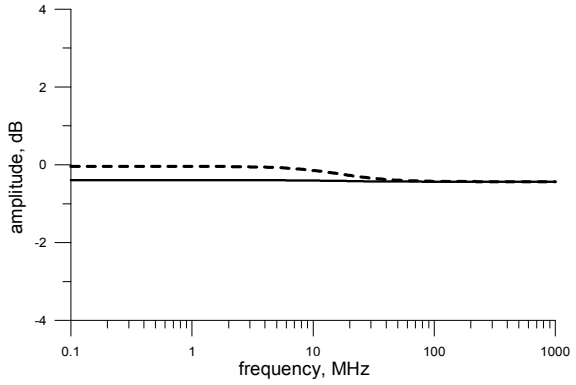

Fig. 6. Simulation results for the first order allpas filter

According to the modifying the allpass condition, the obtained simulation results of the allpass filter is shown in Fig. 6. From this simulation result, it is clearly seen that the magnitude characteristic of the filter remains constant in the wide range frequency region.

5. Low Frequency Limitations of MOS-Only Filter

As mentioned earlier, MOS-only active filters have inherent low frequency limitations since the filters' natural frequencies are in general proportional to g_m/C_{gs}, where g_m is the device transconductance and C_{gs} is the gate-source capacitance. However, for low frequency operation either the value of g_m, i.e. the MOS biasing current, should be decreased or the value of C_{gs} should be increased. The MOS biasing current cannot be decreased beyond the values where the transistors operate in subthreshold regions since exponential nonlinearities may lead to large THD at filters' outputs. On the other hand, to increase the value of C_{gs} implies the use of large devices that increase the chip area occupied by the circuits.

To overcome this problem, we introduce a technique shown in Fig. 7, which is based on capacitance multiplication. If the designed capacitance multiplier is located in the circuit properly, the value of the C_{gs} is increased. The main idea of this technique is that it senses the current of C_{gs} and multiplies this current with the current gain of the current sensor element.

For this pupose, the circuit should be designed such that the current gain between X and Z terminals is greater than unity, where K is the capacitance multiplication parameter, the value of which is greater than unity.

It is clearly seen from the Fig. 7 that the current of the intrinsic gate capacitor is sensed and fed back to the terminal Z after scaling it with a factor K.

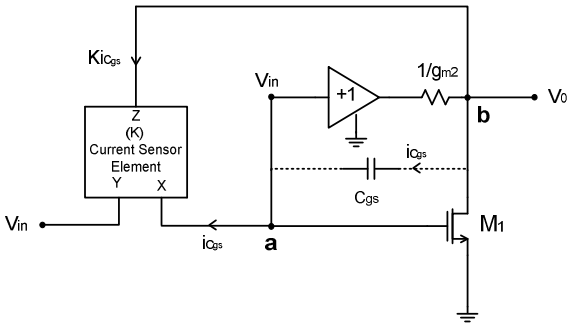

Fig.7. The proposed technique for low frequency operation

In order to clarify the versatility of the proposed technique, we applied the proposed technique to the circuit in Fig. 3 and obtained the modified filter shown in Fig. 8. The current gain is obtained such that the ratio of the current mirrors' transistor dimensions is set to factor K. Routine analysis of this circuit yields the following equation:

$$\frac{V_0^+ - V_0^-}{V_{in}^+ - V_{in}^-} = T_1(s) = \frac{sC(K+1) - (g_{m1} - g_{m2})}{sC(K+1) + g_{m2}} \tag{6}$$

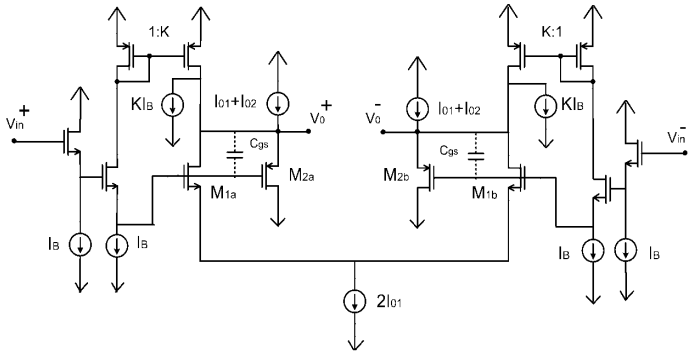

Fig.8. MOS-only allpass filter modified according to the proposed technique

In order to illustrate the feasibility of the approach, we have designed and simulated the filter using Spectre simulation tools

in Cadence design environment using model parameters of 0.35μm CMOS process.

The simulated phase responses of the modified filter are shown in Fig. 9. From these results, the 90° pole frequency of the modified filter is measured as 4MHz. Since the pole frequency of the initial filter was 16.6MHz, it is seen that the value of the pole frequency is decreased by a factor of 4, which is in perfect agreement with the theoretical prediction.

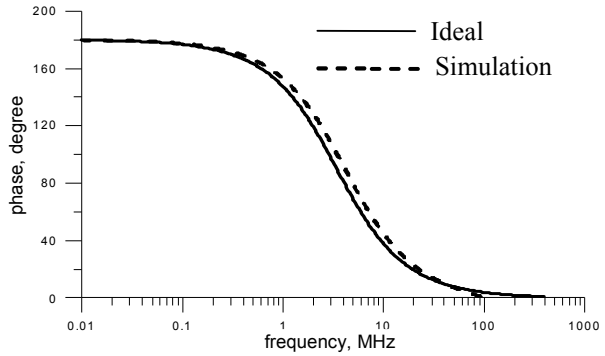

Fig.9. Phase characteristics of the modifying first-order allpass filter (K=4)

6. Conclusions

In this paper, a MOS-only allpass filter having a simple topology with electronically adjustable filter parameters is presented. Cadence Spectre simulation results are provided in order to verify the usefulness and feasibilities of the circuit. Furthermore, in order to address low frequency limitations of the MOS-only active filter, capacitance multiplication technique is proposed. An allpass filter with a 90° pole frequency as low as 4MHz is obtained by modifying the allpass filter according to the proposed technique. It is also concluded from the filter simulation results that allpass filter has an electronic tuning range of approximately half decade.

7. References

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