Pulse Omission Fractional Frequency Synthesizer

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Abstract

This article presents a design of new principle of the fractional frequency synthesizer based on charge balancing for spurious phase modulation suppression when pulses are periodically removed from pulse train. The new synthesizer can be used also as a universal building block in phase locked loop frequency synthesizers. The mathematical analysis and simulations of the system are also presented.

1. Introduction

The aim of frequency synthesis is to generate an arbitrary frequency from a given standard frequency or frequencies. Today, the frequency synthesizers are also an essential part of any modern transceiver system. They generate clock and oscillator signals needed for up and down conversion. The fine frequency resolution, low spurious signals, accuracy and stability are most important for these devices. The two most popular structures of radio-frequency synthesizers are the fractional-*N* frequency synthesizer and the integer-*N* frequency synthesizer. Although fractional-*N* synthesizer owns a great performance in frequency resolution and settling time, its division number depends on accumulator carrier which may lead to spur noise closing to the wanted signal due to the periodically produced characteristic. Consequently, compared with the integer-*N* frequency synthesizer, a more complicated modulator is needed to alleviate the influence of noise for fractional-*N* synthesizer [1 - 7].

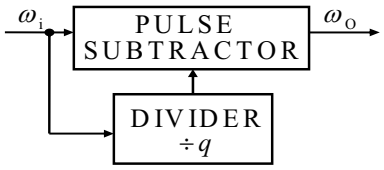

Fig. 1. The block diagram of pulse swallowing of each *q*-th pulse.

One of the simplest solutions for generating desired frequency from reference frequency is pulse-swallow integer-*N* frequency synthesizer (see Fig. 1). Suppose a pulse train in which pulses are placed in regular distances T_i (frequency ω_i) on time axis. If we remove each *q* pulse, then one period is missing and phase undergoes a step change equal 2π, that is,

$$\varphi(t) = \omega_i t - 2\pi V(t_k) \tag{1}$$

where $V(t_k)$ is the step function occurring at instances

$$t_k = kqT_i \tag{2}$$

where k=…-1, 0, 1, 2, …, and the average frequency ω_O may be expressed as

$$\omega_O = \omega_i \frac{q-1}{q} \tag{3}$$

The simulation of input pulses, pulse omission of each 8th pulse (q=8), equally distributed output pulses and spurious phase modulation is shown in Fig. 2. [8, 9, 10].

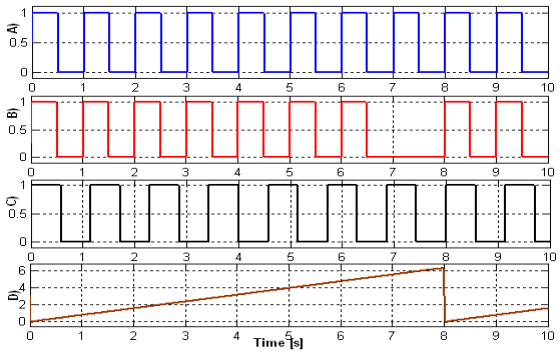

Fig. 2. The time diagram of A) input pulses, B) pulse omission of each 8th pulse (q=8), C) equally distributed output pulses and D) spurious phase modulation.

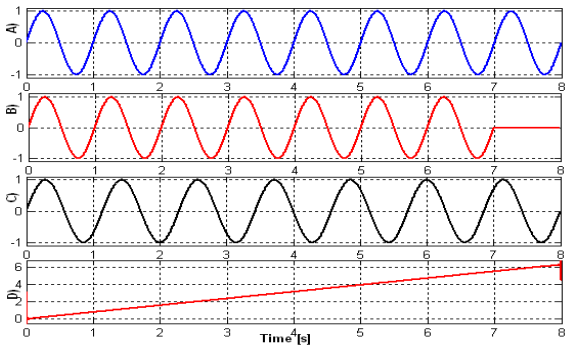

Fig. 3. The time diagram of sine wave signals for calculation of frequency spectrum. A) input, f_i=1 Hz B) one period omission of each 8th pulse (q=8), C) desired sine wave signal f_O=0.875 Hz according (3) and D) spurious phase modulation.

For frequency spectrum calculation, the sine wave signals were used (see Fig. 3). The frequency spectrum of signal with

period omission (q=8) and continuous sine wave signal with desired frequency f_O=0.875 Hz is shown in Fig. 4. The frequency spectrum has bad spectral purity and therefore new frequency synthesizer was developed.

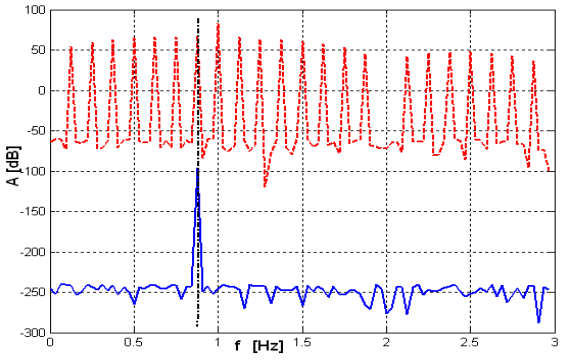

Fig. 4. The frequency spectrum of period swallowing (each 8-th period), top and spectrum of continuous sine wave signal f_O=0.875 Hz, shifted bottom.

2. A New Concept in Frequency Synthesis

The block diagram of fractional frequency synthesizer is presented in Fig. 5. Suppose, that synthesizer is controlled by microcontroller by Ctr1 (control of pulse swallowing) and Ctr2, calculated average value of signal from generator G. Other parts are SW - switch, V_R - reference voltage, Ctr2 - average value of signal with periodic pulse omission, I - integrator, A - amplifier, LP - low-pass filter, C - comparator, f/2 - frequency divider, f_O - output frequency.

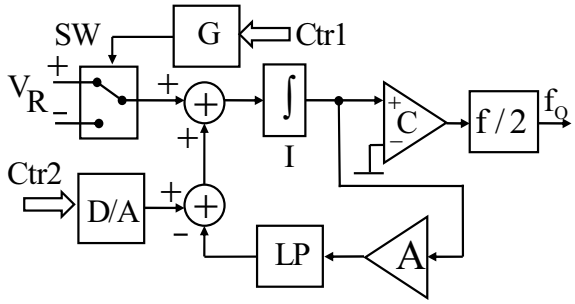

Fig. 5. The block diagram of fractional frequency synthesizer. Ctr1 - pulse swallowing control, G - generator with pulse swallowing possibility, SW -switch, Vr - reference voltage, Ctr2 - average value of signal with periodic pulse omission, I - integrator, A - amplifier, LP - low-pass filter, C - comparator, f/2 - frequency divider, f_O - output frequency.

The synthesizer output signal is derived according example presented in Fig. 6. for V_R = ±2 V and initial integrator voltage V_0. Suppose, that we have input signal (with period T = 5) with omission every 7th pulse (pulse is deleted in time t = 30, signal a) in Fig. 6). The number of pulses without omission pulses is N_P and number of deleted pulses is D_P. The inverted mean voltage V_M on the output of switch SW (for V_R = ±2 V) is given by eq. (4), for N_P = 7 and D_P = 1 (for signal b), Fig. 6).

$$V_M = V_R \frac{D_P T}{N_P T} = V_R \frac{D_P}{N_P} = V_R \frac{1}{7} = \frac{V_R}{7} = \frac{2}{7} = 0.2857 \quad (4)$$

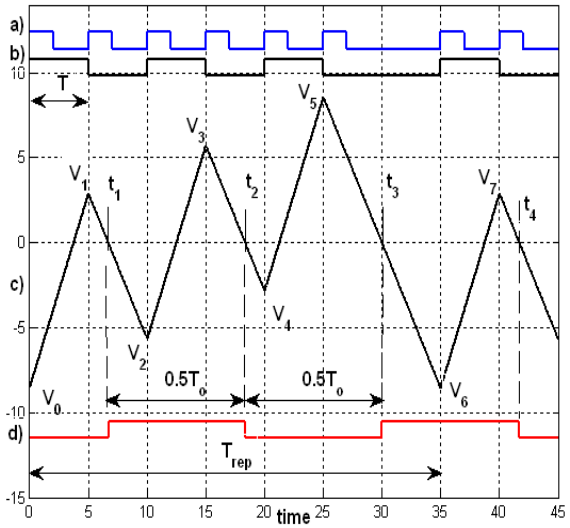

Fig. 6. The time diagram of signals in fractional frequency synthesizer based on pulse swallowing and charge balancing. a) Generator clock signal with pulse omission possibility, period T, b) signal a) divided by 2, c) integrator output, d) output signal f_O. T_{rep} - repeated period, output period T_O. $V_0 \div V_7$ voltage on integrator output, $t_1 \div t_4$ times of integrator voltage leading edge zero crossing.

The voltage V_M is calculated by means of D/A converter and its digital value is Ctr2. The mean voltage V_M on D/A output is added to voltage on output of the switch SW. Therefore for voltage $+V_R$ the voltage slope on integrator output is

$$k_+ = V_R + V_M \quad (5)$$

and for voltage $-V_R$ the voltage slope is

$$k_- = -V_R + V_M \quad (6)$$

Integrator output voltages $V_1 \div V_6$ are given by

$$\begin{aligned}
V_1 &= V_0 + k_+ T = V_0 + (V_R + V_M)T \\
V_2 &= V_1 + k_- T = V_1 + (-V_R + V_M)T = V_0 + 2V_M T \\
V_3 &= V_2 + (V_R + V_M)T = V_0 + 3V_M T + V_R T \\
V_4 &= V_3 + (-V_R + V_M)T = V_0 + 4V_M T \\
V_5 &= V_4 + (V_R + V_M)T = V_0 + 5V_M T + V_R T \\
V_6 &= V_5 + (-V_R + V_M)2T = V_0 + (5V_M + V_R - 2V_R + 2V_M)T \\
&= V_0 + (7V_M - V_R)T \\
&= V_0 + (7V_M - V_R)T = V_0 + (7\frac{U_R}{7} - V_R)T = V_0
\end{aligned} \quad (7)$$

From the eq. (7) can be calculated that $V_6 = V_0$, $V_7 = V_1$ …, all is repeated periodically. The maximal voltage on integrator output is

$$\begin{aligned}\Delta V_{MAX} &= V_5 - V_6 = V_5 - V_0 = V_0 + (5V_M + V_R)T - V_0 \\ &= (5V_M + V_R)T\end{aligned} \tag{8}$$

and for $V_M = V_R/7$ according (4).

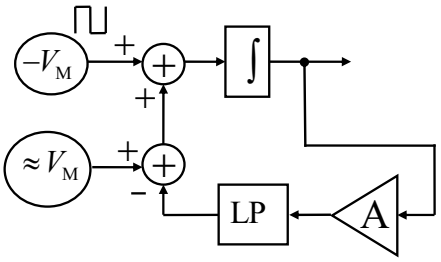

Fig. 7. The equivalent feedback loop of synthesizer. $-V_M$ mean value of pulsed voltage on switch output, $\approx V_M$ dc voltage from D/A converter, LP low pass filter, A amplifier.

The feedback loop consists of amplifier with gain A and low-pass filter LP. The loop holds zero average value on integrator output, see equivalent circuit in Fig. 7 (feedback loop balance some inaccuracy and differences between $-V_M$ and $\approx V_M$). Time t_1 (Fig. 6) can be determined when cross zero voltage of line from V_1 to V_2, where V_1 is

$$\begin{aligned}V_1 &= V_0 + k_+ T = V_0 + (V_R + V_M)T \\ &= \left(-\frac{6}{7}V_R + V_R + \frac{V_R}{7}\right)T = \frac{2}{7}V_R T\end{aligned} \tag{9}$$

and after some manipulation

$$t_1 = T + \frac{T}{3} \tag{10}$$

and similarly t_2 and t_3 (Fig. 6)

$$t_2 = 3T + \frac{2T}{3} \tag{11}$$

$$t_3 = 5T + T = 6T \tag{12}$$

and first half output period $0.5T_O$ is

$$0.5T_O = t_2 - t_1 = 3T + \frac{2T}{3} - \left(T + \frac{T}{3}\right) = \frac{7}{3}T \tag{13}$$

and second half output period $0.5T_O$ is

$$0.5T_O = t_3 - t_2 = 6T - \left(3T + \frac{2T}{3}\right) = \frac{7}{3}T \tag{14}$$

From eq. (13) and (14), frequency synthesizer output frequency is derived

$$\begin{aligned}f_O &= \frac{1}{T_O} = \frac{1}{0.5T_O + 0.5T_O} = \frac{1}{\left(\frac{7}{3} + \frac{7}{3}\right)T} = \frac{3}{14T} \\ &= \frac{3}{14}f_{CLK} = \frac{3}{14}\left(\frac{1}{5}\right) = 0.042857\end{aligned} \tag{15}$$

where is f_{CLK} generator frequency ($f_{CLK} = 1/T = 0.2$ in this example). From previous results the output frequency f_O can be derived

$$f_O = \frac{1}{4}\left(\frac{N_P - D_P}{N_P}\right)\frac{1}{T} = \frac{1}{4}\left(\frac{N_P - D_P}{N_P}\right)f_{CLK} \tag{16}$$

and for $N_P = 7$, $D_P = 1$ and f_{CLK}=0.2 Hz, the f_O is

$$f_O = (1/4)*[(7-1)/7]*0.2 = 0.042857 \quad [\text{Hz}] \tag{17}$$

The frequency spectrum of square wave signal simulation according previous equations is presented in Fig. 8 (for $N_P = 7$, $D_P = 1$ and f_{CLK}=0.2 Hz, amplifier gain $A = 0.0045$ and low-pass filter is 6th order Butterworth filter with corner frequency 0.04 [rad]), [11 - 15].

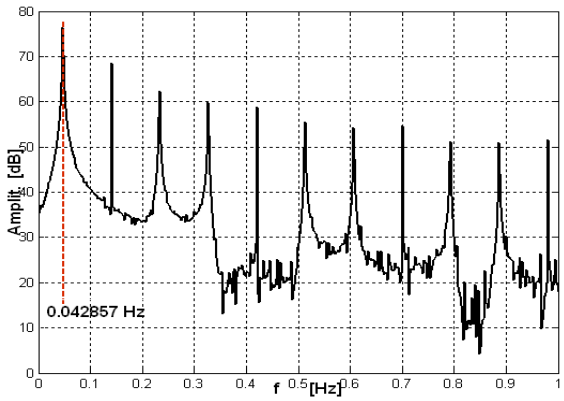

Fig. 8. The frequency spectrum of square-wave output signal of the synthesizer for NP = 7, DP = 1 and fCLK=0.2 Hz The amplifier gain is A=0.0045 and low-pass filter is 6th order Butterworth filter with corner frequency 0.04 [rad].

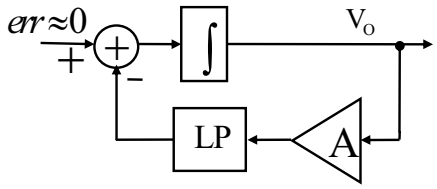

Fig. 9. The equivalent feedback loop for synthesizer stability evaluation.

3. Stability of Closed Loop

Because the synthesizer contain the feedback loop, it is important to solve stability. The simplified feedback loop is shown in Fig. 9. Input signal (err ≈ 0) is difference of the mean

value $-V_M$ (switch output) and $\approx V_M$ (D/A converter output). The closed feedback loop can be described by transfer function

$$\frac{V_O}{err} = \frac{\frac{1}{s}}{1+\frac{1}{s}AF_{LP}(s)} = \frac{1}{s+A\frac{N(s)}{D(s)}} = \frac{D(s)}{sD(s)+AN(s)} \quad (18)$$

where $N(s)$ and $D(s)$ are numerator and denominator of low-pass filter transfer function respectively and A is value of amplifier gain. For system stability the real parts of the roots of closed loop denominator must be negative. The stability and behavior of the closed loop is controlled by gain A of the amplifier. The step response of closed loop for amplifier gain A = 0.0078 and 6th order elliptic low-pass filter with corner frequency 0.04 [rad] is presented in Fig. 10.

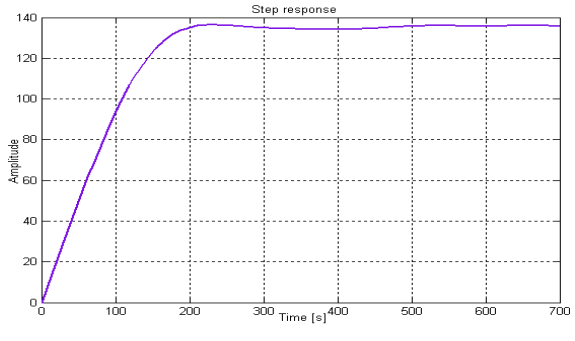

Fig. 10. The step response of the closed loop according Fig. 9 for elliptic 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.0078

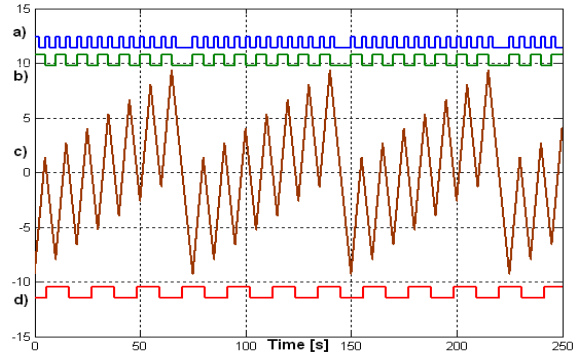

Fig. 11. The time diagram of signals in fractional frequency synthesizer based on pulse swallowing and charge balancing. a) Generator clock signal with pulse omission, b) signal a) divided by 2, c) integrator output, d) output signal f_O = 0.04666 [Hz], for N_P = 15, D_P = 1 and f_{CLK}=0.2 Hz

4. Simulations

The simulation result was derived for N_P = 15, D_P = 1 and f_{CLK}=0.2 Hz, amplifier gain A=0.0045 and 6th order Butterworth low-pass filter with corner frequency 0.04 [rad]. The output frequency, according (16) is f_O = 0.04666 Hz. Fig. 11 shows input signal a), b) input signal divided by 2 (on rising edge), c) integrator output, d) output signal.

5. Measurement Results

The simplified (low frequency) version of pulse swallowing frequency synthesizer was constructed and measured. The result of measuring confirmed theory and simulations. It is important to note that frequency of the output signal (in Fig. 12, 13 and 14) was not divided by 2, therefore output frequency is given by

$$f_O = \frac{1}{2}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} \quad (19)$$

The first example is shown in Fig. 12. In this example The N_P=89 and D_{P1} = 1. The output frequency is

$$f_O = \frac{1}{2}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} = \frac{1}{2}\left(\frac{89-1}{89}\right) 8.0 = 3.955 \text{ [kHz]}$$

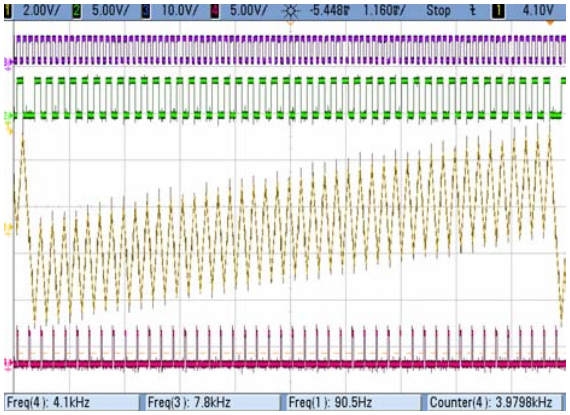

Fig. 12. The time diagram of signals measured in frequency synthesizer. a) Input clock signal, b) signal with pulse omission where input clock frequency with pulse omission is divided by 2, c) integrator output, d) output signal f_O = 3.96 kHz, for N_{P1} = 13, D_{P1} = 1 and f_{CLK}=8.0 kHz.

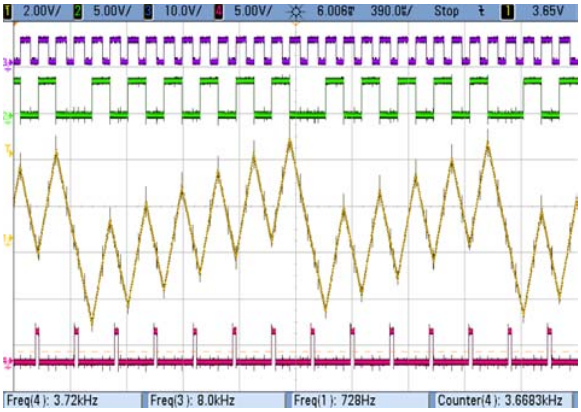

Fig. 13. The time diagram of signals measured in frequency synthesizer. a) Input clock signal, b) signal with pulse omission where input clock frequency with pulse omission is divided by 2, c) integrator output, d) output signal f_O = 3.67 kHz, for N_{P1} = 13, D_{P1} = 1 and N_{P2} = 11, D_{P2} = 1 and f_{CLK}=8.0 kHz.

In second example (Fig. 13) the 2 different values N_P are used. The N_{P1} is 13 and N_{P2} is 11 and $D_{P1} = 1$ and $D_{P2} = 1$. For this example $N_P = N_{P1} + N_{P2} = 24$ and $D_P = D_{P1} + D_{P2} = 2$. Output frequency is

$$f_O = \frac{1}{2}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} = \frac{1}{2}\left(\frac{24-2}{24}\right) 8.0 = 3.667 \quad [\text{kHz}]$$

In third example (Fig. 14) also the 2 different values N_P are used. The N_{P1} is 7 and N_{P2} is 5 and $D_{P1} = 1$ and $D_{P2} = 1$. For this example $N_P = N_{P1} + N_{P2} = 12$ and $D_P = D_{P1} + D_{P2} = 2$. Output frequency is

$$f_O = \frac{1}{2}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} = \frac{1}{2}\left(\frac{12-2}{12}\right) 8.0 = 3.33 \quad [\text{kHz}]$$

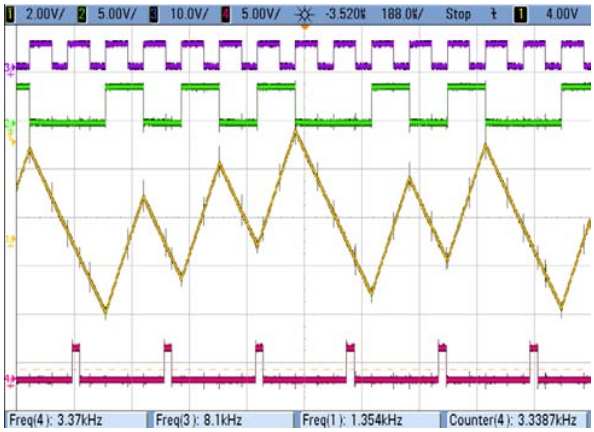

Fig. 14. The time diagram of signals measured in frequency synthesizer. a) Input clock signal, b) signal with pulse omission where input clock frequency with pulse omission is divided by 2, c) integrator output, d) output signal $f_O = 3.3$ kHz, for $N_{P1} = 7$, $N_{P2} = 5$, $D_P = 1$ and $f_{CLK} = 8.0$ kHz

6. Conclusions

A detailed look at the concept of new fractional frequency synthesizer based on pulse omission technique and charge balancing has been presented in this paper. The new synthesizer can be also used as a universal building block in different types of frequency synthesizers (e.g. phase locked loops). The main advantage of this synthesizer is simple generation of fractional frequency which is close to reference frequency. Analysis and simulation results of the new fractional synthesizer were also shown. The architecture described above was simulated in Matlab. The new frequency synthesizer was also constructed and measured results confirmed theoretical assumptions.

7. References

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Acknowledgment

This research was supported by the European Regional Development Fund and Ministry of Education, Youth and Sports of the Czech Republic under project No. CZ.1.05/2.1.00/03.0094: Regional Innovation Centre for Electrical Engineering (RICE).