A FULLY INTEGRATED RANGE-FINDER BASED ON THE LINE-STRIPE METHOD

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ABSTRACT

In this paper, an imaging chip for acquiring range information with 0.35 μm CMOS technology and 5V power supply has been described. The system can extract range information without any mechanical movement and all the signal processing is done on the chip. All of the image sensors and mixed-signal processors are integrated in the chip. The design range is 1.5m-10m with 18 scales.

I. INTRODUCTION

Range-Finding or measurement of the three dimensional profiles of an object or scene, is a critical point for many robotic applications. Numerous range-finding techniques are developed which light-stripe range-finding is one of the most common method [1]. A conventional light-stripe range-finder operates in a step-and-repeat manner. A light-stripe is projected onto a scene; a video image is acquired; the position of the projected stripe in the image is extracted; the stripe position is stepped and the process repeats until the entire scene has been scanned. The rate at which frames of range date can be acquired using this method is limited by the time needed to acquire and process each video image. Note that the number of video images required to build a complete range map increases linearly with the desired spatial range resolution.

The integrated range-finder is based on modification of the basic light-stripe range-finding technique described by Sato et al. [2] and Kida et al. [3]. In the modified method, which is based on parallel light-stripe, the range image is constructed in a parallel manner rather than serial one. Note that in light-stripe method (serial or parallel); an off-chip readout circuitry is needed.

Another technique is passive range-finding method. Passive range-finding techniques are generally based either on disparity in stereo vision or on focus/defocus in mono vision [4-6]. In [7-10], a number of auto-focusing or range-finding methods based on tilted sensor plane are proposed. However, they still suffer from a need for mechanical movement and/or a heavy signal processing overhead.

The technique we used in this paper is based on a sensor plane tilted at an angle with respect to optical axis, so that it is always intersected by the image plane regardless of the distance to the object plane. This technique extracts range information from single image in real time without any mechanical movement. The level of signal processing involved is so simple and accurate that all processing functions are integrated with the sensor matrix on the same chip without any readout circuitry.

The proposed system block diagram is shown in Figure 1.

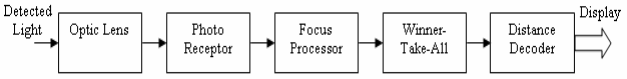

Figure 1. System block diagram

In this system, reflected light from object after crossing of optic lens, is received by photo receptor and generates analog signal which its output is proportional to the light intensity. All pixels in a row are evaluated by an embedded analog focus processor, which calculates the row-wise sum of the absolute value of the spatial second derivatives of pixel signals as a measurement of focus. These analog focus measurements are compared in the WTA[1], which identifies the row of the highest cumulative second derivative, means the highest focus. Finally, a digital distance decoder converts the index of the identified row to the distance information.

The range-finder covers the range 1.5*m*-10*m*. The photo receptor matrix which is used includes 18 lines and each line has 16 pixels, so the range is estimated in 18 levels and the distance between two successive ranges is 0.5*m*.

II. OPTIC LENS

As shown in Figure 2, the range-finder consists of a single optic lens and a sensor whose plane is tilted by an angle with respect to the optical axis. The sensor plane intersects optical axis at the focal point *F*. Any object at a distance *u* from lens projects its focused image on an image plane

[1]- Winner-Take-All

located at a distance v behind the lens. According to the Gaussian lens law, u is related to v by

$$\frac{1}{f} = \frac{1}{u} + \frac{1}{v} \qquad (1)$$

where f is the focal length. Therefore, object distance u can be calculated once the image plane distance v has been determined. Since the sensor plane is laid out at an angle, it intersects image plane for a range of u values and the position of the intersection line I_1I_2 along the w-axis of the sensor plane depends on u.

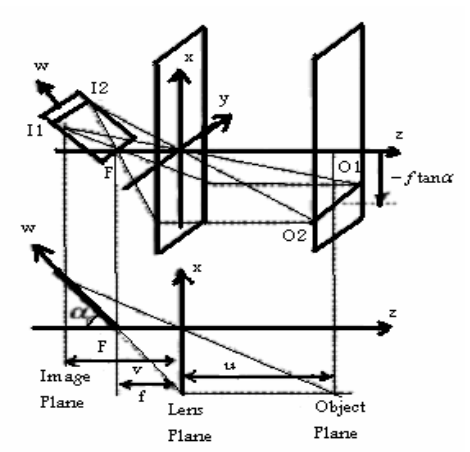

Figure 2. 3D and 2D views of the optic lens and image plane

Note that: 1) line I_1I_2 is where the best focus is obtained for a given u, 2) this line is a projection of a line O_1O_2 of the object plane, 3) the focusable object line O_1O_2 is always on the plane $x = -f.\tan\alpha$, regardless of the value of u. Therefore, the value of v and then u will be determined from the position w of the sensor line of the highest focus.

The lens is made off the shelf and the chip includes photo receptor, focus processor, winner-take-all and distance decoder.

III. PHOTO RECEPTOR

The adaptive receptor is shown in Figure 3(b) [11]. It consists of a source follower receptor input stage combined with amplification and low-pass filtered feedback. The output of the source follower receptor is amplified by the inverting amplifier consisting of Q_n, Q_{cas} and Q_p. The voltage gain $-A_{amp}$ is typically several hundred. Q_{cas} is a cascode that nullifies the miller capacitance from the gate to drain of Q_n and also doubles the gain of the amplifier.

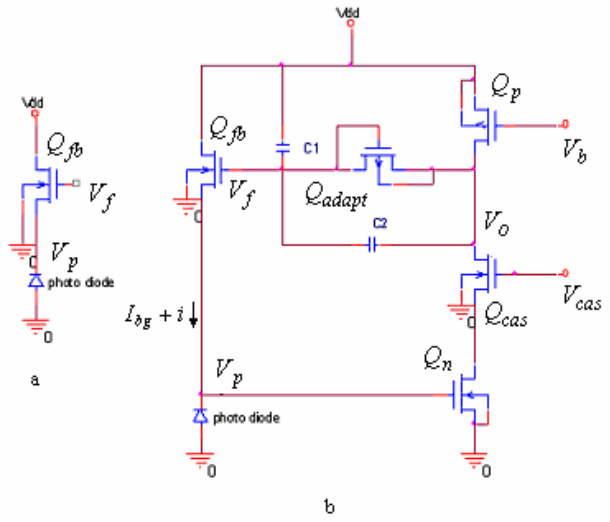

Figure 3. Receptor circuits (a) Source follower receptor (b) Adaptive receptor

The input current comes from a photo diode that generates a photo current that is linearly proportional to intensity [11]. The current consists of a steady-state background component, I_{bg}, and a varying or transient component, i. The photo diode is formed as an extension of the source of the feedback transistor Q_{fb}. For typical light intensities, Q_{fb} operates in sub threshold region.

The high gain in the feedback loop effectively clamps V_P. When the input current changes an e-fold, V_f must change by V_T/k (k is the back-gate coefficient) to hold V_P clamped. So the gain from V_f to V_P is k and from i to V_P is V_T per e-fold intensity change. Also the gain from V_o to V_f is 1 in steady-state and in transient, where the output must fed back to the input through the capacitive divider, is $C_2/(C_1+C_2)$. The closed-loop gain in steady-state and transient are given by (2) & (3).

$$A_{cl} = \frac{V_o/V_T}{i/I_{bg}} = \frac{1}{k} \qquad \text{(Steady-state closed-loop gain)} \qquad (2)$$

$$A_{cl} = \frac{V_o/V_T}{i/I_{bg}} = \frac{1}{k}\frac{C_1+C_2}{C_2} \qquad \text{(Transient closed-loop gain)} \qquad (3)$$

Equation (2) is equal the small signal equivalent of the large signal expression for the steady-state output voltage given by (4).

$$\frac{V_o}{V_T} = \log(I_b) + \frac{1}{k}\log\left(\frac{I_{bg}+i}{I_0}\right) \qquad (4)$$

IV. FOCUS PROCESSOR

Each line of the sensor plane is equipped with a focus processor to calculate the degree of focus along that line. The circuit of a 3-pixel focus processor comprising pixels *i*-1, *i* and *i*+1 is shown in Figure 4. Note that each photo diode drives a pair of NMOS transistors with a common drain. Also note that the diodes shown in Figure 4 are realized with diode-connected MOSFETs.

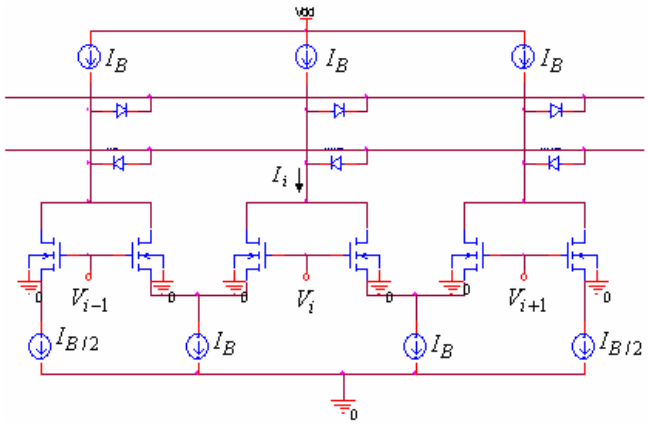

Figure 4. A 3-pixel slice of the focus processor

The common-drain current I_i of pixel-i is given by (5).

$$I_i = I_B - \frac{g_m}{2}[(V_{i+1} - V_i) - (V_i - V_{i-1})] \qquad (5)$$

The difference between I_B and I_i, approximates the second spatial derivative.

$$\Delta I_i \cong I_B - I_i = \frac{g_m}{2}[(V_{i+1} - V_i) - (V_i - V_{i-1})] \qquad (6)$$

If the second derivative is positive, this current flows out of pixel-*i* onto bus-1, and if it is negative, this current flows out of bus-2 into pixel-*i*. These two buses are kept out at virtually constant voltages by two opamps per row and their currents are summed up to generate the sum of absolute value of the second derivatives.

The measurement of focus is representing by SML[1]:

$$SML = \sum_{i=1}^{m-1} |\Delta I_i| \qquad (7)$$

The output current of focus processor, that is the sum of bus-1 and bus-2 currents, represents an analog focus measure for each line.

The current summer, which sums the absolute currents of bus-1 and bus-2, is shown in Figure 5.

[1]- Sum of Modified Laplacian

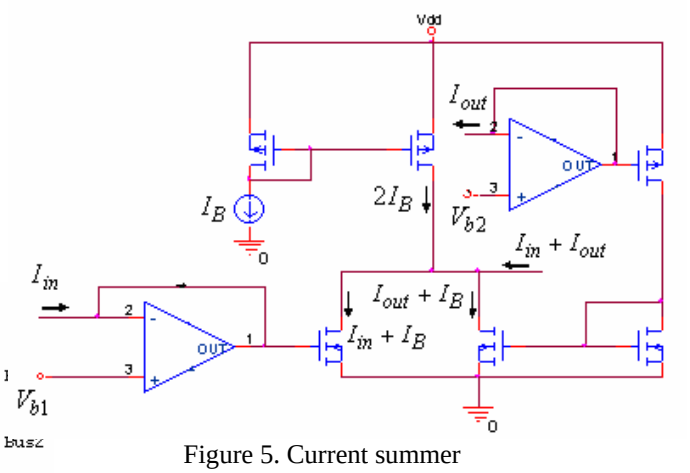

Figure 5. Current summer

V. WINNER-TAKE-ALL

Measurements of analog focus for each line, which are output currents of focus processors, are compared in a winner-take-all block. This circuit identifies the line of the highest output current, hence the highest focus.

Figure 6 is a schematic diagram of the winner-take-all circuit [12]. A wire associated with the potential V_C, computes the inhibition for the entire circuit. To compute the global inhibition, each neuron *k* contributes a current onto this common wire, using transistor M_{2_K}. To apply this global inhibition locally, each neuron responds to the common wire voltage V_C, using transistor M_{1_K}.

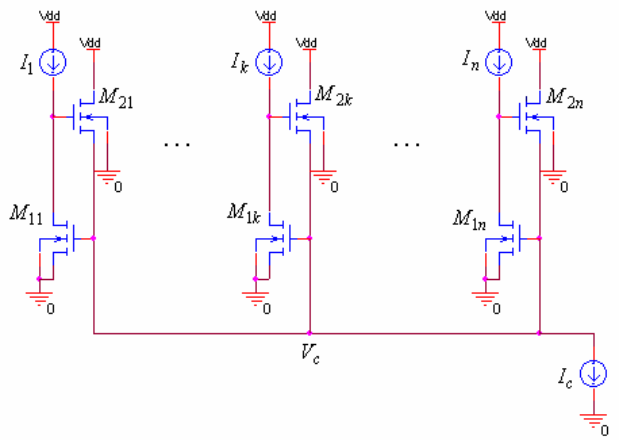

Figure 6. Schematic diagram of the winner-take-all circuit

VI. RESULTS AND SUMMARY

In this section, the simulated results with HSPICE and 0.35 μm CMOS technology for the described units are presented. Figure 7 shows DC sweep simulated result of the photo receptor. Usually the light intensity inside a normal room is below than 1 lux, and the level of intensity produces photo current less than 1*nA*. So, in this simulation, the input photo current has been considered between 0-5*nA*. According to Figure 7, for small photo currents which correspond to transient signals, the photo

receptor is very sensitive, but for large photo currents which correspond to steady-state signals, the photo receptor is adaptive and has small variations in the output.

The simulated transfer function of a slice of the focus processor, as defined by (6), is shown in Figure 8. Figure 9 shows the output currents of the 18 focus processors. The maximum SML belongs to the sensor line that corresponds to the correct distance.

Table I summarizes the properties of the designed chip.

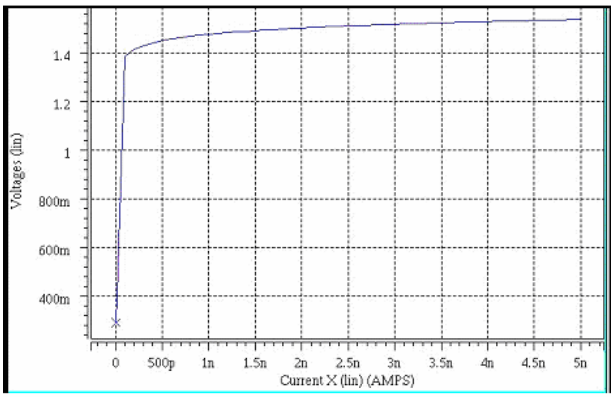

Figure 7. The output voltage DC sweep according to input photo current

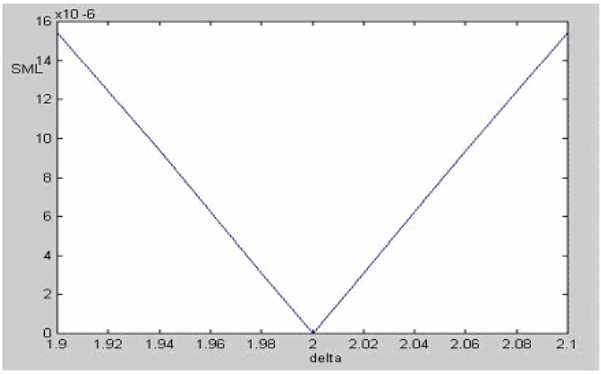

Figure 8. DC response of a slice of focus processor

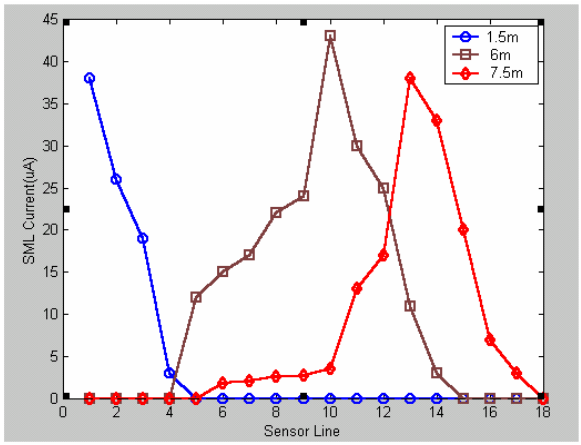

Figure 9. Output current of the 18 focus processors for three different object distances

Table I. Properties of the chip

Range of distance covered	1.5-10m (in 18 scales)
Power consumption	40mW
Technology	0.35 μm -CMOS
Power supply	5V

VII. CONCLUSION

The range-finding technique based on the passive imaging is presented that requires seasonable signal processing stages and can be implemented on a single mixed-signal CMOS chip including the photo sensor matrix. Simulated results are done with HSPICE and 0.35 μm CMOS technology for a 5V power supply.

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