Application of a Statistical Methodology to a Multiplier Using a Low Voltage Square-Law CMOS Analog Cell

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Abstract

A statistical design methodology which uses design of experiments (DOE) and response surface methodology (RSM) is applied to a low power multiplier. The description and initial simulation results of the circuit are given and the nonlinearity of the multiplier is statistically examined. Response surface methodology and design of experiment were used as statistical design techniques combined with the statistical MOS (SMOS) model. Device size optimization and yield enhancement is also demonstrated.

1. Introduction

The trend for lower supply voltages is forcing new design techniques for analog circuits. Analog multipliers are one of the most important building blocks for analog circuits since it is an essential part of many applications such as communications, analog signal processing and neural networks. Many applications require linear multipliers and matching is very important in order to obtain highly linear multipliers no matter what the implementation is [1-5].

Since random device/process variations do not scale down with feature size or supply voltage, statistical design of low voltage circuits is essential in order to keep functional yields of low voltage circuits at levels that are competitive and cost effective [6]. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog part must be minimized such that it has little effect on the yield of the mixed-signal chip.

A new multiplier, statistically robust with good yield is discussed in this paper. Section 2 examines the multiplier. The statistical VLSI design methodology using design of experiments (DOE) and response surface methodology (RSM) are reviewed in Section 3. The statistical design for the linearity performance of the multiplier is given in Section 4. Section 5 summarizes and concludes the work.

2. Description of the Circuit

The low input impedance at the source limits the applicability of a single MOS transistor. A solution would be to use the CMOS composite cell [7], given in Figure 1(a). However, it is not suitable for low voltage designs due to its high equivalent threshold voltage, $V_{Teq} = \mid V_{Tp} \mid + V_{Tn}$.

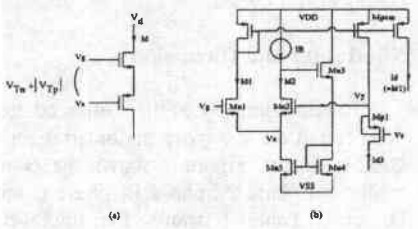

Fig. 1. a) Conventional composite transistor, b) Low voltage low power composite cell

The low voltage low power cell given in Figure 1(b) [8] has been presented in order to overcome the drawback of the composite transistor. Transistors M_{n1} and M_{p1} are the basic CMOS pair transistors. M_{pcm} is the group of PMOS transistors forming the current mirror to ensure that the currents flowing through transistors M_{n1} and M_{p1} are equal, by taking the current through M_{n1} and mirroring it to M_{p1}. The feedback loop formed by transistors M_{n2}, M_{n3}, M_{n4} and M_{n5}, and the bias current I_B always keeps the drain current of transistor M_{n2} equal to I_B. This makes the voltage drop V_{g2} (or $V_{gs2} - V_{Tn}$) of transistor M_{n2} constant. The drain current of the cell is given by

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \tag{1}$$

where

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}}\right)^{-2} \tag{2}$$

$$V_{Teq} = \mid V_{Tp} \mid - \sqrt{\frac{2I_B}{K_{n2}}} \tag{3}$$

The multiplier using the low voltage low power square-law CMOS cell [9] is illustrated in Figure 2. Four low voltage composite cells are connected to build the multiplier.

The output current of the multiplier is derived by

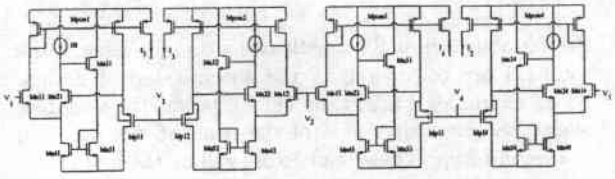

Fig. 2. Multiplier using the low voltage low power square-law CMOS cell

$$\begin{aligned} I_o &= (I_1 + I_4) - (I_2 + I_3) \\ I_o &= K_{eq}(V_1 - V_2)(V_4 - V_3) \end{aligned} \quad (4)$$

where K_{eq} is the equivalent transconductance parameter. Initial simulations were done with MOS transistor level-2 model parameters, using the 2μm MOSIS n-well process. The transfer curve of the multiplier is given in Figure 3 for a bias current of $I_B = 120\mu$A and a supply voltage of 3V. Only the DC analysis results are given since the statistical design of the circuit is done for DC performances only.

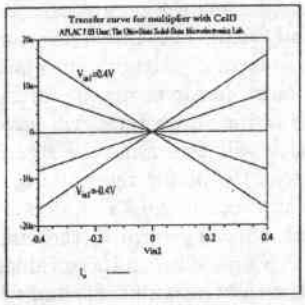

Fig. 3. Transfer curve of the low voltage low power multiplier

3. Statistical VLSI Design Tools

Random variations in integrated circuit processes cause random variations in transistor parameters. Causes of circuit output variance can be divided into two groups [6]: Inter-die device variability and intra-die device variability. Inter-die device variability is characterized by die-to-die, wafer-to-wafer, or lot-to-lot process variability. Inter-die parameter standard deviation is usually much larger than intra-die parameter standard deviation; however, in many analog circuits, it is intra-die parameter variances or device mismatch which cause the greatest deviations in circuit performance. Therefore, a statistical model which comprehends device mismatch is necessary for the statistical analysis of analog circuits. In order to include the random mismatch effects between circuit devices, the statistical model must have a different set of model parameters for each transistor in a circuit. Pelgrom and others [10-13] showed that the variance of the mismatch can be represented by

$$\sigma^2(P) = \frac{a_p}{WL} + {s_p}^2 D^2 \quad (5)$$

where D is the separation distance, WL is the gate area of the transistor, and a_p and s_p are process dependent fitting constants. This model considers two of the greatest effects on device variability of analog circuits: Device size and circuit layout. According to equation (5), the standard deviation of the mismatch is reversely proportional to the area of the transistor, and directly proportional to the square of the separation distance. This equation is a result of Pelgrom's work on measurements that were taken from 2μm and longer channel lengths of transistors, which were fabricated over years. Recent works on the matching issues of submicron channel lengths [14, 15] proves that the 1/WL phenomena changes. Equation (5) is restated such that the variance of the mismatch is reversely proportional to the effective area of transistors, since the effect of the submicron channel length on mismatch becomes a dominant factor. The model calculation procedure for the SMOS model is presented in Figure 4.

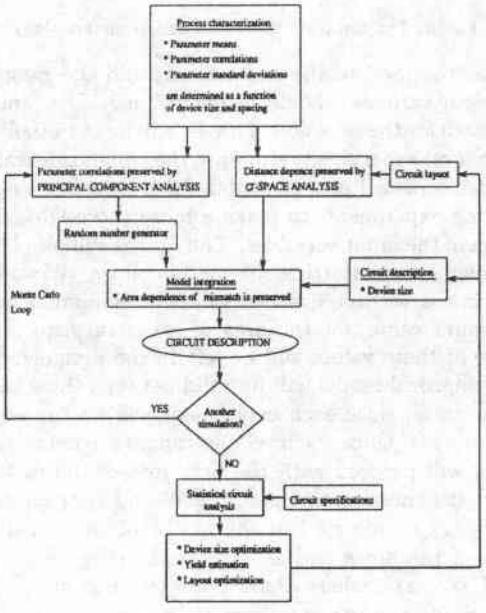

Fig. 4. The model calculation procedure for the SMOS model

The statistical design methodology will help make a robust design, with the aid of statistical techniques, such as DOE [16] and RSM [17]. Both techniques were explained in detail in the previous sections. Figure 5 shows the complete block diagram of the statistical design methodology.

The methodology will be applied once the initial circuit design is complete. Before starting to run the experi-

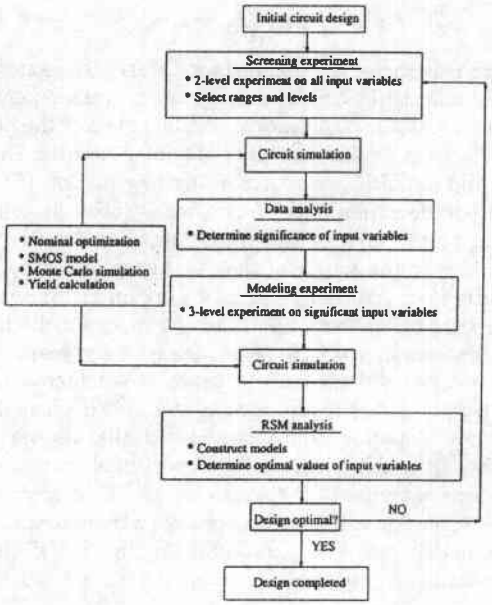

Fig. 5. The complete statistical design methodology

ments, the level of the experiments and the range for the input variables should be determined. The common approach for the selection of levels, will be to initially use a two-level experiment, and once the significant transistors are screened out, to switch for a three-level model building experiment, to make a more thorough examination of the input variables. The ranges will also be determined before starting the methodology. A two-level experiment will require two values; a minimum and a maximum value, for the area of each transistor. The choice of these values will be left to the designer. The final empirical model will be valid between these values of the areas, since each experiment will be run within these ranges. Once the level and ranges are defined, the design will proceed with the first step of the methodology. It is noteworthy, that the W and L of the transistors are represented in the netlist of the circuit, in terms of the areas and aspect ratios, using $W = \sqrt{ab}$ and $L = \sqrt{a/b}$, where a and b are the area and aspect ratio of the transistors, respectively.

The Placket-Burman experiment will be used to screen *out the most contributing transistors. The effect of each* input variable, V_i, is indicated by the sum of squares (SS) as

$$SS(V_i) = \frac{N}{4}[avg(y(V_i = +1) - (y(V_i = -1)))]^2 \quad (6)$$

where -1 and +1 represent the low and high levels, respectively, N is the number of runs, and y is the output performance. Depending on the specified cut off point, the variables whose SS constitutes a certain value of the total SS are considered in the second step of design. As an example; if 5% is the cut off point, the variables whose SS constitutes 95% of the total SS are taken to the second step. These transistors will be the main focal point once they are obtained. The designer will concentrate on optimizing only these transistors, knowing the fact that the remaining transistors are not affecting the circuit performance [16]. The SS values and the contribution of each input variable is calculated with the help of a computer program written in the C programming language. The results of the Placket-Burman screening experiment are applied as the input of the program, and the output is the SS values and hence the contributions of each input variable [16].

The second step of the methodology is a three-level model building experiment, with -1, 0, and +1 representing the three levels of design variables. A Box-Behnken design is suitable for this task, due to its ability to construct a full quadratic model. The results of the Box-Behnken design are analyzed and fitted to a polynomial model using the regression method. The regression method fits the data into a polynomial equation with the least squares algorithm. The equation consists of a constant term, linear terms, quadratic terms, and the interaction terms. Each term will have a "T" (target) value, which will determine the significance of the terms. The rule of thumb for determining the statistical significance is to check if the "T" value is between the values -0.5 and 0.5. Any term in the empirical model which has a "T" value between these values will be considered as statistically insignificant, and will be ignored and excluded from the final empirical formula [16, 17].

The final step of the statistical design process is to plot the relationship between the input variables and the output performance, using RSM. A statistical software tool, Minitab [18], is used for obtaining the response surfaces. The Box-Behnken results are applied to this program in order to construct the empirical model. The fitness of the empirical model is indicated by the regression coefficient, R^2, which explains how good the model is by comparing the overall model and the predicted model. A perfect fit should have R^2=1. Response surfaces will help to visualize the model.

4. The Statistical Design Process

The statistical design of the multiplier [9] will be introduced in this section. Statistical simulations are done for the linearity of the circuit. The nonlinearity coefficient is referred to as α_1 throughout this paper. To measure the nonlinearity of the multiplier, three points are selected from the curve, as illustrated in Figure 6. y_1 and y_2 are written as

$$y_1 = I(V_m) - I(V_m/2) \quad (7)$$

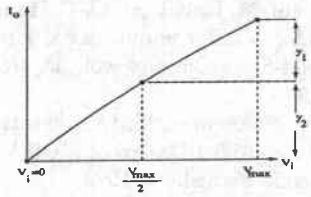

Fig. 6. Representation of nonlinearity

$$y_2 = I(V_m/2) - I(0) \quad (8)$$

The nonlinearity is written with the help of y_1 and y_2 as follows:

$$I_o = \alpha_0 + GV_{in} + \alpha_1 {V_{in}}^2 \quad (9)$$

$$\alpha_1 = \frac{2(y_1 - y_2)}{{V_m}^2} \quad (10)$$

This nonlinearity model will be used in the netlist of the statistical simulations. According to the above mentioned method to determine α_1, the nonlinearity for $V_s = 0.3V$ is calculated from Figure 3 and was found to be -0.0625$\mu A/V^2$ for a transconductance value of 24.8$\mu A/V$.

To apply the statistical model to the cell, layout information must be given. The X-Y coordinates of each transistor which are extracted from the actual layout of the cell is specified in the simulation program [14-17]. If the actual layout does not exist, it is possible to make a good estimation for the placement of transistors in the circuit, and use this information in the netlist. Simulations are done by using APLAC [18].

The statistical design methodology starts by selecting the input variables for the circuit. Seven variables, namely a_{n1}, a_{n2}, a_{pcm}, a_{n3}, a_{n3}, a_{p1}, a_{n45} and a_{pcs} are selected for the circuit and will be applied to the first step of the of the design procedure. a_{n1} represents transistors M_{n11}-M_{n14}, a_{n2} represents transistors M_{n21}-M_{n24}, a_{pcm} represents transistors M_{pcm1}-M_{pcm4}, a_{n3} represents transistors M_{n31}-M_{n34}, a_{p1} represents transistors M_{p11}-M_{p14}, a_{ncs} represents the current source transistors and a_{n45} represents transistors $M_{n(45)1}$-$M_{n(45)2}$. The level and ranges for these input variables should be selected by the designer, as mentioned in Section 3, and is given in Table 1.

TABLE I

Area level and assignments for each transistor in the multiplier

Area sybmol	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	a_{pcs}	a_{n45}
(-1)μm^2	10	200	450	1000	30	450	114
(+1)μm^2	50	1000	2250	5000	150	2250	570

The results of the Placket-Burman screening experiment show that transistors the variables a_{n2}, a_{pcm} and a_{p1} are the most contributing variables for the nonlinearity. These input variables will be considered in the Box-Behnken model building experiment which is the next step of the statistical designm which is the Box-Behnken model building experiment. The results of the Box-Behnken experiments will be used in the statistical tool Minitab [18] to construct the empirical model. The standard deviation of nonlinearity is expressed as the following empirical formula:

$$\begin{aligned} \sigma(\alpha_1) &= 0.4617 + 0.4639a_{n2} - 0.1233a_{pcm} \\ &- 0.04123{a_{p1}}^2 - 0.0232{a_{n2}}^2 \\ &+ 0.0039{a_{pcm}}^2 - 0.0030a_{n2}a_{pcm} \end{aligned} \quad (11)$$

The square term and interaction terms related to a_{p1} are not included in the model since their "T" value is not in the valid range. With $R^2 = 96.9$, the model for nonlinearity is a very accurate one. Figure 7 shows the contour plot for the offset current.

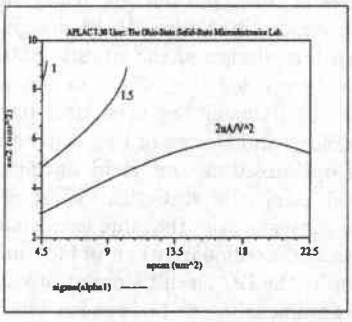

Fig. 7. Contour plots for nonlinearity

It is seen that the offset current and nonlinearity of the multiplier can actually be worse than the results found without considering mismatch effects, e.g., the nonlinearity shows a deviation up to $2\mu A/V^2$, which contradicts with the almost zero nonlinearity coefficient found from the transfer curve. The results of this section prove that statistical design is a crucial step in designing robust multiplier circuits since they depend on device matching to achieve a linearized characteristic. Response surfaces, showing the trade-off between the area and functional yield are provided. The contour curves can be used to keep the offset current and the nonlinearity low by selecting appropriate W and L values for the most contributing input variables.

It is also possible to use the standard deviation information to enhance the yield. Let us assume that the goal of optimization is to obtain the minimum device area while achieving $I_{cm} < 4\%$, with a functional yield of 95%, or equivalently, to achieve the standard deviation of the relative drain current mismatch of 2%. From

Figure 7, the minimum point on the response surface corresponding to 2% is $a_{n2} = 300\mu m^2$, $a_{pcm} = 450\mu m^2$, and $a_{p1} = 30\mu m^2$. From the definition of W and L given in Section 2.2, $(W/L)_{n2} = 122/2.5$, $(W/L)_{pcm} = 150/3$, and $(W/L)_{p1} = 15/2$. Thus, when these aspect ratios are used for the three transistors, the standard deviation will not exceed 2%, and the functional yield will be 95%. The circuit should be fabricated in large numbers to prove these results. However, the whole purpose of making statistical design is to be able to estimate the yield and standard deviation without actually having to fabricate the circuits, in order to reduce the cost. Statistical simulation results will give insight to the designer, and a quantitative measure of how much the standard deviation is going to be.

5. Conclusion

This paper examined the statistical design of a new multiplier circuit using a low voltage square-law CMOS cell. Initial simulations of the circuit were done with MOS transistor level-2 model parameters, using the 2μm MOSIS n-well process. Statistical VLSI design tools were used in the robust design of the circuit. Statistical simulations were made for the offset current and nonlinearity of the circuit using the statistical Response Surface Methodology and Design of Experiment techniques. Device size optimization and yield optimization were demonstrated using the statistical VLSI design tools. The contour curves proved that due to mismatch effects, offset current and nonlinearity can in fact be worse than what the results the DC circuit simulations show. Offset current and nonlinearity can be kept low by selecting appropriate W and L values from the contours which also helps optimizing the functional yield of the circuit.

6. Acknowledgment

Financial support from TÜBITAK (The Scientific and Technical Research Council of Turkey) is gratefully acknowledged.

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