A data driven model of TiO_2 printed memristors

Lucia Valentina Gambuzza[1], Natasa Samardzic[2], Stanisa Dautovic[2], Maria Gabriella Xibilia[3]

Salvatore Graziani[1], Luigi Fortuna[1], Goran Stojanovic[2], Mattia Frasca[1]

[1] Department of Electrical, Electronic and Computer Engineering
University of Catania, Catania, Italy
mattia.frasca@dieei.unict.it
[2] Faculty of Technical Sciences
University of Novi Sad, Novi Sad, Serbia
[3] University of Messina, Messina, Italy

Abstract

After the fabrication of several devices showing memristive switching behavior, recently a growing interest to the realization of dynamical nonlinear circuits based on memristors has been manifested. Currently, many memristor circuits have been mostly conceived on the basis of theoretical memristor models. However, in order to analyze the dynamical behavior of memristor circuits with real components and to implement them, the characteristics of the fabricated devices have to be included in the models used. To this aim, a compact data-driven model is proposed in this paper. The model is based on neural networks and is derived starting from experimental measurements performed on printed TiO_2 memristors.

1. Introduction

Memristors are nonlinear two-terminal electrical elements relating charge and flux. They are at the same time an intrinsically nonlinear element and a memory element, a characteristics which make them a potential candidate to start a new generation of computational circuits substituting transistors. Under this perspective, most efforts are now directed towards the use of memristors to implement high-speed low-power processors and filters [1] and to design non-volatile memories and solid state drives, since memristors can retain memory states, and thus data, in power-off mode, and since they integrate the memory in the same circuitry devoted to memory control, thus resulting in area occupation saving [2, 3, 4]. In the framework of nonlinear dynamics, memristors gained a lot of interest as fundamental blocks for the definition of new nonlinear circuits able to show complex behavior including chaos [5, 6, 7, 8]. Beyond electronics, memristors have also a theoretical importance as models of biological phenomena in simple organisms [9, 10] or human blood properties [11]. Furthermore, memristive properties of synaptic junctions are considered to be at the basis of complex biological mechanisms like the spike-time-dependent plasticity of neural synapses [12].

The existence of memristors was theoretically postulated in 1971 by Leon O. Chua [13] and, only in 2008, experimentally confirmed by the researchers of HP labs who reported on the first memristor device [14]. After the first device based on a TiO_2 thin film produced in the HP labs, several other memristive devices based on the same principle of the TiO_2 memristor have been fabricated with different materials and techniques. Currently, several techniques such as sol-gel spinning [15], sputtering [16], atomic layer deposition [17], electrohydrodynamic inkjet printing [18], have been employed for thin film deposition. Memristive effects with different performance and characteristics have been found by using TiO_2 with different materials for bottom and top electrodes, such as Cu, Ag, Pt, Au or PEO-PANI, and for the active layer such as TaO_x, ZnO, HfO_2, SnO_2 or multiple layers.

For the applications of memristors currently under investigations, the availability of models of the device behaviors and CAD tools is fundamental, since many properties of memristors-based systems, architectures and solutions have to be tuned taking into account the peculiarities of these new devices. Given the variety of techniques and materials employed for their fabrication, the number of models developed is also large. The basic model explaining memristive behavior is the linear drift model [14], which represents the memristor as a series of two resistances, corresponding to the doped and the undoped region and function of their width. The width is a dynamical variable function of the voltage applied to the memristor. The model has been then extended to include nonlinear drift in [19, 20]. However, a fully detailed description of the physical effects that control memristor switching requires more complex models including the types of transport and dynamics occurring in the device. To this aim the development of physics based models is currently investigated (see for instance [21]).

Starting from an analysis of a real device fabricated within the framework of the European Project APOSTILLE, we propose a neural networks based model able to reproduce the $i-v$ characteristics experimentally observed. The model is constructed starting from an experimental campaign of measurements and using the data to train a neural network. In this paper, we discuss the methodology which allows to obtain a simple data-driven model which is therefore independent of the fabrication technology. Furthermore, we have observed a significant variability of the device response which may be due to the technology used for memristor fabrication, still at an early stage,

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and that our neural networks based model is able to capture.

The rest of the paper is organized as follows. Device fabrication and electrical characterization are discussed in Section 2. The neural networks based model is presented in Section 3. In Section 4 the conclusions of the paper are drawn.

2. Device fabrication and electrical characterization

The memristors analyzed in this paper have been fabricated within the framework of the FP7 APOSTILLE project. The memristors consists of three layers as shown in Fig. 1: a substrate (ITO glass), an active layer (thin TiO_2 film) and a top silver electrode. Memristors have been fabricated using Fujifilm Dimatix DMP 3000 ink-jet printer on commercial Indium tin oxide coated glass substrate (703184 Sigma-Aldrich) with surface resistivity of 30-60 Ω/sq. As active layer TiO_2 ink is used, synthesized at LTP/EPFL labs. The layer was deposited with printing frequency of $1kHz$, piezoelement actuation amplitude of $26V$ and drop spacing resolution of $20\mu m$, at room temperature. Reduced layer containing oxygen vacancies was created by heating TiO_2 layer in nitrogen atmosphere for 6h with maximum temperature of $200°C$. Afterwards top Ag electrode (SunTronic U5603 ink) was printed with $25\mu m$ drop spacing resolution and platen temperature of $60°C$ in order to avoid unwanted spreading of silver layer and sintered for 45min at $200°C$ for degradation of organic coating over silver nanoparticles. A detailed discussion on the device fabrication and physical characterization is reported in [22]. The electrical characterization of the device is here briefly described.

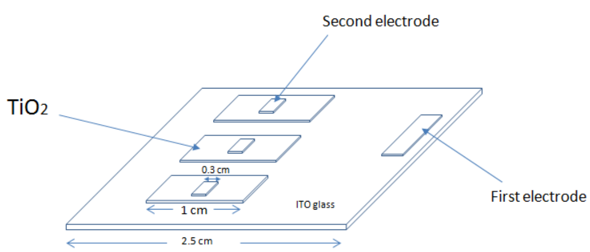


Figure 1. Scheme of the TiO_2 printed memristor.

The device was tested by using a Keithley 2602 programmable sourcemeter. Measurements were performed by applying a voltage sweep from $-9.5V$ to $9.5V$, and viceversa, with step size of $0.2V$ and a settling time equal to $0.1s$ to the terminals of the device, and recording the current through the device. After that, the $i-v$ curve is plotted. The method allows to recover the main feature of the memristive behavior, that is, an hysteresis pinched loop in the $i-v$ plane.

Fig. 2 reports three hysteresis cycles, obtained at different times but under the same nominal working conditions. Despite the qualitatively similar behavior, the area of the hysteresis is different in the three cases and in one of them a large peak in the response is observed. The tests have been repeated several times (up to 20-30 different trials) on the same device and on different devices. The same behavior has been found for all the trials and devices tested. We also note that peaks in the response of memristors have been recorded in other independent experiments [23].

We have first compared the results of our experimental characterization with a model fit based on the nonlinear drift model proposed in [14], including different window functions [19, 20], but we have found that these models do not accurately describe the $i-v$ characteristics of our memristor, and, in particular, the great variability of the experimental behavior under nominally identical conditions. For this reason, we have developed a simple data-driven model based on neural networks.

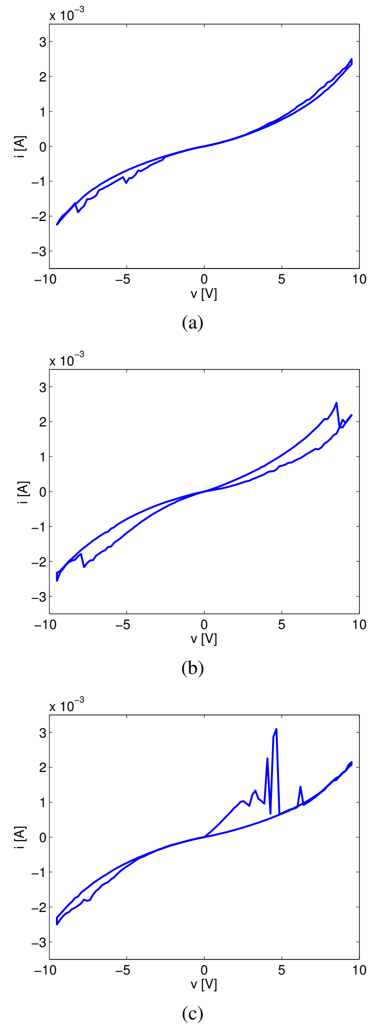
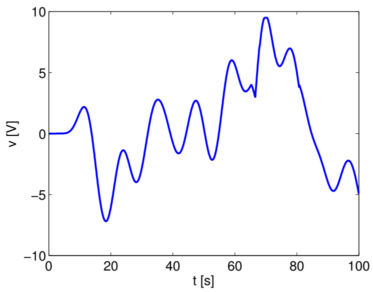


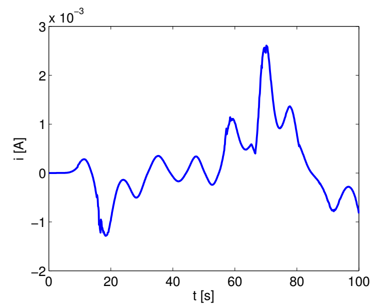
Figure 2. Experimental results. Three different pinched hysteresis loops under nominally equal initial conditions are shown in (a), (b) and (c).

3. The neural network model

Due to the characteristics of the memristors, the most appropriate assumption for the model is to consider a NARMAX (nonlinear autoregressive moving average with exogenous inputs) model. Considering the applied voltage on the memristor as the input, $u(t) \in \mathscr{R}$, and the current as the output, $y(t) \in \mathscr{R}$, and indicating as n the system order, the NARMAX model is described by:



(a)



(b)

Figure 3. Data used for training: (a) input (waveform of the voltage applied to the memristor); (b) output (waveform of the memristor current).

$$y(t_k) = f(y(t_{k-1}),...,y(t_{k-n}),u(t_k),...,u(t_{k-n})) \quad (1)$$

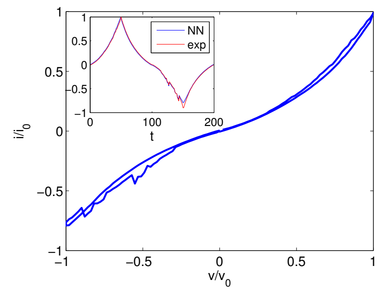
where $t_k - t_{k-1} = \Delta T$ is the sampling time. The NARMAX model considered here is based on one hidden layer multilayer perceptron trained by using the Levenberg-Marquardt algorithm with early stopping strategy to avoid overlearning [24].

The first phase in model derivation dealt with the acquisition of the appropriate measures for learning and validating the model. We run a campaign of measurements devoted to acquire the answer of the memristor to the input waveform shown in Fig. 3(a). The response of the memristor to this waveform is also shown in Fig. 3(b). Additional data (used for validation) are the hysteresis pinched loops reported in Fig. 2. All data used for model derivation have been normalized to be in the range of $[-1,1]$.

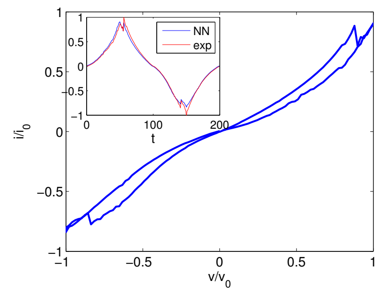
The data have been divided into data for learning, for test and for validation. The data reported in Fig. 3 have been used for the training phase (70% for learning, 15% for testing and 15% for validation). Data have been first shuffled so that their order is randomized.

Based on the a priori knowledge on the memristor dynamics and previously reported models, the system order was fixed as $n = 1$, while the number of units in the hidden layer was determined by using a trial and error strategy. After this, a structure with 5 hidden neurons has been selected as the one showing the best results.

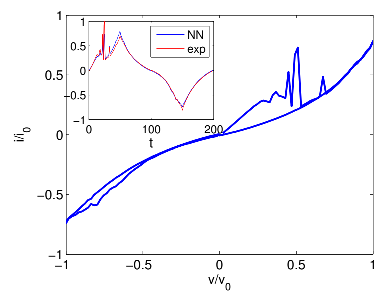
After training, a further validation was carried out on the set of data, most significant from the point of view of memristor analysis, that is, the series of pinched hysteresis loops of Fig. 2(a)-2(c). The main results of this validation step are shown



(a)



(b)



(c)

Figure 4. Pinched hysteresis loop obtained by the neural networks based model.

in Fig. 4, which demonstrates how the obtained neural network is able to reproduce the variability in the hysteresis loop of the device. In particular, the neural network based model is able to fit the hysteresis loops in Fig. 4(a)-4(c) which correspond to the experimental data reported in Fig. 2(a)-2(c). This shows how the variability can be explained by taking into account the different initial condition of the memristor internal state.

4. Conclusions

In this paper we have proposed an empirical, compact model for TiO_2 printed memristors. The memristors, fully realized with printing technology, were first characterized from an electrical point of view. In particular, they showed pinched hysteresis loops with a certain degree of variability under the same nominal working conditions. In order to use the memristors fabricated in this way in real applications (such as nonlinear circuits), the availability of a model based on the real characteristics of the device is fundamental. Since physics based models take into account technologies and materials used and require a perfect knowledge and control of the fabrication process parameters, we have chosen to develop a compact model. The model has the further advantage of being data driven and to be derived in short time. The methodology can then be used for a fast characterization of memristors produced with other techniques or materials. The model developed is able to explain the observed variability in the pinched hysteresis loop as an effect of the initial condition of the model.

5. References

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