HIGH-PERFORMANCE FUZZY PROCESSING MEMORY UNIT FOR HYBRID-MODE FUZZY LOGIC CONTROLLERS

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Abstract – High-performance Fuzzy Memory and Maximum Circuit (FMMC) is designed and simulated. In addition to simplicity of this circuit hardware, simulation results show that a FMMC hardware has high-performance processing speed. Also, this circuit can be easily controlled with standart microcontrollers. Therefore, we offer this circuit for hybrid-mode fuzzy controllers.

I. INTRODUCTION

Fuzzy sets and theory presented by L. A. Zadeh in 1965 is an excellent concept representing human thinking and reasoning. Fuzzy logic has been applied to practical uses in control, medical diagnosis, pattern recognition, and many other fields, employing popularized digital computer.

Although a digital computer system is very useful because of its programmability, it is not so effective with respect to the speed of processing, power dissipation, the functional density, the design and fabrication cost and so on. Fuzzy reasoning with hundreds of fuzzy implications in that manner is not easy to accomplish in the real time mode processing. Therefore, fuzzy information processing requires exclusive hardware systems that deal with fuzzy signals but not binary. For the design of systems, either a special digital circuit structure in very large scale integration (VLSI) (for example, [1]-[2]) or a general-purpose microcontroller is used [3]. The all digital methods are suitable for procesing fuzzy information in (converted) digital form. However, in many application, inputs come from sensors are in analog form and outputs must also be analog in order to drive actuators. Therefore, in application where such input and output analog signals are produced by using a large number A/D and D/A converters. This will increase chip size and power dissipation. To achive this problem, a hybrid-mode VLSI circuits can be used [4]-[5]. In this study, digital signals are used for programming and control, but all processing maintains the analog signals in their original form.

The fuzzy hardware systems can be realized two methods for fuzzy information processing. One method is to digitize the input signal and to process the information in digital mode throughout the system. The another method is to design fuzzy logic controller that composed of intrinsic fuzzy logic circuits. The expections of a fuzzy logic controller's hardware system are summarized following matters.

- *Simple circuit configuration*
- *Low cost*
- *High-speed processing*
- *Providing unimportant errors for high-speed processing*
- *Adjustable fuzzy term definition for each input and output*
- *Producing on a chip.*

This paper is organized as follow: in Section II, the proposed a fuzzy logic controller's hardware system will be introduced. In Section III, Fuzzy Memory and Maximum Circuit (FMMC), a part of the proposed fuzzy hardware system, will be described in detail. This FMMC unit is focus of our study developed by us. The simulation results of FMMC are presented in Section IV. Finally, discussions and conclusions of our study are given in Section V.

II. FUZZY HARDWARE SYSTEM

In this study, fuzzy memory unit of hybrid-mode fuzzy controller hardware system employing intrinsic fuzzy logic circuits is described. The fuzzy hardware system is designed to achieve the following fuzzy inference.

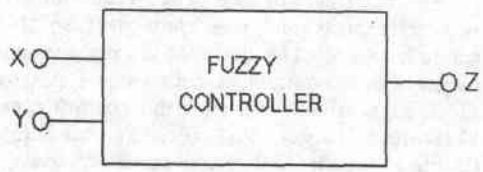

Fig 1. Description of proposed fuzzy controller block

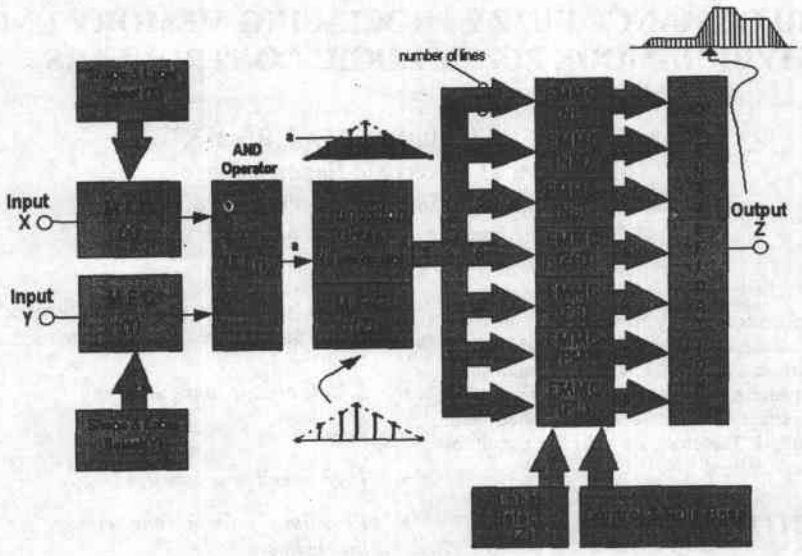

Fig 2. The block diagram of fuzzy hardware system.

(Control Rule I) If x is X_1 AND y is Y_1, THEN z is Z_1

ALSO

(Control Rule II) If x is X_2 AND y is Y_2, THEN z is Z_2

ALSO

(Control Rule III) If x is X_3 AND y is Y_3, THEN z is Z_3

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ALSO - - - - -

(Control Rule N) If x is X_N AND y is Y_N, THEN z is Z_N

(Premise) ***x is X' AND y is Y'***

(Conclusion) z is Z'

Each control rule in the ruleboard contains two antecedents and one consequent so that the controller accepts two deterministic input signals and produces one deterministic output signal as shown in Fig 1. Eight labels are used in this controller, namely PL(Positive Large), PM (Positive Medium), PS (Positive Small), ZR (Approximately Zero), NS (Negative Small), NM (Negative Medium), NL (Negative Large).

The architecture of the fuzzy controller hardware system is shown in Fig 2. Non-fuzzy input signals X, Y are applied to rule board in voltage mode.

A. Minimum and Maximum Circuits

The basic fuzzy logic units in the fuzzy hardware system are Min and Max circuits. The response times of these circuits are within 20 ns for the constructed with discrete transistors. These circuits are called *emitter coupled fuzzy logic gates*. The emitter coupled fuzzy logic gates are highly robust against the supply voltage fluctuations. They operates normally even if $+V_{CC}$ changes +6 V ~ +51 V, and $-V_{EE}$ within –1 V ~ -46 V, while conventional binary system in voltage mode, e.g. TTL, are guaranteed within +4.5 V ~ +5.5 V of supply voltage at most. Furthermore, they exhibit a good thermal characteristic. Their output error caused by the change of ambient temperature -55^0C ~ $+125\ ^0$C is less than 0.8 %F.S. and thus the error is not problem the fuzzy hardware systems [6].

B. Membership Function Generator (MFG)

A membership function of a consequent is sampled to discrete grades, which are represented by voltage ranging 0-5 V and distributed on 5 signal lines (it can be increased for more precision and sensititivity) as shown Fig. 2. This MFG has discrete a triangle form which consist of five voltage values. This generator defines label of output variable of the controller (z).

C. Truncation Gates

A truncation gate accepts one fuzzy vector signal from MFG. Value of "a" is ranged from 0 V to

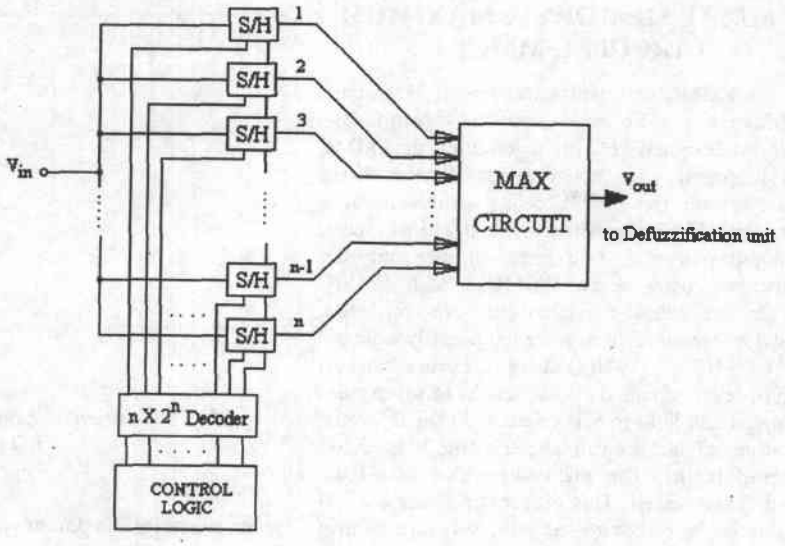

Fig 3. A Fuzzy Memory & Maximum Circuit Cell

5 V. The fuzzy vector represents a membership function of consequent and is delivered from the MFG. "a" represents the degree of matching between the fact and the antecedent, and is delivered from the Min (1) circuit. The truncation gate produces a fuzzy vector signal truncated by the fuzzy scalar input signal as shown Fig. 2. In other words, the truncation gate accepts a 5-element input data and one analog input. Corresponding to the inputs, a 5-element output data is produced. The voltage distribution of output data is truncated according to the analog input level. This can be constructed by arranging MIN circuits in an array. Each element of the array is compared with value of "a" by MIN circuits with two inputs. Finally, one vector array is produced as a output array. This array is a consequent vector fuzzy inference engine.

D. Membership Function Circuit (MFC)

The block diagram of MFC is shown in Fig. 2. The input of MFC (V_{in}) is voltage-mode. Digitally controlled with analog switches shape select terminals define shape of membership function. Label select terminals define labels of membership function (i.e. PM, ZR, NS, NL etc.). Our simulation results show that this MFC can realize standart four function of a triangle, trapezoidal, S-shape, and Z-shape. The label selection of MFC is provided by label select circuit. With this circuit the center voltage of membership function can be adjusted. This center voltage is ranged –5 V; +5 V and distributed on seven signal points[7].

E. Defuzzification Unit

The procedure to obtain a deterministic value, on the universe of discourse, from a fuzzy value is called *defuzzification* and its tool a *defuzzifier*. The most popular way of defuzzification is a center-of-gravity method (c.o.g.), or a centroid method [8], [9]. In this study, we used center-of-gravity method as defuzzification method.

A membership function is often represented by a set of elements on the universe of discourse as well as continuous one as shown in Fig. 2. The center-of-gravity can be calculated from the following equation depending upon discrete form.

$$C.O.G = \frac{\sum_{i=1}^{n} i\mu_i}{\sum_{i=1}^{n} \mu_i} \qquad (1)$$

where n represents the number of elements of the sampled membership funtion (n=35 in this study) and μ_i is the grade of *i*th element.

Basically, the FLC composed of two sections.The first one is a *fuzzy inference engine* which achieves an individual fuzzy inference and second one is a *defuzzifier* which aggregates all the individual conclusions and derives a center of gravity of the membership function of final conclusion[4].

III. FUZZY MEMORY & MAXIMUM CIRCUIT (FMMC)

A FMMC cell, which has seven S/H circuits and a Max circuit with seven inputs, is shown in Fig. 3. Since we designed FLC for seven rules, the FMMC cell is proposed with seven inputs. In this fuzzy hardware system, five FMMC cells constitute a Fuzzy Memory and Maximum Circuit. Each FMMC has a input/output pair with five lines. In the controller structure, we used seven FMMCs. Each FMMC represents one output (z) label (PL, NS, NL etc.). Fuzzified information signals are temporarily storaged in S/H(1), S/H(2), ..., S/H(7) along rule processing. At the end of seven storaged cycles, results of seven rules are sampled and hold in S/H circuits. At the 8th cycle, all the storaged data are inferenced by the Max circuit with seven inputs. The maximum value of all the storaged data is taken. This proccess realized by S/H circuits is digitally controlled with software control algorithm. Switching speed of this circuits is greater than 10 MHz frequency. Because of this switching feature, a FMMC can be controlled easily with standart microcontrollers. Timing waveforms used for this purpose are shown Fig. 4. In this figure, the each rule has been sampled and hold at a certain interval of time. This sampled and hold data are memorized during all rule processing. After all rules processing, all obtained data are used altogether (in parallel form) for fuzzy inference engine. The data from FMMCs are send to defuzzification unit for converting real-value data.

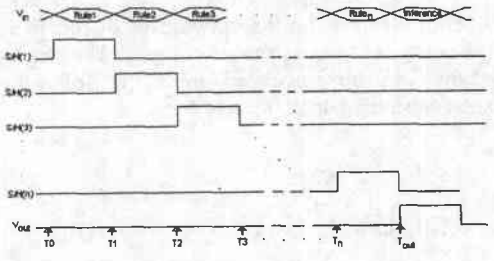

Fig. 4. Control timing waveforms of FMMC

IV. SIMULATION RESULTS

The FMMC has been simulated for seven rules. In simulations, the FMMC input value from rules were selected for the worst-case. The worst-case is that the maximum value of FMMC inputs is placed in first cycle (0-1μs). Each processing time of rule was selected as 1μs. Although the selected case is the worst case, as shown in Fig. 5at the end of the 7 μs processing time for

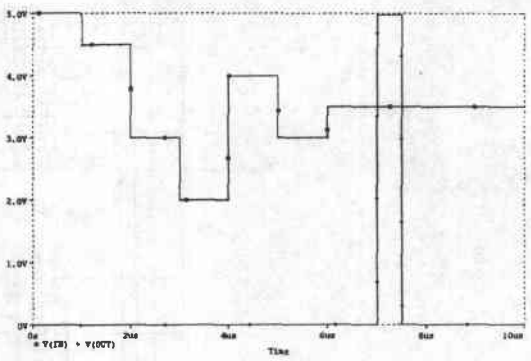

Fig. 5. The transient response of FMMC for seven rules

seven rules, the maximum value of all the memorized data is selected and precisely transferred defuzzification (output) stage. Maximum value is represented as V_{out}. In the worst case, decreasing maximum value is approximately which is % 0.4 insignificant from simulation result.

V. CONCLUSION

A new Fuzzy Memory and Maximum Circuit (FMMC) has been proposed and behaviours of this circuit were simulated with SPICE programme. This circuit realizes all rule processing on only a rule board instead of using a rule board for a rule processing. Because of this feature this FMMC configuration has a simplicity hardware structure. This is important advantage for implementation of fuzzy logic controller hardware systems. In addition to simplicity hardware structure, this configuration has high-performance fuzzy processing speed. Altough all rules are processed in a rule board as serial, processing speed is high compared with in several studies in literature [10]. Since this FMMC configuration has the feature referred above, this circuit structure is very suitable for hybrid-mode fuzzy controllers.

VI. REFERENCES

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