Basic Circuits for Multi-Valued Sequential Logic

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Abstract

Multi-valued logic circuits have been offered as a solution to general interconnection and chip area problem. It has the potential of reducing the number of active elements and interconnection lines. More data may be transferred trough a single wire using logic signals having more than two levels. This technology leads to a decrease in number of interconnections and resistance and capacitance of contacts and interconnections. However, in spite of their potential advantages, developments in multi-valued systems are not satisfactory. In particular, it is very difficult to find circuits to implement the multilevel sequential circuits.
In this paper we present a new latch and restoration circuit which improves the performance of the previously designed flip-flop circuit. The flip-flop is the basic building block of multilevel sequential circuits and may be used to design sequential circuits such as multilevel counter/dividers and other sequential circuits.

1. Introduction

Flip-flops are well known sequential circuits and can be realized using multiple-valued logic circuits. Characteristic equations and next-state tables of the multi-valued conventional flip-flops such as RS and JK are defined by [1,2]. Studies about implementation of these flip-flops can be found in the literature but they are very limited and complicated [3,4]. In addition, while calculating the next-state output, these conventional flip-flops use input values, current state output and inverse of current state output. In current-mode multi-valued circuits, inversion operation is performed by subtracting the input signal from $(r-1)*I_b$, where r is the radix (number of logic levels) and I_b is the reference current level. (Other logic levels are determined as integer multiples of the reference current. In this study, we use 4-level logic with the 5μA reference current level). The inversion operation should be avoided, because it increases the power consumption of the circuit considerably.

2. AB flip-flop

As a solution to the inversion operation of the conventional flip-flops, we propose a new flip-flop structure named as AB flip-flop due to its A and B inputs and its next-state equation is defined as follows [9];

$$Q_{n+1}=A+B.Q_n \quad (1)$$

The state transition table of the AB flip-flop is given in Table 1 and it is clear that the flip-flop can successfully change its state from one to other for any input combination.

Table 1. Transition table of the AB flip-flop

Q_n \ AB	00	01	02	03	10	11	12	13	20	21	22	23	30	31	32	33
0	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
1	0	1	1	1	1	1	1	1	2	2	2	2	3	3	3	3
2	0	1	2	2	1	1	2	2	2	2	2	2	3	3	3	3
3	0	1	2	3	1	1	2	3	2	2	2	3	3	3	3	3

Block diagram of the AB flip flop is introduced in Figure 1. It is composed of a *MIN* circuit to perform AND operation, a *MAX* circuit to perform OR operation and a *LATCH* circuit to HOLD the current state.

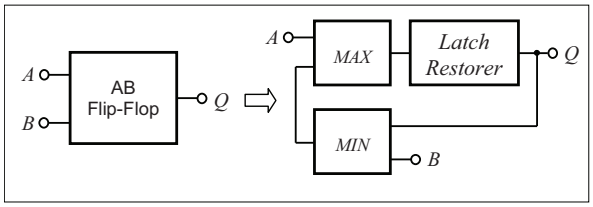

Fig. 1. AB flip-flop

The MIN [5] and MAX [6] circuits are current-mode, multi-input circuits working based on winner/loser-takes-all principle. The LATCH/RESTORER circuit is based on level restoration circuit design given in [7] and optimized for the new application to obtain smooth transitions. The main drawback of current-mode multi-valued logic circuits is that they are not self restored unlike the binary logic circuits. The predefined current levels can be deviate from their original values due to some variations in active element dimensions, power supplies, technology parameters, etc. This variations on the output signal is carried to the next stages. It can be tolerated and output can be detected correctly for a range of value that is called noise margin i.e., $\pm I_b/2$. The signal must be restored to its original value before it exceeds this value. In addition, the flip-flop circuits have positive feedback in nature, which prohibits any variation from

the predefined level. Otherwise this variation forces the output to shift either to ground or power supply voltage. The restoration circuit is modified as LATCH/RESTORER circuit by adding a pass transistor properly. Both HOLD and restore operations performed at the same time by using the circuit given in Figure 2.

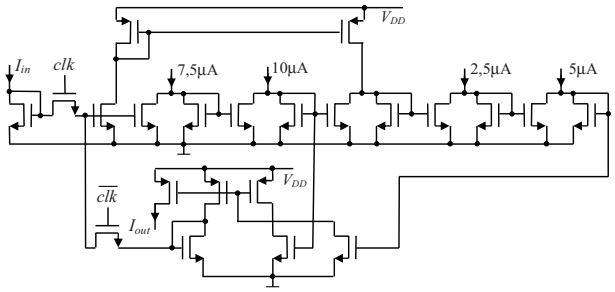

Fig. 2. Modified latch and restoration circuit

Timing of the flip flop circuit is performed by using opposite phase clock signals (*clk*, $\overline{clk}$) stimulating the pass transistor of the latch circuit. The number of *Q* outputs (I_{out}) can be increased by adding more current mirrors to the final stage. Applied input signals and the resulting simulation output are given in Figure 3 and Figure 4 respectively and it is fully compatible with Table 1.

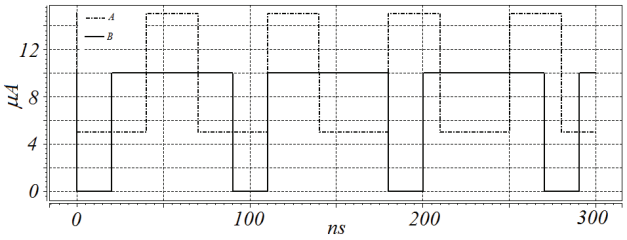

Fig. 3. *A* and *B* input signals of the flip-flop

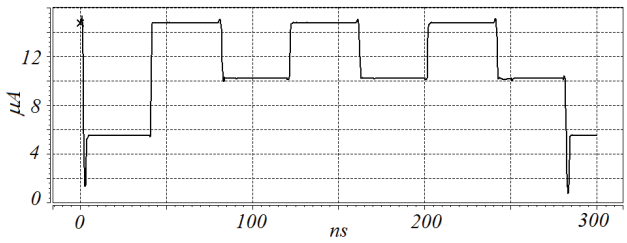

Fig. 4. The *Q* output signal of the flip-flop

3. AB flip-flop Applications

In order to show the usefulness of the proposed AB flip-flop, 2-digit modulo-16 counter is designed. It is supposed to be count as given in Figure5.

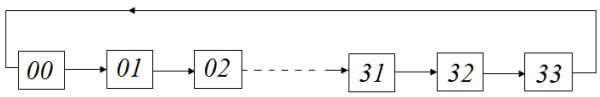

Fig. 5. Counting diagram for 2-digit modulo-16 counter

Using this counting diagram and state transition table of the flip-flop, we can obtain the next-state equation of the counter as follows, after necessary minimizations;

$$A_1 = Q_1^{\to 1},\ B_1 = 0$$
$$A_2 = {}^{3}Q_1^{3} \cdot Q_2^{\to 1},\ B_2 = {}^{0}Q_1^{2} Q_2 \qquad (2)$$

Here, $Q_1^{\to 1}$ and $Q_2^{\to 1}$ indicate 1-level clock-wise cyclic operation [8] and ${}^{3}Q_1^{3}$ and ${}^{0}Q_1^{2}$ are literal operations. The ${}^{3}Q_1^{3}$ operation is logically equal to 'detect if $Q_1 \geq 3$ ', and the ${}^{0}Q_1^{2}$ operation is logically equal to 'detect if $Q_1 \leq 2$ '. So, we can replace the literal circuits with upper and lower threshold circuits, respectively. Threshold circuits are simpler and use fewer transistors than literal circuits. The complete block diagram of the synchronous 2-digit modulo-16 counter and simulation results are given in Figures 6 and 7, respectively.

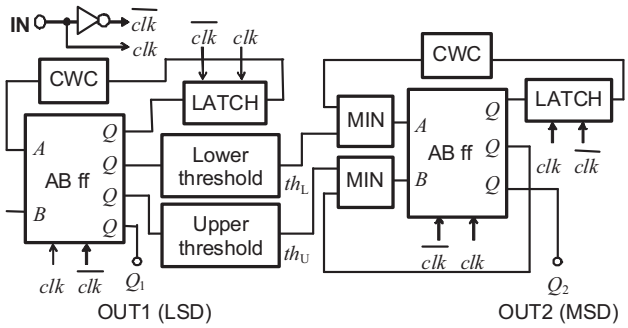

Fig. 6. Synchronous 2-digit modulo-16 counter

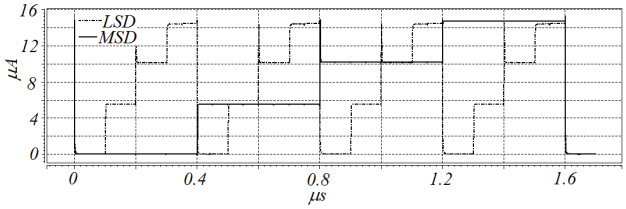

Fig. 7. Simulation result of 2-digit modulo-16 counter

4. Conclusions

In this study, a new current-mode multi-valued sequential flip-flop circuit and its application to a synchronous 2-digit modulo-16 up counter is presented. Proposed flip-flop performs its operation successfully. With minor modifications, radix of the circuit can be increased. Multi-valued logic design is still an open area, especially the sequential design part. This study is just a step to that open area and needs improvement in circuit level and extended system level design.

5. References

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