Multistandard Transceivers: State of the Art and a New Versatile Implementation for Fully Active Frequency Agile Filters

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***Abstract*—The various architectures of transceivers for current standards are firstly compared. Different possibilities to achieve multi-standard transceivers are also recalled and compared. We demonstrate that ease of realization and flexibility evolve in opposite directions. The advantages and drawbacks of reconfigurable active filters are indicated. We demonstrate that the second generation current controlled conveyor operating in current mode is perfectly suitable for the realization of frequency-agile filters. After a brief recall of the essential points of agile filters, a second order frequency agile bandpass filter operating in current mode is implemented with CCCII+. It has four central frequencies whose values could be selected digitally. The validation results show that its tuning ratio $n = f_{0max}/f_{0min}$ is equal to 5.1 with f_{0max} = 1.22GHz.**

I. Introduction

Since many years, telecommunications play more and more important role in contemporary societies, both on the economical and technological development levels. The explosion of applications in areas such as voice, data transmission and multimedia has therefore contributed to different corresponding standards, [1-4]. Firstly, the handling of each standard was achieved by a specific tool, which gave rise to a great number of devices. Each receiver enables the processing of a unique transmission frequency that belongs to a given standard and the architectures were designed in order to receive a given frequency band corresponding to a predefined application, [1,2].
Thanks to its high reliability, Superheterodyne architecture was firstly used. This architecture was then optimized for better signal processing. It is shown on figure 1, [1]

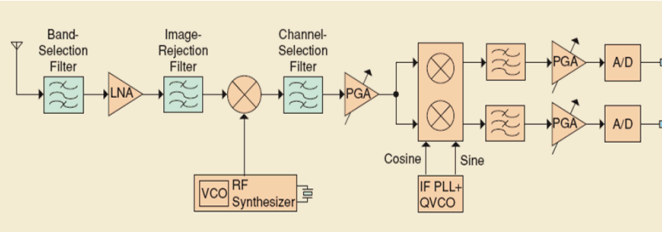


Fig. 1: Superheterodyne receiver architecture, [1].

The trend has now reversed and transceivers should currently be able to handle many standards simultaneously.
In this paper, after a comparison between the receiver architectures of existing standards, we summarize the possible solutions for multi-standard transceiver and we point out that flexibility and ease of integration are not compatible. Then we will draw up the state of the art for reconfigurable active filters that are used in multi-standard transceiver and we compare them. We will show that the second generation current controlled conveyor (CCCII) is perfectly suitable for the realization of frequency agile filters. For this, we will briefly recall the theory and the basic properties of agile filters before we present the design of a second order, fully active, band-pass filter based on CCCII+. The proposed filter has four center frequencies that could be selected by switches. We will give simulation results that allow validation of our approach.

II. Receiver Architectures

Five architectures (i.e. Superheterodyne, Image-reject, "Zero-IF", "Low-IF" and Subsampling) are currently used for the implementation of radicommunication receivers in different standards. All these architectures make use of external band-pass filters. Due to their large size they cannot be integrated into silicon. The choice of the appropriate architecture for each standard is based on many criterions (i. e. cost, ease of integration, Silicon area, etc.). Nevertheless many configurations always coexist in each standard, [1]. Table I indicates the advantages and drawbacks of each architecture; it also shows that the choice of the architecture is not easy as this is after all based on many criterions already chosen [1-3].

Table I: Advantages And Drawbacks Of The Various Architectures.

Receiver architecture	Advantages	Drawbacks
Superheterodyne	Sensitivity and high selectivity. No DC offset Low 1/f noise	More complex architecture High fabrication cost High consumption Needs external components Requires image reject filters
Image reject	Easier integration Low cost No DC offset Low 1/f noise	I and Q must have perfect phase quadrature
"Zero-IF"	Simple architecture Easier integration Low cost No image reject filters	Requires highly linear oscillators and LNAs DC offset I and Q must have perfect phase quadrature High 1/ f noise
"Low-IF"	Simple architecture Easier integration Low cost Low DC offset Low 1/f noise	Requires image reject filters Requires two quadrature phase conversions
Subsampling	Simpler architecture	High noise from sampling Rarely used

Table II indicates the architectures that are mostly found in literature for each of the principal telecommunication standards. The “Zero-IF” and “Low-IF” architectures are however the most used, certainly

because of their low cost. Generally "Low-IF" is widely used for narrowband standards (Bluetooth, HomeRF, …) while "Zero-IF" is widely used for large band standards (UWB, HiperLAN, …) and less for narrowband ones (WiFi 802.11 a/b/g).

TABLE II : THE DIFFERENT ENCOUNTERED ARCHITECTURES IN THE VARIOUS STANDARDS.

		Super-heterodyne	Image reject	"Zero-IF"	"Low-IF"
Mobile Phone	GSM(0,9G)	●		●	●
	DCS(1,8G)	●		●	●
	PCS	●		●	●
	WCDMA(3G)		●	●	
WLAN	HyperLAN 2			●	
	802.11a/g			●	●
	UWB (802.15.3)			●	
WPAN	Bluetooth				●
	HomeRF				●
	ZigBee (802.15.4)				●

For these architectures, the current trend is to use a unique, multi-standard receiver; the latter should be able to deal with many bands simultaneously [4-6].

III. MULTISTANDARD TRANSCEIVERS

A multichannel transceiver has the possibility of receiving several standards simultaneously by using an architecture whose parameters can be modified in order to be able to adapt to the specifications of each standard. That receiver that allows the reception of several standards is of great interest because it will lead to important savings: reduction of size, price, complexity, consumption, etc. However, such a receiver is more complex to implement than traditional ones. The following architectures can be used to implement multistandard transceivers.

3.1 Receiver with elements in parallel

The receiver, shown in figure 2, is obtained by placing in parallel several elements which correspond to the various standards, [5]. The choice of the elements appropriate to the reception of the selected standard is then carried out using switches. The disadvantage of this solution lies in the high number of elements that it requires, thereby increasing size, cost and consumption.

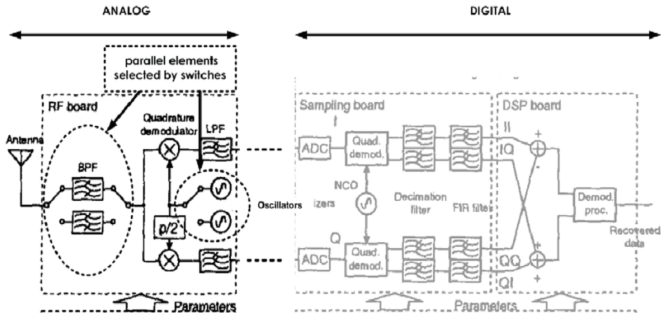


Fig. 2: Example of a multichannel receiver with elements in parallel, [5].

3.2. Receiver with reconfigurable elements

The sharing of certain blocks in the receiver chain makes it possible to reduce the size of the circuit and its consumption by using reconfigurable elements. Two reception architectures using reconfigurable elements currently coexist: architecture with direct conversion to "Zero IF" which includes reconfigurable wideband elements and superheterodyne architecture with "digital IF" which includes reconfigurable narrow band elements.

Homodyne Architecture or "Zero IF" with wideband reconfigurable elements is shown on figure 3, [5]. The receiver is deduced from the classical "Zero IF" architecture, to which additional baseband processing is added: sampling circuits, decimation filters and amplifiers with programmed gain. The analog part includes a wideband LNA and low pass filters.

The superheterodyne receiver with "digital IF" and reconfigurable narrow band elements is presented in figure 4, [6]. This architecture is identical to a traditional superheterodyne architecture. The digitization of the signals is carried out at the intermediate frequency. ADC at these frequencies (for example with IF = 70 MHz) are currently available, [7]. The LNA is a broadband amplifier, [8]. Only the band pass filters are reconfigurable here because their narrow band of transmission of the signal can be moved, [6].

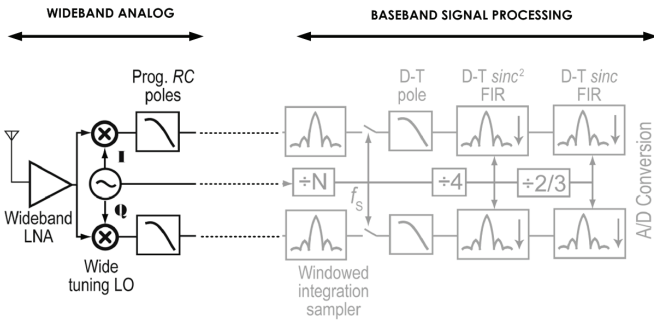


Fig. 3: Example of "zero IF" architecture with wideband reconfigurable elements

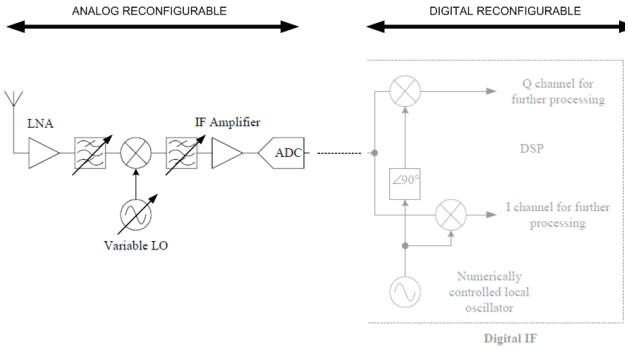


Fig. 4: Super-heterodyne structure with "digital IF" and reconfigurable narrowband elements.

3.3 Mitola's Transceiver

For J. Mitola, [4], the best way to implement a multistandard transceiver consists in first of all digitizing the totality of the spectrum received by the antenna. The signal is then processed: digital filtering of the frequency and the desired channel, then demodulated and possibly decoded. This nevertheless would require a very powerful digital processor. Indeed, a transceiver which would work for all current telecommunications standards should cover the frequency range: 800MHz - 6GHz, [5]. In order to digitize the signal while respecting the theorem of sampling of Shannon, it would then be necessary to have a converter ADC of 12 bits functioning for a rate of 12GS/s (Gsymbols/second), [5]. These performances are well beyond the current state of the art of the converters. Current technologies thus limit the use of this approach to the UHF band (30-300 MHz, [5]).

3.4. Conclusions

As shown, various practical approaches allow the realization of multistandard transceivers: elements in parallel or reconfigurable

elements. The configuration of the receiver is currently carried out in the digital domain and at low frequency in the analog domain. Digital signal processing allows a great flexibility of the receiver reconfiguration. Operations such as filtering and demodulation are easier to carry out in the digital domain (using a DSP for example). However, to fully benefit from the DSP, it is desirable that this treatment is carried out at higher frequencies as close to the antenna as possible. Figure 5 shows the evolution of wireless receivers, from inflexible but easily realizable architectures to entirely flexible but not easily realizable architectures (such as for example that of Mitola), [1, 10]. Current research concentrates on the receivers for which the digitalization of the signal is after RF reception elements, which constitutes a trade-off between two extreme architectures of figure 5. Such architectures require reconfigurable analog elements: LNA, local oscillators, mixing and filters. Reconfigurable LNA and local oscillators currently exist. As example, broadband LNA, [8], makes it possible to replace easily several narrowband LNAs, tunable wideband frequency synthesizers were implemented, [9]. However, the implementation of integrated and easily reconfigurable RF filters over a wide frequency range remains a more delicate task.

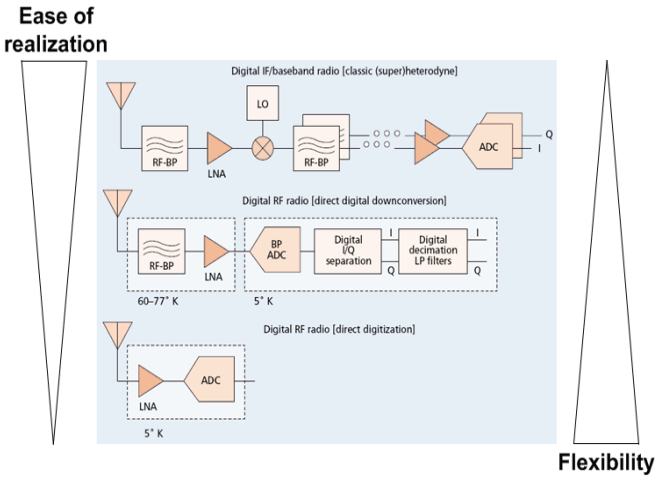


Fig. 5: flexibility versus the ease of realization of various architectures of multichannel reception, [10].

IV. Reconfigurable Active Filters

4.1. Generalities

Reconfigurable active filters are those which up to 2.5 GHz present a greater ease of center frequency tuning. They are also completely integrated on current silicon technologies and require for their realization only small silicon surfaces. Some of them include passive inductors. Thus, we call them partially active filters. The others, where the inductor is generally simulated from active components (and so do not include passive inductors) will be called purely active. Note that dimensions of the partially active filters are, because of the presence of inductors, generally more important than those of the purely active filters.

Figure 6 represents the classification of the various types of reconfigurable active filters, [10-11]. Partially active filters comprise passive inductors and capacitors (LC) integrated on silicon. They are tuned by means of either varactors or OTAs.

Entirely active filters comprise principally variable state filters, Switched Capacitor filters and filters with simulation of inductors, [10-11]. The filters with simulation of inductors belong to the continuous time filters. Here, the inductor is simulated by using the principle of the "Gyrator". Active inductors thus realized make it possible to replace the passive integrated inductors which are relatively bulky and have a low quality factor. The value of the inductance can moreover be modified using the various biasing currents of the elements. An active circuit which is equivalent to a negative resistor can also be added to improve the quality factor. Let us note however that active inductors have the disadvantage of introducing sources of noise and nonlinearities because of the big number of transistors necessary to their realization. Moreover, contrary to the passive inductors, the biasing of the transistors generates energy consumption. Inductors can be simulated in several ways: using OTAs, transistors or current conveyors. In figure 6, for each type of filter is indicated on the first line the technology and the topology or the active element used (according to the case). On the second line we have indicated the element through which the adjustment of the filter parameters is carried out.

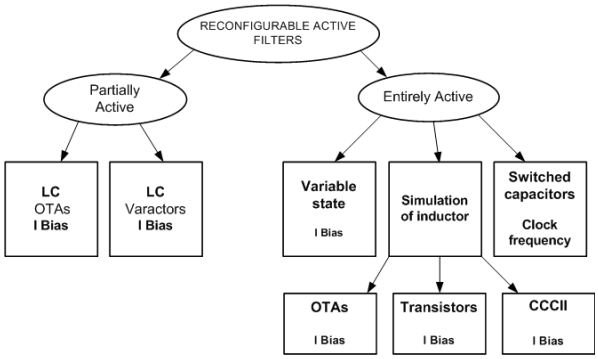


Fig. 6 : Classification of the reconfigurable active filters, [10-11].

Table III summarizes the advantages and drawbacks of existing reconfigurable active filters. They are easy to integrate on silicon and are characterized by a small size. They also exhibits low insertion losses, but their consumption is obviously more important than purely passive filters, [10-11].

4.2. Definitions

We will define in this paragraph some concepts used to well characterize the reconfigurable filters.

Adjustment range

Several ways for defining the range of adjustment of the center frequency f_0 of the filters are used by various authors. However one among them, that we will adopt, is of most interest to us. By supposing that the center frequency f_0 is adjustable between two values noted f_{0min} and $f_{0\,max}$, we will call n the tuning ratio, [12]:

$$\frac{f_{0max}}{f_{0min}} = n \qquad (1)$$

This expression is also often noted '$n : 1$'. Let us add that in order to be able to locate well the range of adjustment of f_0 it is also necessary always to indicate the value of f_{0min} or of f_{0max} . As an example, we will say that an adjustable filter will have a ratio n starting from the frequency f_{0min} when f_{0max} is equal to nf_{0min} .This definition makes it possible to illustrate the fact that two adjustable filters with an adjustment ratio of n are not equivalent if their values of f_{0max} are different (f_{0max} being 150MHz and 1GHz, for example).

TABLE III : ADVANTAGES AND DRAWBACKS OF EXISTING RECONFIGURABLE ACTIVE FILTERS.

Advantages	Drawbacks
Partially Active Filters, LC with Varactors	
reduced size compared to the external passive filters Easily integrated on silicon	Low Q for integrated inductors(about 5) Need for an active circuit for Q improvement (source of noise and non- linearity) Low tuning range of f_0 (up-to n = 1.4, [13]) Power consumption
Partially Active Filters, LC with OTA	
Reduced size compared to the external passive filters Easily integrated on silicon Q up to 350, [14]	Low tuning range of f_0 (n = 1.25, [14]) Limitation because of the performances of OTA Power consumption
Entirely Active Filters : Variables State	
Ease of realization Availability of all the transfers (LP, BP, HP)	limited performance, low frequency (up to 10MHz) Power consumption
Entirely Active Filters : Switched capacitor	
Integrated on silicon High quality factor of (up to 300, [15]) Small surface <2mm², [15]	Discrete time Need for a clock at high frequency Low tuning range (up-to n = 2.2, [15]) Frequency Limitation (up-to 530MHz, [15]) Power consumption
Entirely Active Filters : Simulation of inductor	
reconfigurable filters having the most reduced sizes wide band of adjustment : 3:1 [17] Ease of adjustment (Biasing currents) High quality factor up to 140, [17] or 300, [16]	Power consumption

Reconfigurability against tunability

In existing literature, the concepts of tunable (or adjustable) and reconfigurable filters are very often used interchangeably. It is thus necessary first of all to establish a definition of the concept of reconfigurability. We can define a 'tunable filter' as a filter whose tuning of f_0 is carried out only around f_0 principally to compensate for the drifts (thermal, technological …) while for a reconfigurable filter the variation of f_0 is expected to be carried out over a very wide frequency range. Thus, we can define now a tunable filter as a filter for which the tuning ratio n is lower than *2*; i.e. $f_{0max} < 2\ f_{0min}$ Conversely, we will say that a filter is reconfigurable if its tuning ratio is higher than *2*, which leads to $f_{0max} > 2\ f_{0min}$. Let us also specify that to be completely reconfigurable, a filter must have an adjustable quality factor.

Agility

It seems also necessary to define what we understand by agility. A frequency agile filter will be a reconfigurable filter as defined in the previous paragraph. It must moreover have the property of agility, i.e. the hop between two consecutive frequencies f_1 and f_2 must be able to be carried out very quickly during the transmission of the signal, in order not to disturb the signal processing.

4.3. Characteristics of reconfigurable active filters

Table IV compares the main characteristics of existing reconfigurable active filters. This table indicates the state of the art for each type of reconfigurable active filter as well as the corresponding reference, [10-11]. We first of all showed the most important parameters for the agility: maximum center frequency, f_0 tuning range (also characterized by ratio n), switching time of f_0 the quality factor and the necessary silicon surface. The table mentions also the consumption magnitude, the dynamic range and the insertion loss. Generally, it is noted that when f_{0max} is high (>1 GHz) the ratio n remains lower than 1.5. However, they are always smaller

TABLE IV: COMPARISON OF THE CHARACTERISTICS OF EXISTING RECONFIGURABLE ACTIVE FILTERS.

Topology of the filter			reconfiguration Technique	f_{0max} (GHz)	Maximum value of n @ f0min	Switching time of f_0	Q	Size	Consumption	Linearity and Dynamic range	insertion loss
ACTIVE FILTERS	Partially	LC	-Varactors -OTA	2.5	1.39@1.8 GHz, [13] 1.25@1.6 GHz, [14]	1-100ns	100 [18]	Very large >8 mm²	High > 54 mW	SFDR > 30dB	Low
	entirely	Variable state	-Biasing current	-	-	1-100ns	-	-	-	-	Low
		Switched capacitors	-Frequency of clock	0.6, [15]	2.2@240 MHz, [15]	1-100ns	Up to 300	Large 1mm²	High 60 mW, [15]	DR. > 30dB	Low
		With active inductor	-Biasing current	1.56, [16]	1.53@1.6 GHz, [19] 2.75@400 MHz, [20]	1-100ns	Up to 300 [16]	Very low < 0,03 mm², [21]	High 46 mW, [17]	DR. ≈ 54dB, [22]	Low

than 2.75, [20]. The switching times are in general lower than 100ns and their consumption remains always lower than 100mW. Their insertion losses remain also very low. For the entirely active filters, the silicon area is lower than 0.1mm^2, excepted for the Switched Capacitor filters.

4.4. Conclusions

As we can see from the previous sections, the implementation of multistandard transceivers requires frequency agile active filters. Indeed, it is necessary that the hopping between two consecutive frequencies f_1 and f_2 must be carried out very quickly during the transmission of the signal, in order not to disturb the signal processing. Then, for the realization of these filters, it will be necessary to use active elements having the shortest possible response delay. On the other hand, it was repeatedly shown [23, 24] that the frequency possibilities of circuits operating in current mode are much better than circuits operating in voltage mode. These circuits are also generally less complex because the implementation of mathematical functions is simpler in current mode. This will lead to smaller silicon areas. As we will see in the next section, the implementation of agile filters requires summing of many signals. These operations are easily achieved in current mode as currents are added on nodes with no need of additional active elements.

For all these reasons, the active filters that we designed were in current mode, using second generation current controlled conveyor (CCCII), [25-29]. In the next section we characterize this circuit for this application, in order to show that it is perfectly suitable for the design of frequency-agile active filters.

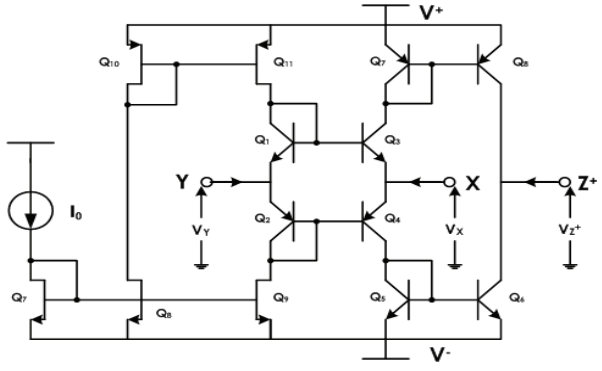
V. Controlled Current Conveyors

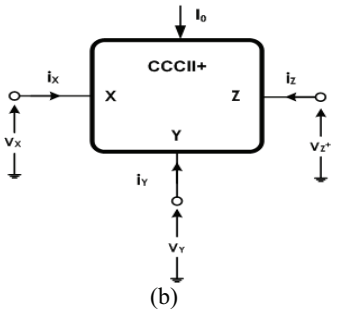
5.1 Implementation

Since their introduction in 1970, [25], the second generation current conveyors (CCII) have led to a great number of applications in the various designs of analogue electronics, like amplifiers, filters or more generally signal processing circuits, [26-27]. In 1996 were introduced the current controlled conveyors that are an evolution of previous CCII, [28-29]. They have an intrinsic resistance R_X whose value $R_X = V_T/2I_0$ is tunable by the bias current. The current controlled conveyor is widely used for the implementation of controlled electronic functions (amplifiers, filters, etc.) operating in either voltage mode or current mode. Figure 7-a shows the electric diagram of a current controlled conveyor with positive transfer from X to Z. I_0 is the bias current. The current conveyor uses a mixed trans-linear loop at the input (transistors Q1 to Q4), MOS mirrors for biasing (Q5 to Q7) and (Q10 to Q11) and bipolar mirrors for the signal processing in order to achieve the highest possible frequency performances. This circuit operates in class AB. Figure 7-b shows its associated symbol. Its matrix relationship between conventional variables is then, [28-29]:

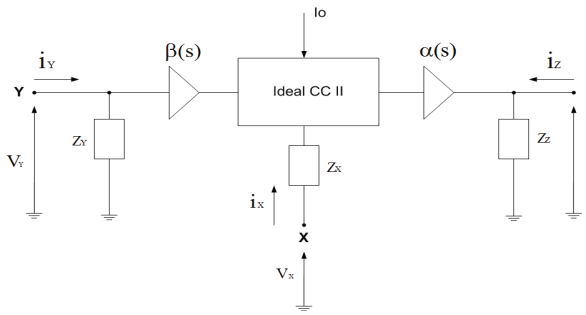
$$\begin{pmatrix} i_y \\ V_x \\ i_{Z+} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ i_x \\ V_{Z+} \end{pmatrix} \qquad (2)$$

(a)





(b)



(c)

Fig. 7 : Current controlled conveyor CCCII+:
(a) Schematic implementation, (b) Associated symbol,
(c) General equivalent circuit including parasitic elements.

Figure 7-c shows the general equivalent circuit that is used to represent the behavior of a CCCII+ for a fixed value of the bias current I_0 . It contains an ideal CCCII+ between ports X', Y' and Z'. $\beta(s)$ and $\alpha(s)$ with:

$$\beta(s) = {\beta_0}/{\left(1 + {s}/{\omega_\beta}\right)} \text{ and } \alpha(s) = {\alpha_0}/{\left(1 + {s}/{\omega_\alpha}\right)}$$

are respectively, the voltage (from Y to X) and the current (from X to Z) frequency dependent transfers of the conveyor.

β_0 and α_0 ($\beta_0 \approx \alpha_0 \approx 1$) are respectively the transfers at low frequency. ω_α and ω_β are their corresponding poles.

5.2 Characteristics and simulated performances

The different circuits were integrated in 0.25 µm SiGe BiCMOS technology from STMicoelectronics, [31]. The transition frequency of the NPN transistors in this technology is 55 GHz; the vertical PNP transistors have f_{TP} of 6 GHz. The characteristics of the CCCII in this technology are given in table V, for ± 2.5 V and I_0 = 100µA. Table VI gives the frequency performances of the CCCII as a function of the bias current. These indicate that the -3 dB bandwidths for $\alpha(s)$ always remain close to the transition frequency of the PNP transistors. The -3 dB bandwidths for $\beta(s)$ are much greater.

TABLE V: CHARACTERISTICS OF THE CCCII, $V^+ = -V^- = 2.5$ V; $I_0 = 100$ µA.

	Voltage follower	Current follower
Gain (dB)	-0.009	0.03
-3dB Bandwidth	21.6 GHz	4.5 GHz
Input Impedance	466kΩ//0.046pF	162Ω
Output Impedance	162Ω	152kΩ//0.04pF
Output offset	486µV	3µA
Consumption	2.57 mW	2.57 mW

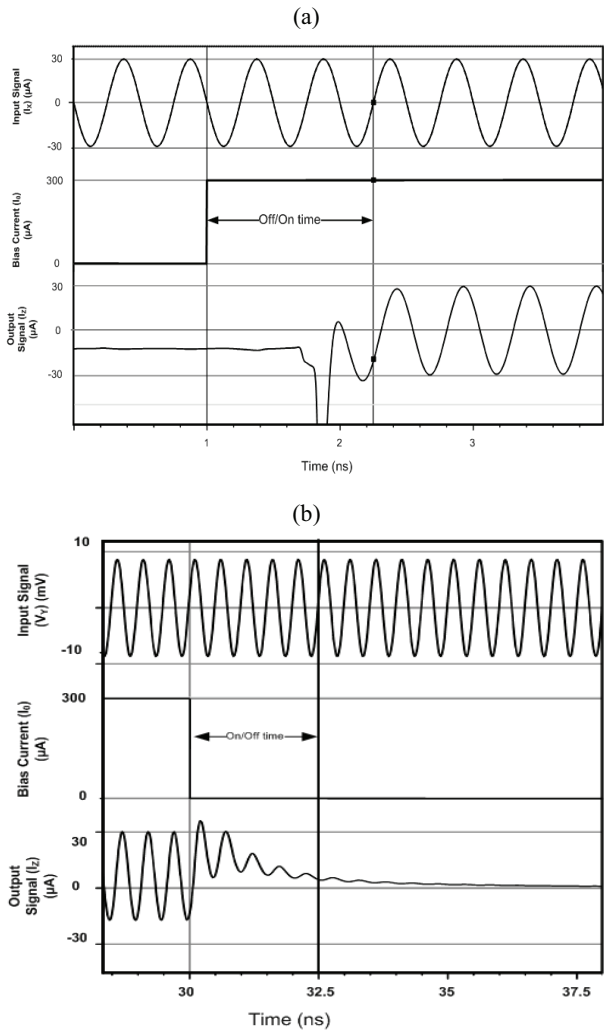


Fig. 8: Transient responses of the CCCII (a) "Off/On time", I_0 varies from 0 µA to 300 µA; (b) "On/Off time", I_0 varies from 300 µA to 0 µA.

TABLE VI: FREQUENCY PERFORMANCES OF THE CCCII, as a function of I_0; $V^+ = -V^- = 2.5$ V

I_0 (µA)	Current follower ($R_L = 0$)		Voltage follower ($R_L = \infty$)	
	f_c à -3 dB $\alpha(s)$, (GHz)	α_0, (dB)	f_c à -3 dB $\beta(s)$, (GHz)	β_0, (dB)
50	3.4	0.067	11.5	-0.008
100	4.6	0.029	20.6	-0.009
200	5.4	0.061	38.6	-0.011
300	5.4	0.38	50.4	-0.016
500	4.6	1.39	60.1	-0.065

Besides the frequency responses, it is also necessary for this type of application to characterize the speed of the response of the CCCII+. Table VII gives the values of the slew rate and the 1% settling time when the CCCII is used as current follower with zero load or as voltage follower with infinite load. The relatively high Slew rates and short settling time are good characteristic performances of the CCCII.

TABLE VII: SLEW RATE AND SETTLING TIME OF THE CCCII AS A FUNCTION OF I_0.

	Voltage follower		Current follower	
I_0, (µA)	"Slew Rate", (V/µs)	Settling Time, (ps)	"Slew Rate", (mA/µs)	Settling Time, (ps)
50	96	104	50	200
100	179	58	44	229
200	194	50	45	226
300	190	48	46.4	227

For the implementation of our agile filters, many CCCII are used as switches (open when not biased and closed when the biasing current is equal to I_0). It is therefore necessary to determine the starting (Off/On) and the cutoff (On/Off) time defined as the delay for the switch to go from Off to On state and vice versa, [10].

Figure 8 that shows the input and output signals of CCCII as well as the biasing current I_0, illustrates its functional behavior. It allows also identifying the starting and cutoff times. The starting time is reached when the input and output signals are identical. We consider that the cutoff is reached when the amplitude of the output of CCCII is equal to 1/20 of the input signal.

TABLE VIII: VARIATION OF THE OFF/ON TIME AND THE ON/OFF AS A FUNCTION OF I_0.

I0 (µs)	Off/On time (ns)	On/Off time (ns)
50	≤ 2,95	≤ 2,5
100	≤ 1,93	≤ 2,5
200	≤ 1,35	≤ 2,5
300	≤ 1,25	≤ 2,5

Table VIII indicates the variation of these times as a function of the value of the biasing current I_0. These times, which are always lower than 3ns confirm that the filters implemented with CCCII are indeed agile.

VI. THE THEORY OF FREQUENCY AGILE FILTERS

The theory of frequency agile filters will be recalled here briefly. This theory is based on a classical second order filter structure which includes an input and two different outputs at least: bandpass and lowpass, [10, 32, 33]. Figure 9 shows this classical circuit operating in voltage mode. This cell that is called class 0 filter, constitutes the basic element for the implementation of a frequency agile filter.

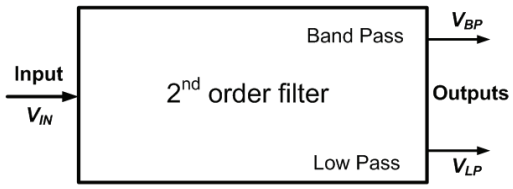


Fig. 9: Basic second order filter including two different outputs (class 0 agile filter).

V_{IN} is the input voltage of the filter. V_{BP} and V_{LP} are respectively its band pass and low pass outputs. The transfer functions $F_{BP}(s)$ and $F_{LP}(s)$ are respectively given by:

$$F_{BP}(s) = \frac{V_{BP}}{V_{IN}}(s) = \frac{a's}{1 + as + bs^2} \quad (3)$$

$$F_{LP}(s) = \frac{V_{LP}}{V_{IN}}(s) = \frac{d'}{1 + as + bs^2} \quad (4)$$

In these equations a and b are real positive constants to ensure stability of the filter. We also suppose that a' and d' are real positive constants. The values of these constants are related to the values of the different components of the circuit in fig. 9. They allow us to determine the characteristic parameters of the filter.

Its center frequency is given by $f_0 = 1/2\pi\sqrt{b}$. This frequency corresponds simultaneously to the center frequency of the bandpass and the -3dB cutoff frequency for the low-pass output.

The quality factor is given by $Q = \sqrt{b}/a$.

The gain at f_0 of the band pass is $G_{BP} = a'/a$ and its -3dB Bandwidth is $\Delta f = a/2\pi b$.

The gain at low frequency for the low pass output is $G_{LP} = d'$.

Figure 10 shows the Class 1 second order frequency agile filter circuit obtained from the previous basic cell, [10, 32-33]. The voltage of the low pass output is first amplified through an amplifier with an adjustable gain A. The amplified voltage is then added to the input voltage V_{IN}. The new input voltage of the filter is then V_E and the circuit always includes two outputs: V_{BP} and V_{LP} which remain of the same type as the starting structure. The input signal of the new circuit being now given by $V_E = V_{IN} - AV_{LP}$.

The characteristic frequency f_{0A} of this new circuit is then related to f_0 of the class 0 filter and the gain A of the amplifier by:

$f_{0A} = f_0\sqrt{(1 - Ad')}$. By the same way, its Q-factor Q_A is given by:

$Q_A = Q\sqrt{(1 - Ad')}$.

The voltage gain of the bandpass output remains identical to the gain of the bandpass in the starting cell, the gain of the low pass being now given by : $G_{LPA} = G_{LP}/(1-Ad')$. All these relations indicate that the class 1 filter will be stable provided that $(1-Ad')$ remains positive (Routh-Hurwitz criterion), [10, 32-33].

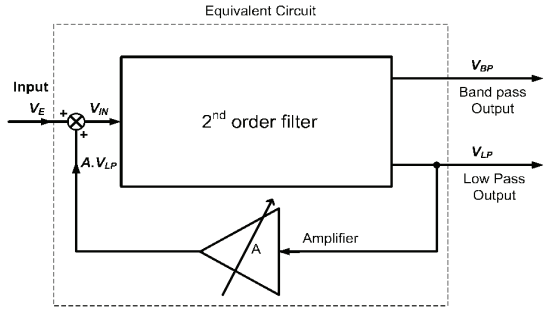


Fig. 10: Class 1 frequency agile filter made from the basic cell.

The theory above has been generalized to the n[th]-class to obtain the class n frequency agile filter,[10, 32-34].

Fig. 11 shows the class n frequency agile filter obtained in the same way as above from the class $(n-1)$ implementation. It is noticeable that only two types of adjustable-gain amplifiers are necessary: amplifiers with gain A and amplifiers with gain $(1-Ad')$, with $A < 1/d'$. The latter condition is necessary to ensure the stability of the circuits.

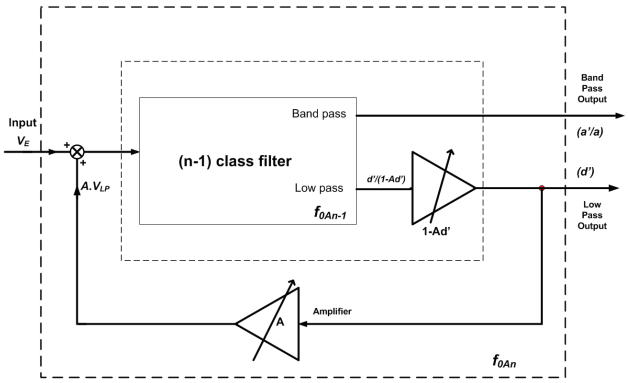


Fig. 11: Class n frequency agile filter.

Table IX gives the characteristic parameters of the n[th]-class agile filter as a function of the parameters of the zero-class filter.

Figure 12 shows the variation of f_{0An} according to the parameter n and the gain A of the amplifier. This figure illustrates the linear shape of the ratio for n =2. It also indicates that when A is negative the variation of f_{0An}/f_0 will be faster as much as n will be greater.

TABLE IX: CHARACTERISTIC PARAMETERS OF THE N[TH]-CLASS AGILE FILTER (FIG. 11) AS A FUNCTION OF THE PARAMETERS OF THE ZERO-CLASS FILTER (FIG. 9).

	Starting Block (fig. 9)	n[th]-class frequency agile filter (fig. 11)
Center frequency	$f_0 = \frac{1}{2\pi\sqrt{b}}$	$f_{0An} = \sqrt{(1-Ad')} \cdot f_{0An-1} = (1-Ad')^{\frac{n}{2}} f_0$
Q-factor	$Q = \frac{\sqrt{b}}{a}$	$Q_{An} = \sqrt{(1-Ad')}\, Q_{An-1} = (1-Ad')^{\frac{n}{2}} Q$
BP Gain	$G_{BP} = \frac{a'}{a}$	$G_{BPAn} = G_{BP}$
BP : -3dB Bandwidth	$\Delta f = \frac{a}{2\pi b}$	$\Delta f_{An} = \Delta f_{An-1} = \Delta f$
LP Gain	$G_{LP} = d'$	$G_{LPAn} = \frac{G_{LP}}{(1-Ad')}$

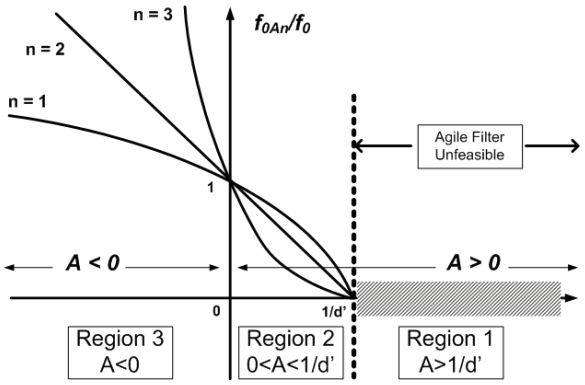


Fig. 12: Variation of f_{0An}/f_0 as a function of gain A for various values of n.

VII. Implementation of the Frequency-Agile Filter

7.1 Generalities

As it is shown on figure 12, a particularly interesting case is the class 2 filter for which the equation between f_{0An} anf f_0 is linear according to A: $f_{0A2} = f_0\ (1\text{-}Ad')$ with $A < 1/d'$. In this case the modulus of the various sensitivities are less than unity [10, 32, 34]. In this way, a variation of A about *1%* brings a relative variation of f_{0A2} about *1%* too. The same is also true for Q.

We decided to implement this case for the implementation of the agile filter for multistandard transceivers. We selected A<0 in order to have f_{0A2} higher that starting frequency f_0.

Figure 13 shows the schematic implementation of the class 2 frequency agile filter that has been directly deduced from the theory above, [10, 34]. In this schema, that has been drawn in voltage-mode for simplicity, input and output variables are voltages. The equivalent schema operating in current-mode, where input and output variables will be currents, can be deduced easily. In this schema, the input currents of the amplifiers A must be identical to the input current of amplifier *(1-Ad')* for the one and to the output current of amplifier *(1-Ad')* for the other.

Note that these copies of currents can be obtained easily from the CCCII, using dual output CCCIIs for example.

7.2 Basic second order filter structure

Figure 14 shows the second order (class 0) current mode filter implemented from three CCCII+. In this circuit, the conveyors 1 and 2, and capacitors C_1 and C_2 act as a shunt RLC circuit. Conveyor Q, connected as a negative resistance allows tuning of the Q-factor through current I_Q, [17].

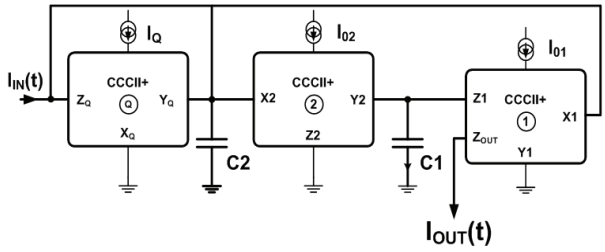


Fig. 14 : Zero-class 2nd order current mode filter.

This circuit has a bandpass output I_{OUT}. The voltage across capacitor C1 has a lowpass transfer, [10, 32-33].When the bias currents of conveyors 1 and 2 have been chosen identical (ie. $I_{01} = I_{02} = I_{01}$ that implies $R_{X1} = R_{X2} = R_X$) and capacitors C1 and C2 have same values (ie. C1 = C2 = C), these transfers are expressed as :

$$\frac{I_{OUT}}{I_{IN}}(s) = \frac{-R_X C s}{D(s)} \tag{5}$$

$$V_{C1}(s) = \frac{R_X}{D(s)} I_{IN} \tag{6}$$

With $D(s) = 1 + (2R_{XQ} - R_X^2/R_{XQ})Cs + R_X^2 C^2 s^2$

The characteristics parameters of the filter are given by :

$$f_0 = 1/2\pi R_X C \tag{7}$$

$$Q = R_{XQ}/(2R_{XQ} - R_X) \tag{8}$$

The filter is orthogonal, the bias current I_0 allows, but to some extend only, to change f_0 .The current I_Q makes it possible to tune Q to the desired value.

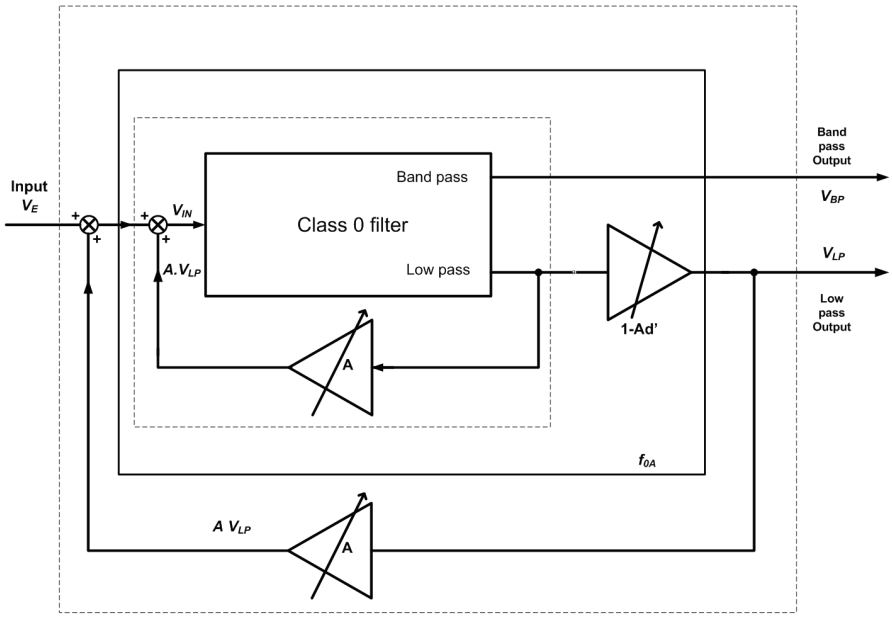


Fig. 13: Schematic implementation of the class 2 frequency agile filter.

The gain of the band pass output is -*Q*.
The previous equation for *Q* shows that the stability of the filter implies that $2R_{XQ}$ exceeds R_X, i.e. that I_Q must be less than $2I_0$.

7.3 Frequency-Agile filter implementation

The complete implementation of the frequency-agile bandpass filter operating in current mode that is directly deduced from the schema in Fig. 13 above is shown in Fig. 15. $I_{IN}(t)$ is the input current. The various band pass outputs are available on $I_{OUT}(t)$. This circuit has four center frequencies : f_0 , $(f_{0A2})_1$, $(f_{0A2})_2$ and $(f_{0A2})_3$.
The value of gain *A* is negative in order to have frequencies $(f_{0A2})_1$, $(f_{0A2})_2$ and $(f_{0A2})_3$ higher than the starting frequency f_0. They are given by the following expressions: $(f_{0A2})_i = f_0 (1\text{-}A)_i$, with *i= 1,2 or 3.*
When the three switches K_1 to K_3 are open, none of the feedback CCCII+ is biased. The filter is then equivalent to the starting class 0 filter. The center frequency is f_0. When one of the switches K_1 to K_3 is closed (e.g. K_i with i= 1, 2 or 3) the current I_{0CRi} biases the CCCII+ of the corresponding feedback C_{Ri}. The resulting center frequency is then $(f_{0A2})_i$.
The unique feedback current conveyor (C_{Ri}) used in this structure allows synthesizing all different feedbacks of the theoretical diagram in figure 13. The gain A_i of the amplifier is given by $|Ai| = I_{0CRi}/I_0$. On the other hand, the corresponding gain of the output Z of each feedback conveyor is clearly indicated on the symbol. The output Z with gain $(2\text{-}A_i)$;(i.e. $i_z/i_x = (2\text{-}A_i)$) was obtained by properly dimensioning the emitter areas of the transistors of this output, [10, 34]. The expression of the feedback amplified current that is added to the input (see fig. 15) is then, with A_i negative:

$$(2 - A_i)V_{C1}/R_{XCRi} \qquad (10)$$

Where $R_{XCRi} = V_T/2I_{0CRi}$ is the intrinsic resistance of the input X of CCCII (C_{Ri}).
Note that the joint use of the current mode and CCCII conveyors allows us to obtain a frequency-agile filter implementation having a reduced number of active elements.

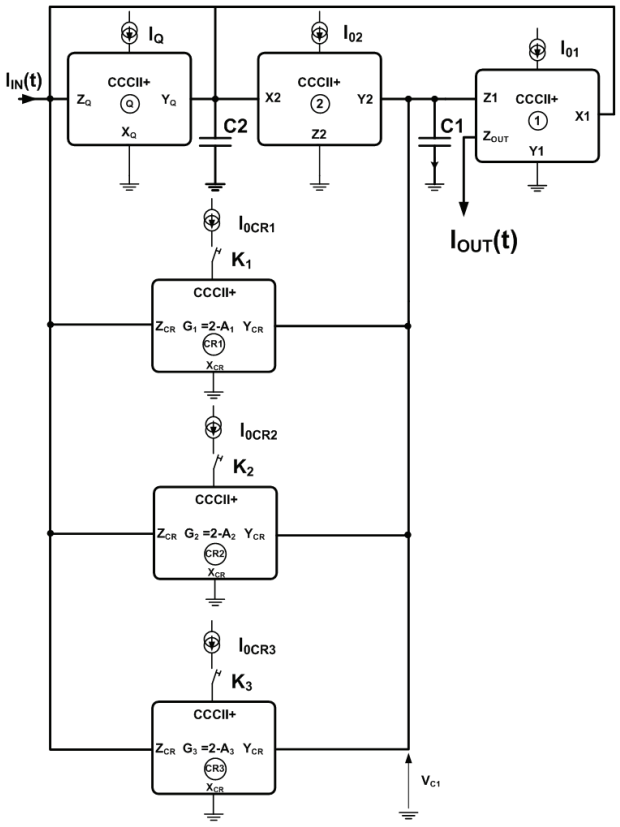


Fig. 15: Current-mode Frequency-agile filter with A<0.

VIII. VALIDATION RESULTS

The frequency-agile filter in Fig. 15 was implemented, with C1 = C2 = 2pF, in the 0.25 µm SiGe BiCMOS technology from STMicoelectronics, [31]. The CCCII+ that we have characterized above in section 5.2 was used. The circuit was biased under ± 2.5 Volts. Fig. 16-a shows the frequency responses obtained for the filter with K_1 to K_3 open, when the bias current I_0 is varied from 50µA to 200µA. Note that beyond 100µA the gain of the filter decreases significantly as well as the value of *Q*, mainly because of the parasitic resistances R_Y, R_Z of the CCCII+ which appear to be in parallel to capacitors C1 and C2. Indeed the values of these parasitic resistances decrease when I_0 increases.

Table X: Various characteristics of the frequency-agile filter with K_1 to K_3 open.

I_0 (µA)	I_Q (µA)	f_0 (MHz)	Q	Power consumption (mW)
50	100	237,5	2,5	5,5
75	170	320	2,6	8,6
100	250	390	2,64	11,92
200	450	597	1,37	22,4

Table X gives the corresponding values of f_0. We have also shown I_Q and the power consumption of the filter. All these results show the limitations of conventional second order filters. Indeed tuning the bias current I_0 do not allow a wide tuning range of center frequency f_0. For the following simulations we fixed the value of I_0 at 50µA.
Fig. 16-b shows the four frequency responses obtained for the frequency-agile filter varying the position of the switches K_1 to K_3.
For K_1 to K_3 open, the central frequency is 239.7 MHz.
For K_1 closed, K_2 and K_3 open ($A_1 = 1$ and $I_{0CR1} = 50\mu A$), the central frequency is 466.4 MHz.
For K_2 closed, K_1 and K_3 open ($A_2 = 3$ and $I_{0CR2} = 150\mu A$), the central frequency is 835.5 MHz.
For K_3 closed, K_1 and K_2 open ($A_3 = 6$ and $I_{0CR3} = 300\mu A$), the central frequency is 1223 MHz.
It should be noted that for our frequency agile filter, the corresponding value of $n = f_{0max}/f_{0min}$ is equal to 5.1. To our knowledge such high value was never published before for an agile active filter (see table IV, where the maximal value is *n* = 2.75, [20]).
Also note that the positions of the switches can easily be controlled digitally. In that case, we obtain a digitally controlled frequency-agile filter.
The frequency agile filter has been implemented here with integer values for gains A_i. This leads in consequence to integer values for the ratios of the emitter areas of the output transistors. Note that this is not necessary and any value for the ratios can be realized. In consequence, any central frequency $(f_{0A2})_i$ can be obtained.
Also note that the center frequency $(f_{0A2})_i$ could also be adjusted if necessary by slightly adjusting the bias current I_0 of conveyors 1 and 2. In the same way, modification of biasing current I_Q allows also tuning of the corresponding Q-factor.

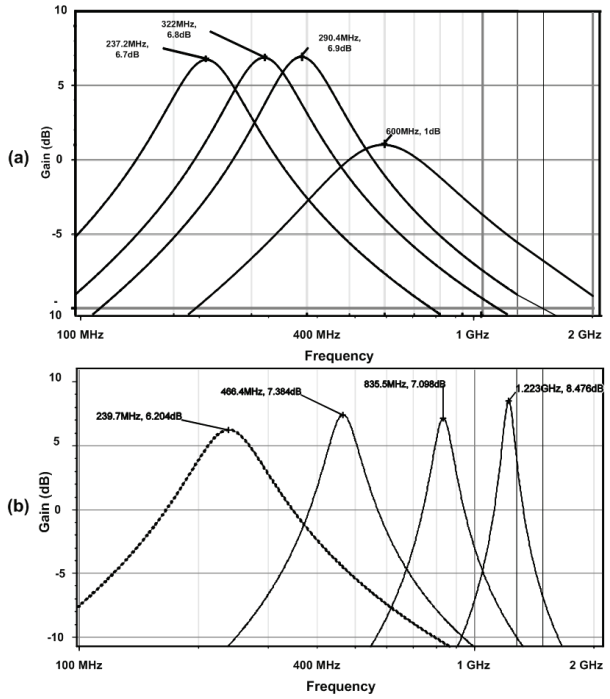


Fig. 16 : Frequency response of the frequency-agile filter.
(a) Frequency responses of the class 0 filter obtained varying I_0.
(b) Frequency responses obtained by varying the positions of the switches, $I_0 = 50\mu A$.

IX. CONCLUSIONS

In this paper, we firstly recalled the existing techniques for multistandard transceivers implementation: multichannel receiver with elements in parallels or reconfigurable elements. Then, after having given the definitions of the concepts used to fully characterize reconfigurable filters, we made the state-of-the-art of them. To be able to implement a true frequency-agile filter it is necessary that the hopping between two consecutive center frequencies of a reconfigurable filter must be carried out very quickly. It must have in consequence very reduced switching times. The second generation current controlled conveyor has then been characterized in this way. It has been shown that, with switching times that are less than 3ns, this active element is a perfect candidate for implementing frequency agile filters.

The theory and the main properties of the frequency agile filters recently introduced were recalled briefly in the second part of the paper. This has then been used to design a 2nd order bandpass frequency-agile filter from the CCCII+. This filter operates in current-mode, it has four center frequencies digitally controlled and a value for f_{0max}/f_{0min} equal to 5.1, with $f_{0max} = 1.2$ GHz. This frequency-agile filter appears in consequence eminently suited for multistandard transceivers.

It can also be noted that frequency agile filters reaching higher values for f_{0max} will require more efficient SiGe BiCMOS technology with higher f_{TP}. This PNP transition-frequency appears indeed to be the most important limiting parameter for the used technology.

REFERENCES

[1] Pui-in Mak, Seng-Side U, Rui P. Martins "Transceiver structure selection: Review, State-of-the-art survey and case study" IEEE Circuits and Systems Magazine, Vol. 7, Issue 2, 2007, pp. 6-25.

[2] Behzad Razavi, "RF Microelectronics" Prentice Hall (1997), ISBN : 978-0138875718.

[3] Yi-Ran Sun, "Generalized Bandpass Samplig Receivers for Software Defined Radio", Doctoral Thesis, Royal Institute of Technology, ICT, Stockholm, Sweden, 2006.

[4] Mitola, J., "The software radio architecture" IEEE Comm. Magazine, Vol.33, No.5, May 1995, pp. 26-38.

[5] Abidi, A.A. "The Path to the Software-Defined Radio Receiver", IEEE Journal of Solid-State Circuits, Vol. 42, Issue 5, May 2007, pp. 954-966.

[6] Mac Leod, J.R., Nesimoglu, T.; Beach, M.A., Warr, P.A., "Enabling technologies for software defined radio transceivers", MILCOM 2002 Proceedings, Volume 1, 7-10, Oct. 2002, pp. 354-358.

[7] Maurer, L., Hueber, G., Dellsperger, T., Burger, T., Huemer, M, Weigel, R., "A frequency agile terminal receiver for wireless multi-standard applications", IEEE Radio and Wireless Symposium, 17-19 Oct. 2006, pp. 291- 294.

[8] Balwant Godara, "Conception of novel wideband performance-controllable RF circuits in SiGe : Impedance matching circuit, single-ended to differential baluns, and single-ended and differential low-noise amplifiers", Doctoral Thesis, IMS Lab., Bordeaux, France, November 2006.

[9] Cedric Majek, "Contribution a l'etude d'un Synthetiseur de Frequence pour Objets Communicants Multistandards en Technologie CMOS SOI", Doctoral Thesis, IMS Lab. Bordeaux, France, October 2006.

[10] Yahya Lakys, "Filtres à Fréquence Agile Totalement Actifs : Théorie Générale et Circuits de Validation en Technologie SiGe BiCMOS 0.25µm", Doctoral Thesis, IMS Lab., Bordeaux, France, December 2009.

[11] Lakys, Y., Godara, B., Fabre, A. "Cognitive and Encrypted Communications, Part 1: State of the Art for Frequency-Agile Filters", ELECO'09 Proceedings, pp. 1-16, 5-8 November 2009, Bursa, Turkey.

[12] Koochakzadeh, M., Tamijani, A., "Multi-scale tunable filter covering a frequency range of 6.5:1", Micro. Symp. Digest, 2008 IEEE MTT-S International, 15-20 June 2008, pp. 1023-1026.

[13] Nakaska, J.K.; Haslett, J.W., "2 GHz Automatically Tuned Q-Enhanced CMOS Bandpass Filter", IEEE/MTT-S International Microwave Symposium, 3-8 June 2007, pp. 1599–1602.

[14] Pipilos, S., Tsividis, Y.P., Fenk, J., Papananos, Y., "A Si 1.8 GHz RLC filter with tunable center frequency and quality Factor", IEEE j. Solid-State Circuits, vol. 31, No 10, 1996, pp. 1517-1525.

[15] El Oualkadi, A.E., El Kaamouchi, M., Paillot, J.-M., Vanhoenacker-Janvier, D., Flandre, D., "Fully Integrated High-Q Switched Capacitor Bandpass Filter with Center Frequency and Bandwidth Tuning", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 3-5 June 2007, pp. 681–684.

[16] Salem, S., Fakhfakh, M., Masmoudi, D, Loulou, M., Loumeau, P., Masmoudi, N., "A high performances CMOS CCII and high frequency applications", Analog Integrated Circuits and Signal Processing, Vol. 49, Number 1, October 2006, pp. 71-78.

[17] Fabre, A, Saaid, O., Wiest, F., Boucheron, C., "High Frequency High-Q BiCMOS Current-Mode Bandpass Filter and Mobile Communication Application", IEEE Journal Of Solid-State Circuits, Vol. 33, No. 4, April 1998, pp. 614–625.

[18] Dülger, F., Sánchez-Sinencio, E., Silva-Martinez, J., "A 1.3-V 5-mW fully integrated tunable bandpass filter at 2.1 GHz in 0.35-µm CMOS", IEEE journal of Solid-State Circuits, vol. 38, No 6, 2003, pp. 918-928.

[19] Yue Wu, Chunlei Shi, Xiaohui Ding, Ismail, M., Olsson, H., "Design of CMOS VHF/RF Biquadratic Filters", Analog Integrated Circuits and Signal Processing, Vol. 33, Issue 3, December 2002, pp. 239–248.

[20] Yue Wu, Ismail, M., Olsson, H., "RF Bandpass fitler design based on CMOS Active inductors", IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 50, No. 12, December 2003, pp. 942–949.

[21] Zhiqiang Gao, Mingyan Yu, Yizheng Ye, Jianguo M "A CMOS bandpass filter with wide-tuning range for wireless applications", Proceedings ISCAS 2006, pp. 867-870.

[22] Fabre, A., Saaid, O., Wiest, F., Boucheron, C., "High frequency applications based on a new current controlled conveyer", IEEE

Transaction on Circuits and Systems, vol. 43, February 1996, pp. 82-91.
[23] Roberts, G.W., Sedra A. S., "All current-mode frequency selecting circuits", electronic letter, Vol. 27, No. 12, 1999 pp 759-761.
[24] Fabre, A., "Electronique analogique rapide", Ellipses, Technosup, 204 pages, 1st edition, ISBN13 : 978-2-7298-4386-1, juin 2009.
[25] Sedra, A., Smith, K., "A second-generation current conveyor and its applications", IEEE Transactions on Circuit Theory, Vol. 17, Issue 1, February 1970, pp. 132-134.
[26] Sedra, A., "The current conveyor: history and progress", IEEE International Symposium on Circuits and Systems, Vol. 3, 8-11 May 1989, pp. 1567-1571.
[27] Fabre, A., "Dual translinear voltage/current convertor", Electronics Letters, Vol. 19, November 1983, pp. 1030-1031.
[28] Fabre, A, Saaid, O., Wiest, F., Boucheron, C., "High Frequency High-Q BiCMOS Current-Mode Bandpass Filter and Mobile Communication Application", IEEE Journal Of Solid-State Circuits, Vol. 33, No. 4, April 1998, pp. 614–625.
[29] Fabre, A., Saaid, O., Wiest, F., Boucheron, C., "Low Power Current-Mode Second-Order Bandpass IF Filter", IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 44, No. 6, June 1997, pp. 436–446.
[30] Fabre, A., Saaid, O., Wiest, F., Boucheron, C., "High frequency applications based on a new current controlled conveyer", IEEE Transaction on Circuits and Systems, vol. 43, February 1996, pp. 82-91.
[31] Multi-Projets website : http://cmp.imag.fr.
[32] Lakys, Y., Godara, B., Fabre, A. "Cognitive and Encrypted Communications, Part 2: A new approach to Active Frequency-Agile Filters and Validation results for an Agile Bandpass Topology in SiGe-BiCMOS", ELECO'09 Proceedings, pp. 16- 29, 5-8 November 2009, Bursa, Turkey.
[33] Lakys,Y., Fabre, A., " The Shadow Filter, A new Familly of 2nd Order Filters", Electronic letters, 2010, vol. 46, n° 4, pp. 276-277.
[34] Lakys,Y., Fabre, A., "Shadow Filters, Generalization to the nth Class", Electronic letters, 2010, vol. 46, n° 14, pp. 985-986.