

Design of a Three-Phase Unity Power Factor Single-Stage Telecom Rectifier

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Abstract

This paper presents the design and implementation of a three-phase unity power factor single-stage rectifier. The main use of the converter is expected to be in the telecommunications industry where it supplies constant DC voltage to the telecom network and charges the high capacity batteries while providing unity power factor to the utility. The converter is based on the flyback topology operating in discontinuous current mode (DCM). A fast dynamic response, low cost, small size, and a very simple control are the further viable benefits of the converter. The study includes finding an optimum transformer design with the lowest leakage inductance and the selection of components with the lowest parasitic effects for high efficiency and good performance. After the design is verified using the Simulink and PLECs models of the converter, a full-scale prototype was implemented to evaluate the performance of the design. Finally, experimental results demonstrate that converter works successfully and meet the design expectations.

1. Introduction

The harmonics drawn from the utility lines due to distorted current waveforms and low power factor caused by these currents are important power quality problems [1-4]. The common approach for the solution of these problems is to use two-stage power conversion schemes. The two-stage schemes employ a power-factor correction stage where harmonic currents are eliminated and another cascaded stage such as a DC-DC converter for generating regulated output with fast dynamic response and isolation. However, the cascaded converters increase the complexity of the system, and so the cost and the size of the product. For this reason, major research has been carried out for the development of less complex single-stage systems which provide the same performance as their two-stage counterparts [5-9]. Most manufacturers are still looking for realization of alternative systems that improve on the specifications of the products available today, but also offer lower cost, smaller size, and simpler control requirements with superior dynamic response. Studies have showed that the flyback based converter topologies still have the most potential to achieve these demands [10-13]. However, the research so far has considered the flyback topology being more feasible in low power applications. In this study, we propose a design that demonstrates the practicability of single-stage flyback based PFC systems in high power applications.

The circuit topology of the proposed conversion system is shown in Fig. 1. The converter is based on flyback topology operated in discontinuous current mode (DCM). Flyback topology offers the lowest component count and isolation. Operation in DCM mode offers many advantages such as

elimination of turn-on switching losses that allows higher switching speeds for IGBTs, elimination of half-plane zero in the feedback loop that allows a robust and stable control, and lastly very fast dynamic response.

The main disadvantage of operation in DCM is the discontinuous current waveforms with high peaks both at the input and at the output of the converter. For this reason, a low-pass filter at the input and a capacitive smoothing filter at the output, as shown in Fig. 1, are needed to remove the high frequency components of the current and to reduce EMI. Moreover, both of these filters especially the capacitor at the output should have high RMS ripple current capacity.

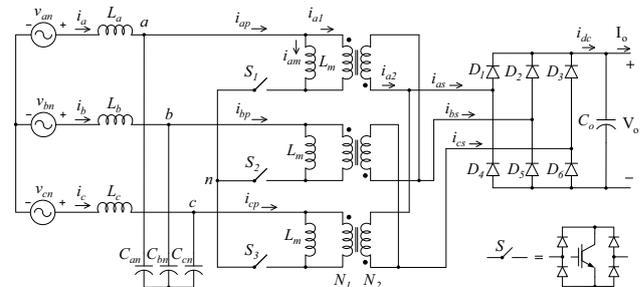


Fig. 1. The circuit topology of the proposed converter

Another challenging design problem in high-power flyback based converters is to minimize the parasitics especially the leakage inductance in the transformer and the parasitic inductances along the paths through which the energy transfer occurs. Energy transfer from input to the output suffers significantly especially during current transfers that occur at switch turn-offs [9, 14-15]. Even so, a carefully designed flyback transformer wound on a distributed-air gapped ferrite core with taller window area and using sandwiched winding techniques are considered as effective solutions to the leakage inductance problem. The work presented in reference [9] has implemented such a converter and obtained results that could be used as proof of concept. Now, in this work, major developments and design improvements have been made to bring the idea from a concept into a commercially viable product.

As mentioned above, the main design improvements include the following:

- All of the current carrying power lines are transferred to the printed circuit board (PCB) instead of bus bars.
- Low-profile screw type IGBT and diode packages such as SOT 227 are used to shorten the current paths and therefore to reduce the parasitic inductances.
- Smaller sized components with reduced current ratings are used in parallel instead of large single component in order to

reduce parasitics. For example, Schottky diodes will be paralleled and many small value capacitors will be paralleled to make the output capacitor.

- Secondary sides of the flyback transformers are connected as Delta for two reasons: zero sequence currents cannot flow to output, and it allows lower turns ratio of the transformers which reduces the voltage stress across the primary side switches.
- Distributed air gap in the core, taller window area, and sandwiched windings with wide copper strips.

2. Basic Operational Principles of the Converter

The waveforms shown in Fig. 2 are the theoretical voltage and current waveforms over the positive half-cycle of one phase of the converter shown in Fig. 1. These waveforms will be used to explain the basic operational principles of the converter. The v_{an} is the line-to-neutral input voltage, i_{ap} is the instantaneous flyback transformer primary winding current which is also the unfiltered converter input current, i_a is the instantaneous average of i_{ap} , which is the current to be drawn from the utility line.

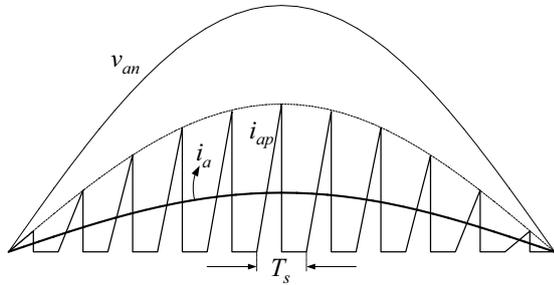


Fig. 2. The theoretical waveforms of the input voltage (v_{an}), the flyback transformer primary winding current (i_{ap}), and its instantaneous average (i_a)

The converter is operated with a fixed switching frequency. The waveform of i_{ap} in Fig. 2 indicates a duty ratio of the switch at 50%. The three switches at the primary side of the converter are operated simultaneously using the same gate pulse. Because of DCM operation, every time the switches are turned on, the primary current starts from zero and increases almost linearly to a maximum. During this mode, energy is stored in the magnetizing inductance L_m of the flyback transformer, no current flows to the secondary side due to three-phase rectifiers at the output, during this time the load power is supplied by the output capacitor C_o . When the switches are turned off, all of the energy stored in the magnetizing inductances of each phase is transferred to the output through the flyback transformer secondary windings and the three-phase rectifier. The capacitor C_o smoothes the ripple at the output voltage caused by the rectified current pulses.

3. Analysis of the Converter

Performing the analysis only for the positive half-cycle of the input voltage as shown in Fig. 2 is adequate to drive all of the necessary design equations. Moreover, we will assume that all the components are ideal and converter operates in DCM mode and in periodic steady-state. Also assume a pure sinusoidal voltage $v_{an}(t) = \hat{V}_{an} \sin \omega t$ is applied to the phase a of the converter.

As shown in Fig. 2, the peak of input current i_{ap} depends on the applied voltage and the duty ratio of the switch. If the duty ratio is fixed, then all the peaks will change according to the voltage. Because the applied voltage changes sinusoidally at the input, the peaks of the current will also change sinusoidally, as indicated by the dashed line in Fig. 2. This peak envelope is the sign of fact that the moving average of the triangular pulse train (the input current) will also be sinusoidal, which is shown by the ticker line in Fig. 2 as i_a . The moving average of this current waveform can be written as $i_a(t) = \hat{I}_a \sin \omega t$. It is important to note that this averaged current is in phase with the input voltage. This is how the converter achieves unity power factor.

Fig. 3 shows the waveforms of primary current i_{ap} and secondary side current i_{as} reflected to the primary side over a switching period when the input voltage is at its peak. The sum of these two currents gives the flyback transformer magnetizing current $i_m = (i_{ap} + N_2/N_1 i_{as})$. As indicated in Fig. 3, we have assumed that the change in the input voltage during switch on time is negligible and therefore the increase in the magnetizing current is linear. As shown in Fig. 3, a small dead time region can be added every time after the secondary current is brought to zero to guarantee DCM operation under abnormal conditions.

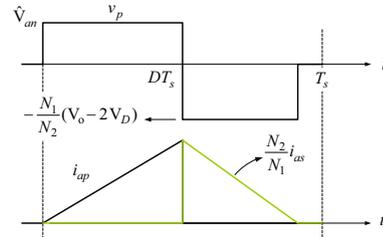


Fig. 3. The waveforms of the transformer primary voltage (v_p), transformer primary current (i_{ap}) and secondary current (i_{as}) reflected to the primary side

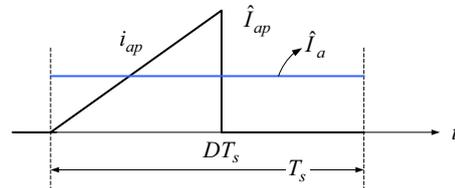


Fig. 4. The waveforms of transformer primary current (i_{ap}) over a switching cycle and its cycle based average (\hat{I}_a)

Fig. 4 shows the primary current and its cycle based average. The average of the primary current at this specific time (when v_{an} is at its peak) gives the magnitude of the sinusoidal current drawn from the utility line, which is \hat{I}_a . Therefore, the area of the triangular in Fig. 4 gives this maximum.

$$\hat{I}_a = \frac{1}{2} \hat{I}_{ap} D \quad (1)$$

The peak of the primary winding current \hat{I}_{ap} in (1) is found using equation (2), where \hat{V}_{an} is peak input voltage, D is duty ratio of the switch, L_m is the magnetizing inductance of the flyback transformer, f_s is the switching frequency.

$$\hat{I}_{ap} = \hat{V}_{an} D / L_m f_s \quad (2)$$

Equation (3) gives the input real power per phase.

$$P_a = \frac{1}{2} \hat{V}_{an} \hat{I}_a \quad (3)$$

Using (1), (2), and (3), duty ratio of the switch can be derived as given by (4).

$$D = 2 / \hat{V}_{an} \sqrt{P_a L_m f_s} \quad (4)$$

The parameters D , L_m , and f_s in (4) are not specified and should be determined for a given P_a and \hat{V}_{an} . This is the step where a good design optimization is required. Selection of these parameters greatly affects the performance, size and the efficiency of the converter. After an optimum design is obtained, we go to the next important design step which is the design of the flyback transformer. The main criterion in the design of the transformer is to achieve the lowest possible leakage inductance. Equations (5) through (9) are used to determine the optimum core area A_{core} , the number of primary turns N_1 , and the air gap length l_g . Moreover, equating the volt-second area across the magnetizing inductance gives the value of the turns ratio of the flyback transformer. From Fig. 3, and assuming operation at the boundary of continuous current mode (CCM), the equation for the turns ratio becomes,

$$\frac{N_1}{N_2} = \frac{\hat{V}_{an} D}{(1-D)(V_o + 2V_D)} \quad (5)$$

where V_D is the diode voltage and V_o is the average output voltage.

$$\lambda_{max} = \frac{\hat{V}_{an} D}{f_s} = 2 \sqrt{\frac{P_a L_m}{f_s}} \quad (6)$$

$$N_1 A_{core} = \frac{\lambda_{max}}{B_{sat}} \quad (7)$$

$$L_m = \frac{N_1^2 \mu_o A_{core}}{l_g} \quad (8)$$

$$l_g = \frac{N_1^2 \mu_o A_{core}}{L_m} \quad (9)$$

Equation (6) gives the maximum flux linkage. Using (7), (8) and (9) in a spreadsheet program, an optimum core size, the number of primary turns, the magnetizing inductance value, and finally the air gap length are determined.

4. Design of the Converter Power Stage

This section presents the design of the converter based on the mathematical analysis performed in the previous section. The Mathcad software was used to determine the design parameters. The program uses the specifications given in Table 1 as the input data and provides results by simultaneously solving the equations derived in the analysis section. An optimum design, which is given in Table 2, is obtained by evaluating these results. The following paragraphs will discuss the criteria for the optimum design.

The first step in the design process is to specify the switching frequency. It is selected as 30 kHz since this value is high enough to allow small size of magnetic components and low enough to allow the use of new generation high speed discrete IGBTs. Next, we need to find the duty ratio of the switch.

Because the input voltage range is very wide, as shown in Table 1, the range duty ratio will also be wide. Using (4), this range is found between 33.74% and 67.76% for a magnetizing inductance of 150 μ H. Staying within this range is a design objective since anything beyond this range would make it difficult to obtain the desired performance from the converter. Therefore, the value of the magnetizing inductance was selected based on this criterion.

Table 1. The input and output specifications of the converter

Output voltage range	40-56 V
Nominal output voltage	48 V
Maximum output current	50 A
Output power	2000-2400 W
Output voltage ripple (pk-pk)	less than 100 mV
Input voltage range	132-220-242 V
THD of the input current	less than 5%
Power factor	unity
Efficiency	90%

Table 2. The summary of design parameters

Parameters		Value
Switching frequency	f_s	30 kHz
Magnetizing inductance	L_m	150 μ H
Duty ratio	D	33.74-67.76%
Flux linkage	λ_{max}	5 mWb
Primary number of turns	N_1	18
Secondary number of turns	N_2	2
Core area	A_{core}	785 mm ²
Air gap length	l_g	2.13 mm
Switch voltage	V_{sw}	852 V

The flyback transformer design is the most rigorous part of this project. Fig 5 shows the core assembly and the finished transformer. The U shaped core pieces made from Ferrite material is used to minimize the core losses at 30 kHz. Besides minimizing the losses, it is very important to obtain the lowest possible leakage inductance. To achieve this objective, the following was done in the design of the transformer.

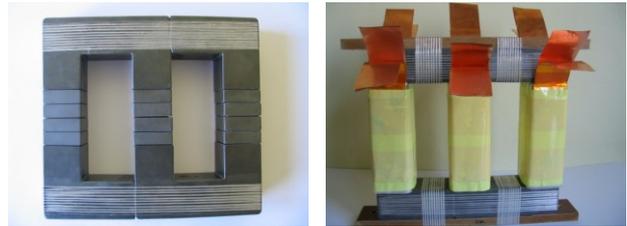


Fig. 5. The flyback transformer core assembly (left), the finished three-phase flyback transformer (right)

First of all, instead of using a single large air gap, which is 2.13 mm, we distributed the gap along the legs. As shown in Fig. 5, there are five air gaps along each leg. Besides providing the same magnetic properties and the energy storage requirements, the distributed air gap method significantly minimizes fringing and also contributes to the low leakage in the transformer. Second, we put the U pieces face to face to obtain a taller window area. In a taller window, escaping of flux from the upper and lower returns of the core sides is quite less. Then,

instead of using round conductors for windings, thinner but wider copper foils are used to minimize the space between the turns where the high leakage flux is generally present. Finally, secondary winding is sandwiched between the two primary halves in order to reduce to peak magnetic field intensity in the window; this technique significantly reduces the leakage inductance. A finished three-phase flyback transformer which provides the all design criteria is shown in Fig. 5. The total leakage inductance of the transformer is measured as less than 1%. Lastly, as seen from Fig. 5, even the leads of the windings are made using wide copper strips to minimize parasitic inductance between the transformer and the PCB connection points.

The EMI filters at the input use 300 μH inductors wound on an iron powdered toroidal core and 3 μF metal film EMI suppression capacitors. These components produce a corner frequency of 5.3 kHz.

As shown in Fig. 1, a bipolar switch is needed for the converter. From the analysis, it can be found that the switch will see maximum 852 V when switching transient voltages are ignored. To build the bipolar switch, one 1200 V high speed IGBT and 4 fast recovery diodes are used. Especially in flyback applications, the transient over voltages are always present and they are expected to be very high in magnitude due to the fast turn off of the IGBT. For that reason, using 1200 V device here seems risky, but a passive voltage clamp circuit will be used to protect the switches against transient over voltages. The clamp will be designed to fix the maximum switch voltage always below 1000 V to ensure the safety of the devices. SOT 227 package type devices will be used in order to shorten the paths for the current flow and therefore to minimize the parasitic inductances.

The three-phase rectifier at the output stage is constructed using 150 V Schottky diodes in SOT 227 package. Each package has two diodes in parallel. The low on state voltage of Schottky will contribute to the efficiency and again the paralleling is expected to reduce parasitics. As stated earlier, the current waveform at the output is highly discontinuous and has high RMS to average ratio. From the simulation studies, it was found that at nominal conditions when the average output current is 50 A, the RMS of the DC bus current is 114 A and the RMS of the ripple current flowing into output capacitor is 103 A. Therefore, 20 pieces of 200 V and 470 μF electrolytic capacitors with 6.45 A continuous current rating, which is based on 30 kHz ripple frequency and 55°C ambient temperature, are connected in parallel to handle 103 A. Table 3 lists the main semiconductors and the passive components used in the power stage of the converter.

Table 3. The list of the components used in the power stage

Part description	Manufacturer part number
IGBT	IXYS IXEN 60N120D1
Fred diode	IXYS DSEI 2x61-12B
Schottky diode	IXYS DSS 2x101-015A
Output capacitor	Kendeil K05200471_PM0CB

5. Design of the Control System

The most attractive characteristic of this converter is the very simple control requirements. As seen in the Simulink model of the controller system shown in Fig. 6, only a single-loop voltage-mode control technique is enough to do the control job.

The same PWM pulse is applied to the three switches of the three-phase converter. The controller here is capable of regulating a constant output voltage with excellent dynamics. Fig. 7 shows the details of the PLECs model of the power stage that is shown as a block in Fig. 6. Simulation was used to determine the controller parameters based on the dynamic response of the output. Since the PLECs model provides a real representation of the power stage during simulations, the mathematical model was not needed for control development. The control algorithm was then implemented in a microcontroller. For this job, we used 16-bit dsPIC30F2020 digital controller from Microchip Technology Inc.

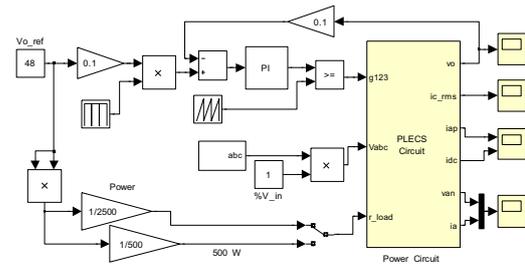


Fig. 6. Simulink model of the control system

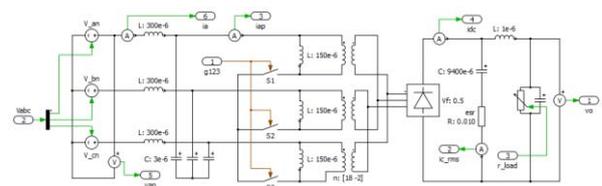


Fig. 7. The PLECs model of the power stage

6. Experimental Results

Fig. 8 shows the experimental setup of the converter system and the test arrangement. To monitor and evaluate the system performance, we used precision meters such as a 3193 HIOKI power analyzer that has 0.1% reading accuracy, and a TPS2024 Tektronix scope to capture waveform information. Fig. 9 shows the experimental waveforms of the voltage and the current drawn from the utility line of one phase. Fig. 10 is the screen copy of the power analyzer and lists all the important input and output parameters, where $U_{1,2,3}$ reads the utility line-to-neutral voltages, $I_{1,2,3}$ reads the utility line currents, P_{123} and S_{123} are the total three-phase real and apparent power, respectively. Then, in the same screen, U_4 reads the average output voltage, I_4 is the average output current, and P_4 is the real power measured at the output stage. Finally, λ_1 is the power factor, ϕ_1 is the power factor angle (phase shift between the voltage and the current), U_1 is the THD of the utility voltage, I_1 is the THD of the utility current, and η_1 reads the overall efficiency of the converter.

The current waveform in Fig. 9 clearly demonstrates the capability of the converter in realization of sinusoidal current with very low distortion plus a power factor very close to unity. As also shown in Fig. 10, the THD of the current waveform is 1.75%, which is well below what regulations state [1], and the power factor is 0.9981. The 3.53° phase shift here is due to the input EMI filter and it is not because of the converter operation. Finally, the efficiency of the converter is measured as 86.85%, which is around 3% less than the design objective of 90%.

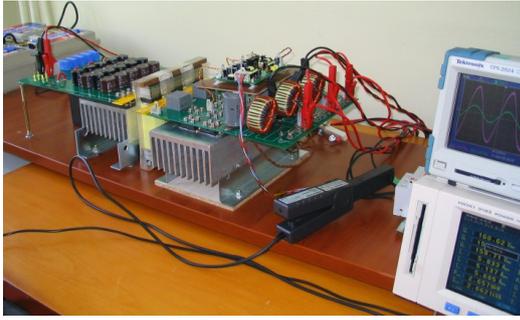


Fig. 8. The experimental setup of the implemented converter

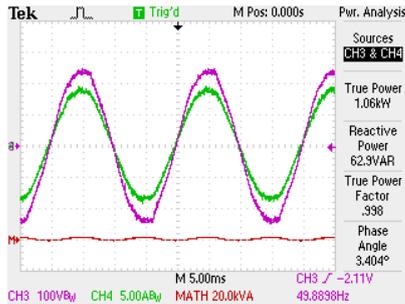


Fig. 9. The experimental waveforms of the utility voltage (purple) and the current (green waveform)



Fig. 10. The experimental results of the converter

7. Conclusions

This paper has presented the design and the experimental verification of a three-phase high power quality single-stage telecom rectifier. The main objective was to implement a commercially competitive solution to multistage and complex converter structures in the rectifier applications. In the design process of the converter, advanced design tools and techniques were employed to achieve the though design objectives.

In conclusion, the test results demonstrate that the converter satisfactorily achieves the input current harmonic and the power factor requirements. But, the overall efficiency is measured a little lower than expected. However, the distinct advantages such as low cost, nearly zero harmonic emission to the utility lines, a power factor close to unity, small size, and very simple control requirements make the topology attractive for commercialization.

8. Acknowledgements

This project is supported by the Scientific Research Project Fund of Eskisehir Osmangazi University (PN 200715043). The

author also would like to thank Arda Yesil, N. Nihat Ozturk, and A. Ihsan Yalap for their great help in the project.

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