Volume and Efficiency Optimization of a Step-down DC/DC Converter Based on F-L-N Parameters

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Abstract

In the design process of a practical power converter, a designer considers not only the electrical input/output performance criteria which the converter is supposed to meet, but also efficiency and overall volume. Mostly, factors that strongly affect efficiency and converter volume such as choice of switching frequency (f) and the amount of inductance (L), are solely selected depending on the designer's former experience and/or widely accepted rules of thumb, without any serious calculation. This study aims to show an efficiency and volume optimization based design process of a 1 kW step-down dc/dc converter. Effects of changing f and L value on system's overall efficiency and volume will be shown and an optimum design point will be reached. Also the phase number (N) is considered as an optimization parameter.

1. Introduction

Today's power converters are expected to have high efficiency and high power density while accomplishing stringent criteria set for electrical performance (low ripple, low noise, fast dynamic response etc.). For a commercial converter, robustness, reliability and cost are also very fundamental design aspects that cannot be overlooked. A designer must carefully select proper topology, mode of operation, switching frequency, cost effective electrical components (semiconductor switches, inductors and capacitors) which vary in price, volume and material that they are made of, while maintaining aforementioned indicators of quality. Therefore, converter design is a multi-dimensional problem, every element of which is affected by the change in the other elements.

It is often left to the designer's previous experience or widely accepted norms to decide on the selection of switching frequency (f) and inductance value (L). However, such an approach will most likely yield a result less than the optimum solution: it is beneficial to consider most, if not all, possible choices of design parameters for an optimized solution. Fig. 1 is a simplified illustration of a converter design process where the efficiency and power density are main concerns. Once the topology and mode of operation are selected for a specific application, there are several decision points most of which are also dependent on each other.

Having in mind that all converter design processes have their own unique restrictions and concerns depending on the application of interest, one general formula or set of rules cannot be defined to govern all possible kinds of converter design. Therefore, a 1-kW hard switched, non-synchronous step-down (buck) converter with continuous conduction mode of operation is selected as the design goal based on which efficiency and volume calculations will be carried out for this study. Effect of changing f and L values on converter's efficiency and volume will be studied. Interleaving technique is also considered (N phase system): same analysis will be run for both single phase structure (no interleaving) and multiphase (2, 3 and 4 parallel phases) structure in which each parallel phase processes a portion of total power. Examination of the effect of interleaving on converter efficiency and volume may also serve the task of phase number optimization.
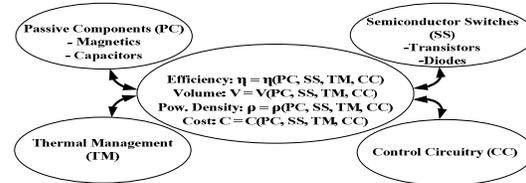
Fig. 1. Conceptual power electronic converter design optimization diagram showing the interdependency of design parameters

Similar efficiency and power density oriented converter optimization approaches can be found in the literature [1]-[5]. Different optimization techniques are introduced and their effectiveness is compared in [1]. There also are similar studies focusing on different converter topologies like phase shift PWM [2], flyback converter [3] and interleaved boost converter [4]. An efficiency optimization study targeted for MHz frequency range low power on-chip Buck converter applications is reported in [5].

2. Descriptions on the Approach for Optimization

2.1. General Converter Specifications

1-kW hard switched, non-synchronous buck converter example which forms the ground for the efficiency and volume analysis to be carried out, has 56 V input (18A) and 28 V output (36 A). The frequency range is swept between a minimum value of 25 kHz and a maximum value of 150 kHz, and its impact on efficiency and volume optimization is evaluated. The inductance value is also varied between a minimum that corresponds to 30% peak to peak current ripple (10.8 A) and a maximum that corresponds to 10% peak to peak (3.6 A) current ripple. Note that these minimum and maximum inductance values are also dependent on frequency.

A mosfet is assumed as the main switch which is accompanied by a schottky diode for freewheeling.

2.2. Inductor Design

Since the study of converter efficiency and volume optimization requires examination of various inductors, it is convenient to determine a fixed core material type and geometry such that all the inductors that will be used in efficiency and volume calculations are made of same core type and material with different sizes and number of turns. Toroid sendust powder core family introduced by Magnetics® under the name "Kool μ" is selected. The main optimization program includes an inductor design module, which designs an optimal inductor at each step as the inductance, frequency and current rating values are swept by the main optimization program. Necessary inductor related parameters required by the analysis such as inductor core and winding losses, temperature rise and total volume of the designed inductor are also calculated and fed back. The flowchart of the inductor design module is shown in Fig. 2. The inductor design program starts with core model 0077059A7 which has volume 1.8 cm^3 and relative permeability 60, and increases its physical dimension proportionally by 2% at each step if the current size of the core is not sufficient for target inductor design values.
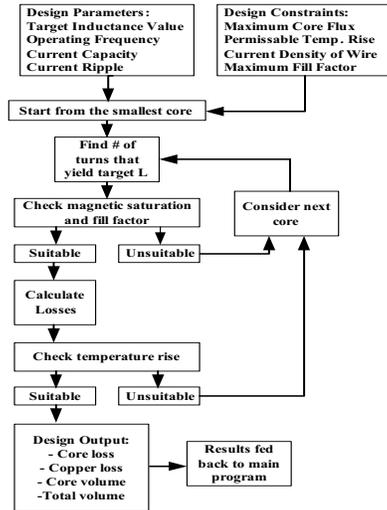
Fig. 2. Flowchart diagram of the inductor design program

Expressions for inductance and magnetic flux density for a toroid core are given in (1) and (2). As shown in the roll-off curve of Fig. 3, magnetic permeability values of sendust powder cores are heavily degraded with increasing DC bias. This characteristic is modeled in (3), where a, b, c and d are constants that depend on the initial permeability of core and T is the value of ampere turn value applied. Therefore, (1)-(3) must be considered together to find the number of turns which yields the target inductance value. AC flux swing and temperature are two other factors that affect permeability. But, they are omitted from the analysis since their effects are minimal (less than 1-2%) for the design constraints set.

$$L = (N^2 . A) / (l / \mu) \tag{1}$$

$$B = (N . I) / (l / \mu) \tag{2}$$

$$\mu(p.u) = a + b.T + c.T^2 + d.T^3 + e.T^4 \tag{3}$$
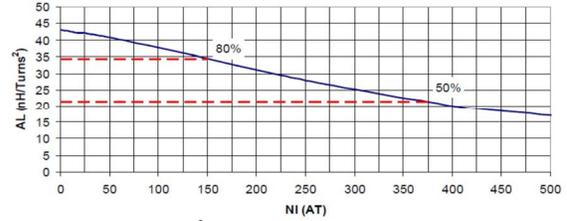
Fig. 3. nH/Turns^2 roll-off characteristics of the sendust core 0077059A7 with respect to the increasing DC bias

After the required number of turns to reach the target inductance is calculated, the inductor design program confirms that the roll-off in N.I is smaller than that of 50% (guarantees that the magnetic saturation is avoided). Next, temperature rise is considered. First the winding ohmic losses are calculated. Although its contribution is small for the frequency range of interest, skin effect is considered throughout the analysis yet proximity effect is omitted. Core loss is calculated (4) by the multiplication of core volume and core loss density formula (5). Note that B and f stand for magnetic flux density ripple and operating frequency respectively and the terms marked as K, α, β are constants depending on the initial permeability which are equal to 193, 2.01 and 1.29 respectively for μ=60 case. Finally, the temperature rise (ΔT) due to the losses (core and winding losses combined) occurring in the inductor is calculated via (6) and the result is compared to the preset allowable temperature rise value. If the criterion is met, design process is complete and the inductor design program feeds the necessary parameters back to the main optimization program.

$$P_{CORE} = P_{CORE.DENS} . V_{CORE} \tag{4}$$

$$P_{CORE.DENS.} = K . B^\alpha . f^\beta \ (mW \ / \ cm^3) \tag{5}$$

$$\Delta T (°C) = \left(\frac{P_{CORE} + P_{WND} (mW)}{Area(cm^2)} \right)^{0.833} \tag{6}$$

2.3. Converter Semiconductor Loss Modeling

For the buck converter with the given specifications, the main semiconductor losses are conduction and switching losses. Relatively small loss mechanisms namely gate drive losses and losses that stem from mosfet output capacitance are also included in the analysis. Diode reverse recovery phenomena is not taken into consideration since a schottky type diode was assumed. Expressions for loss calculations are given in (7)-(11). A constant 2W loss is assumed for the representation of power consumed by control and logic circuitry. For the analysis, all mosfets are assumed to turn on and off with 300 A/μs rate that makes turn on and turn off times depending on the current value they switch. The total semiconductor losses are given in (11) as P_{ST}.

$$P_{SW} = (1 / 2) . V . I . (t_{on} + t_{off}) . f \tag{7}$$

$$P_{COND} = I_{rms}^2 . R_{on} \tag{8}$$

$$P_{GATE} = Q_{GATE} . V_{DRIVE} . f \tag{9}$$

$$P_{COSS} = (1 / 2) . C_{OSS} . V_{IN}^2 . f \tag{10}$$

$$P_{ST} = P_{SW} + P_{COND} + P_{GATE} + P_{COSS} \tag{11}$$

2.4. Volume Considerations

A converter's volume depends not only on the components used but also on the PCB design, spacing between sub-

systems and packaging. Therefore, a strict estimation of overall converter volume is impractical. In this study, the term "volume" corresponds to heat sink ($V_{H.S}$) and magnetic volume (V_L) combined (12), as these are the two basic components that dominantly determine converter volume for the design example. Effect of changing f and L on the converter volume is analyzed through variations in heat sink and magnetic volume. Magnetics volume is given by inductor design program and a heat sink volume is calculated (13) from the total semiconductor losses (P_{ST}) with the assumption that the required heat sink volume is 1.5 cm³/W (k=1.5).

$$V_{TOT} = V_{H.S} + V_L \qquad (12)$$

$$V_{H.S} = k.P_{ST} \qquad (13)$$

2.5. Approach for Comparison: Equal I - Equal L

For an electrical component, effective series resistance (or Rds_{ON} for a mosfet) decreases as the current rating increases. Therefore, assuming components with same ESR values for both single phase and interleaved cases for an efficiency comparison, corresponds to comparing single phase structure with current rating I_{rated}, to interleaved structure with current rating $N.I_{rated}$, favoring interleaving. For a fair comparison, ESR values for components are assumed to increase proportionally with increasing number of phases. Same inductance values are taken into consideration for different number of phases. This approach developed for the analysis is named "equal current rating – equal inductance approach". For the 1kW converter example, the selected semiconductor parameters for loss calculation are listed in Table I. (Note that mosfet output capacitance (C_{OUT}), and mosfet gate charge (Q_{GATE}) increases with increasing current rating).

Table I. 1kW converter power semiconductor parameters

N	Rds_{ON} (mΩ)	V_F (V)	R_{DIODE} (mΩ)	C_{OUT} (pF)	Q_{GATE} (nC)
1	10	0.6	4	800	144
2	20	0.6	8	400	72
3	30	0.6	12	266	48
4	40	0.6	16	200	36

3. Analysis on the Effect of f, L and N on Converter Efficiency and Volume

3.1. Outputs of the Analysis

In view of the descriptions and assumptions made thus far, a MATLAB code, flow chart diagram of which is given in Fig.4, is written to generate efficiency (at full/rated load) and volume graphs for varying N, f and L. Efficiency versus L and f axes can be seen on Fig. 5.a for various N. Variation of total volume is also analyzed and can be seen on Fig. 5.b.

In addition to the efficiency and volume analysis introduced, a figure of merit (FoM) for the converter is defined (14) to represent the optimum design point. $V_{TOT,MAX}$ and $P_{L,MAX}$ expressions stand for the maximum total volume and loss values encountered in the analysis which are 282.48 cm³ and 64.33 W respectively. By comparing each f, L pair's corresponding loss (P_L) and volume (V_{TOT}), FoM can be defined for the converter under examination. Variation of FoM can be seen on Fig. 5.c.

$$FoM = \frac{P_{L,MAX}.V_{TOT,MAX}}{P_L.V_{TOT}} \qquad (14)$$
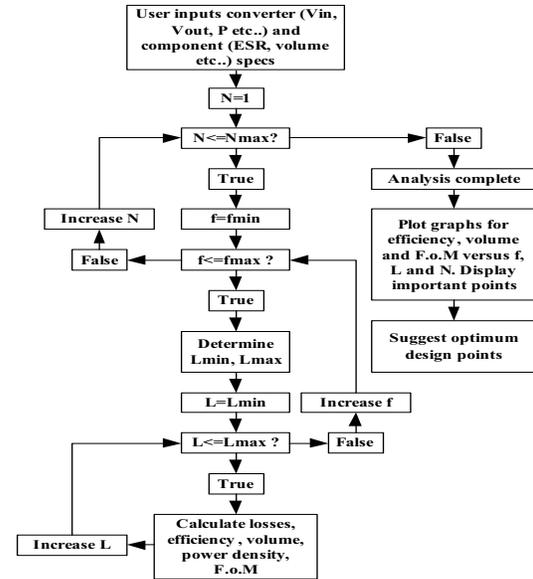
Fig. 4. Flowchart diagram for the program written for the efficiency and volume optimization analysis
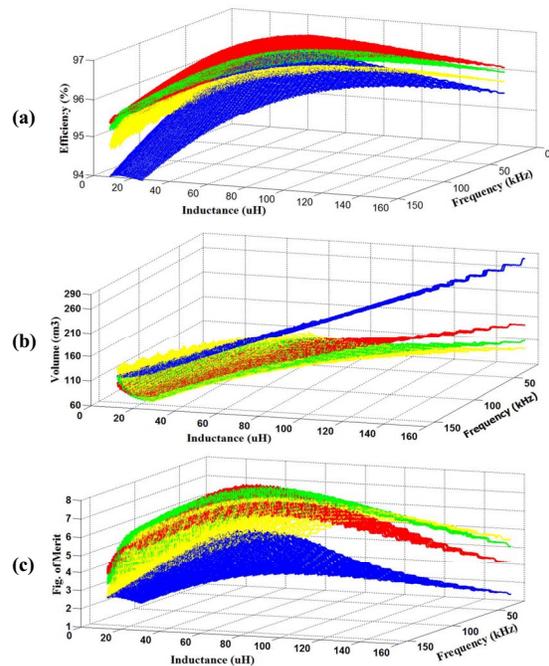
Fig. 5. Efficiency (a), volume (b) and FoM (c) as a function of f and L with N parameter. Single phase structure (N=1, blue) and interleaved structures: (N=2, red, N=3, green, N=4, yellow)

Although visualization tools serve the purpose of showing an overall picture of change in the observed quantity with respect to the variables being changed, it may be hard to observe critical design targets such as maximum efficiency or minimum volume points. Therefore Table II is created to summarize those important points.

Table II. Design extrema and their parameters

N	Quality	Eff. (%)	V_{TOT} (cm³)	V_L/V_{TOT} (%)	FoM	f (kHz)	L (µH)
1	Max. Eff.	96.35	123.14	67.88	3.90	26	50.86
	Min. Eff.	93.96	123.00	31.39	2.30	150	25.75
	Max. Vol.	95.64	282.48	86.22	1.41	25	154.50
	Min. Vol.	95.79	86.83	41.69	4.47	65	20.34
	Max. FoM	96.17	97.84	53.12	4.67	43	30.14
2	Max. Eff.	**96.75**	84.78	63.60	6.38	29	54.63
	Min. Eff.	95.36	99.73	45.37	3.74	148	8.76
	Max. Vol.	96.34	146.81	79.74	3.26	26	148.46
	Min. Vol.	96.34	69.92	40.23	6.86	90	26.33
	Max. FoM	96.61	71.59	49.83	7.25	57	31.47
3	Max. Eff.	96.47	72.50	56.44	6.87	42	62.04
	Min. Eff.	95.18	113.13	56.53	3.17	147	8.99
	Max. Vol.	95.27	113.56	56.32	3.23	150	8.81
	Min. Vol.	96.25	64.46	38.35	7.26	100	35.48
	Max. FoM	96.40	65.85	44.87	**7.39**	71	40.75
4	Max. Eff.	96.17	68.02	48.42	6.71	53	67.44
	Min. Eff.	94.68	129.56	62.02	2.50	146	9.05
	Max. Vol.	94.82	134.60	63.35	2.47	147	8.99
	Min. Vol.	96.02	**63.08**	36.58	6.96	106	36.19
	Max. FoM	96.11	63.72	40.78	7.07	82	47.10

3.2. Examining the Overall Converter Behavior and Target Design Points Under Varying f, L and N

The study results clearly demonstrate the importance of an efficiency and volume based analysis before the implementation of a converter: there exist different values of f and L which correspond to basic design goals like minimization of losses and volume or both (FoM maximization). General rules of thumb such as increase in switching frequency decreasing the passives' hence converter's overall volume and interleaving technique's volume reduction effect can be observed throughout the analysis. On the other hand: following aforementioned rules of thumb without any calculation of loss and volume with respect to varying parameters can lead the designer unexpected design outcomes such as a higher frequency converter which results in a bigger volume.

3.2.1. Examining the Results in View of Efficiency

While varying f, L, and N in the 1-kW hard switched buck converter example, efficiency changes between a maximum of 96.75% (which occurs for the maximum efficiency point for N=2 case) and a minimum of 93.96% (which occurs for the minimum efficiency point for N=1 case). Corresponding change in loss is 33.63 and 64.33 W respectively. Since "equal current rating-equal inductance" approach is adopted and conduction losses are dominant in the design example, a wide difference in the efficiency values is not observed. The factors creating difference in efficiency analysis can be stated as switching losses, inductor losses and the effect of current ripple in each phase. It was assumed that switches turn on and off with 300 A/µs. Under that assumption interleaving results in lowered switching losses but rate of reduction in losses decrease with increasing number of phases. For interleaved converters, it should also be noted that every single phase of the converter experiences the same current ripple of the non-interleaved converter. This yields additional conduction and inductor losses.

3.2.2. Examining the Results in View of Volume

From the converter optimization program's outputs, it can be observed that increase in f has volume reduction effect up to 60-100 kHz band (depending on number of phases), above that band there is no gain in volume with increasing f due to the fact that little or no volume reduction is accomplished in inductors compared to the increase in heat sink volume because of the increased switching losses. Note that volume value at 150 kHz for N=4 case is even larger than the value at 25 kHz. From Table II and Figures 5-7 it can be seen that interleaving both boosts efficiency and volume but that boosting effect quickly saturates for the converter example under consideration: volume and efficiency results for two and three phases are very close, four phase operation is worse, yet still better that single phase operation. Figure 6 shows the variation of volume with respect to L at 25, 85 and 150 kHz f values for N=1.
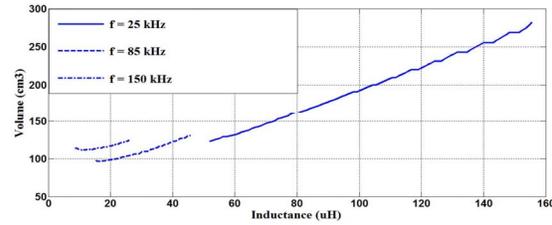
Fig. 6. Total volume versus inductance graph for N=1

Fig. 7.a-b show total volume versus f when ripple is kept constant at 3.6 A (a) and 10.8 A (b) respectively. From Fig. 7.a, volume reduction benefit of interleaving and the decrease in rate of reduction can be observed. Fig. 7.b corresponds to minimum inductance - maximum current ripple hence maximum core loss case and shows that there occurs a volume reduction when phase number is two but as phase number is increased, volume increases even beyond single phase structure. This is due to the fact that all phases experiencing large amount of current ripple under high frequency yields serious core losses, which requires larger cores since all the inductors are designed to satisfy same thermal limit.
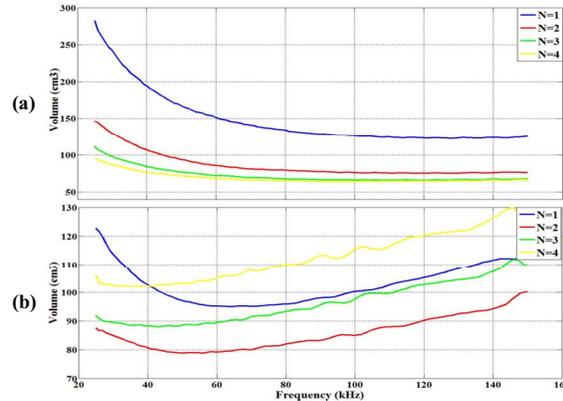
Fig. 7. V_{TOT} vs f graph for ΔI=3.6 A (a) and ΔI=10.8 A (b)

Examining inductor core and winding losses separately further explains results of Table II and Fig. 7.a-b. In Fig. 8.a-b, total core and winding losses are given for N=1 and N=3 cases for minimum and maximum current ripple situations respectively. As the frequency is increased and a large ripple

in current hence core magnetic field is allowed, core losses have profound effect. Combining that with N, total inductor losses for multi-phase converter can exceed single phase converter inductor losses. Although it seems reasonable to drastically decrease L in a multi-phase buck converter, relying on the ripple cancellation property of interleaving, the resulting multi-phase converter may lack its single phase counterpart in terms of both efficiency and volume while the designer expects just the opposite situation.
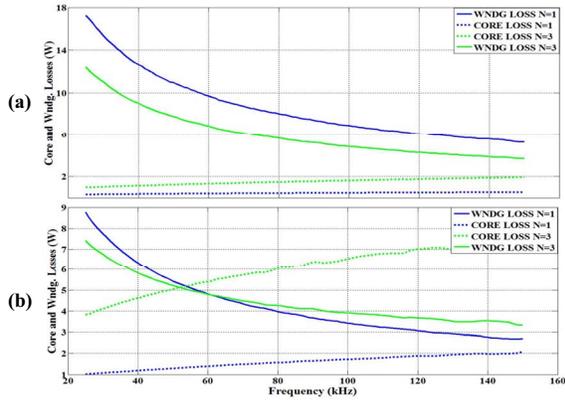
Fig. 8. Core and winding losses versus frequency for $\Delta I = 3.6$ A (a) and $\Delta I = 10.8$ A (b) cases

3.2.3. Optimum Design Point with FoM Comparison

A FoM was defined which equals the multiplication of gains in volume and efficiency so that it promotes more efficient converter in a small volume. Depending on the characteristics of the application, a designer may promote some properties of the converter above others but from a general point of view, FoM maximization can be considered as the optimum design point. According to the FoM definition set for the analysis, optimum design point turns out to be: (f, L, N) = (71 kHz, 40.75 µH, 3) which yields 96.40% efficiency in 65.85 cm^3 volume. Narrowing the analysis' results down to N=3 case, it is seen that design points for maximum efficiency, maximum FoM and minimum volume converge. Comparing maximum FoM point to minimum volume point shows that 2% volume reduction is possible with the price of 4% increase in loss. Similar comparison of maximum FoM and efficiency suggests that 2% reduction in losses is possible with increasing volume by 12%.

The results introduced in Table II can give an idea about cost. Since semiconductor switches' overall current rating is kept same for all N and volume is analyzed through heat sink and inductance volumes, variations in cost are proportional to variations in volume. Also, considering sendust core having a higher $/cm^3 ratio compared to heat sink, V_L/V_{TOT} column of Table II suggests minimum volume and maximum FoM points as lower cost solutions compared to maximum efficiency points. For more comprehensive cost analysis, components such as sensors, gate drive and control circuitry etc. could also be considered to further extend the accuracy.

The analysis and its outputs can also be viewed as the answer of whether or not a designer should employ interleaving technique. Interleaving turns out to be beneficial in terms of both efficiency and volume for the converter example defined therefore utilization of interleaving is advised. Results tabulated in Table II may serve the task of

phase number optimization once interleaving is adopted. Maximum FoM value is obtained for N=3 therefore from a maximum efficiency and minimum volume based design goal, optimum number of phases can said to be three for the 1-kW buck converter examined. A designer can choose the minimum N value that best satisfies the FoM defined, or at least can have an intuition about optimum point for phase number, looking at the efficiency and volume graphs for varying N. A similar efficiency based phase number optimization is reported in [7]. Another benefit introduced by interleaving is the "dynamic number of phases" ability: it is common practice to shut down some of the parallel phases under light-load conditions to obtain a flat efficiency curve as load current varies. Fig. 9 shows load current versus efficiency graph of maximum FoM point with active phase number being reduced with decreasing load current. It is seen that by the application of "dynamic number of phases" approach, flattening the efficiency curve and obtaining higher efficiencies under light load conditions is possible.
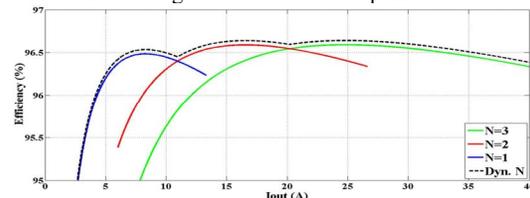
Fig. 9. Efficiency for max. FoM point under varying load current

4. Conclusion

Effect of choosing different f and L values on converter efficiency and volume is shown on a buck converter example. Effect of interleaving, considering two, three and four parallel phase structure is investigated and shown to be beneficial in terms of efficiency and volume. Results show that, for the converter example under examination, an optimum point can be found which tries to set both efficiency and power density high as possible. The need of such an analysis for any converter's design is highlighted. Although the analysis was conducted for a specific converter type and set of conditions, the concept is general and can be followed to pursue an optimal design for any type of converter with its own set of conditions.

5. References

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