Unity Power Factor Isolated Bridgeless Rectifier Based on Coupled Inductors

Seyed Hossein Hosseini¹, *Member, IEEE*, Soheil Nazemi²

¹ Islamic Azad University, Tabriz Branch, Tabriz, Iran

² Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran

hosseini@tabrizu.ac.ir, s.nazemi86@ms.tabrizu.ac.ir

Abstract

In this work, a unity power factor rectifier based on coupled inductors is presented. Use of coupled inductors has obtained galvanic isolation between AC and DC sides. Suitable switching pattern based on PWM, makes possible unity power factor operation for this rectifier. The proposed rectifier has a symmetrical configuration which any halves acts on one half cycles. This configuration uses minimum number of power electronics elements, no conventional diode bridge, two switches (IGBT) and two blocking diodes. The proposed rectifier uses two simple controls and supplies a dc load on low voltage and high current. The simulations have been executed on PSCAD/EMTDC demonstrate its results and practicability.

1. Introduction

In recent years, the growth in the use of electrical equipment has resulted in more stringent international standards and utility requirements to ensure that the line current harmonic content of the equipment connected to the ac mains is limited [1]. These harmonics can be significantly reduced if the input power factor is corrected by shaping the input current in each of the three phases so that it is sinusoidal and in phase with the phase voltage. Due to this fact, switch-mode rectifiers for power factor correction have gained considerable attention. Other reasons for the use of power factor corrector (PFC) rectifiers are their adaptability to different line voltages and the fact that they preregulate the dc output voltage, which may be supplying a dc-dc converter [2]. To reduce the harmonics, one of the most widely used methods is the boost topology operating in continuous conduction mode (CCM) followed by a dc/dc converter. It shows good performance such as high power factor and fast output-voltage regulation but increases cost and size due to additional semiconductor switches and control circuitry [3], [4]. Another approach is the single-stage method, which combines the harmonic regulator with dc/dc converters into one stage [5]. These converters inherently draw a high-quality line current waveform through discontinuous conduction mode (DCM) operation and have a single control loop to regulate an output voltage. Although it has simple structure, this approach has an undesirable feature. This is because only a single control loop exists for the output-voltage regulation, and the link voltage is determined by the input-to-output charge balancing [6], [7]. Most single-stage converters suffer from this problem, which makes it difficult to use single-stage converters for the applications that require a universal input voltage of 90-265 Vrms. To overcome this disadvantage, several concepts have been suggested. The first one is the variable switching control method, but it has problems such as low conversion efficiency

and/or difficulty in the optimal design of the filter and inductor [8]. Other possible approaches are using magnetic feedback [9], [10] and parallel power processing [11], [12]. They can be applicable to converters with wide input-voltage ranges but still show high voltage stress and/or complex circuit structure [13]. In often rectifiers, there is a conventional diode bridge before any switching and/or current shaping stage. An instance of these types recently proposed by Lee in [7] and has been showed in "Fig. 1" includes four main parts, is commenced by a LC filter and continued by a diode bridge, proposed flyback topology and finally the energy storage capacitor. In this paper, a simple rectifier has been proposed with some prominent merits like being bridgeless. Very often proposed bridgeless rectifiers have been implemented a boost type circuit configuration (also referred to as dual-boost PFC rectifiers) because of their low cost and their high performance in terms of efficiency, power factor and simplicity. A simplified schematic of the conventional bridgeless PFC boost rectifier is shown in "Fig. 2". Although the bridgeless boost rectifier is very simple and popular, it has the same major practical drawbacks as the conventional boost converter. These drawbacks are that the dc output voltage is always higher than the input voltage peak, input-output isolation cannot be easily implemented, high startup inrush current, as well as a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages, such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier [14]. Moreover, the proposed topology demonstrates other capabilities like electrical isolation between line voltage and load, unity power factor, low harmonic (THD) on drawn current, reduction of line current THD as well as parallel filter (active or

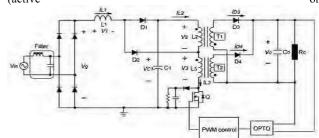


Fig. 1. A traditional primary rectifier

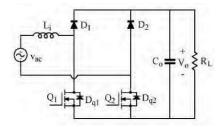


Fig. 2. An unisolated bridgeless UPF rectifier

passive), constant DC output voltage for vide range of input voltage variation and finally independency of drawn current from input voltage waveform and amplitude. On obtaining smooth output voltage, two control strategies used for switching pattern generation, one faster path for drawn current control and a slower feedback loop from output DC voltage. The simulation has been executed for a 100 W instance on 220 V of line voltage with a 35 percent of peak diminution. This circuit has a symmetrical configuration, one half of that operates on positive half-cycle and the other one on negative half-cycle of line voltage. For any half-cycle a power switch with off ability is implemented and has been shown in "Fig. 3" as Q1 and Q2. As seen in "Fig. 3" for any operating mode, one or two power electronics element passes the current and at major part of any duty cycle just one element suffers the appropriate current that can be the switch or the diode in load side $(D_1 \text{ or } D_2)$. This type operation results in low conduction losses and lower costs. On achieving unity power factor, PWM switching function is used but unlike its tradition, duty cycle isn't constant and varies by line voltage amount at any sampling moment. . Unlike conventional control manners that use drawn current sampling for their arithmetic and logical processing, in this proposed control strategy, independent of drawn current, line voltage peak and line voltage waveform, hasn't been used any current sensors and instead of them a sample and hold unit operates on line voltage. Operational principles and modes of proposed rectifier are presented in 2, control strategies in 3 and simulation results in <u>4</u>.

2. Operational Principles

The proposed rectifier is depicted in "Fig. 3". Its operation is based on flyback action of the coupled inductors and freewheeling diodes. Two coupled inductors pair are paralleled in secondary side and are contributed to output capacitor

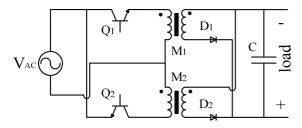


Fig. 3. Proposed UPF isolated bridgeless rectifier

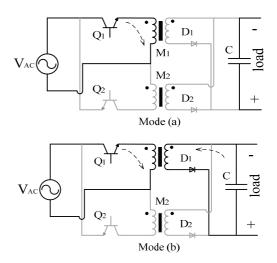


Fig. 4. Operating modes, (a) mode (a), (b) mode (b)

charging. As seen in "Fig. 4(a)" to "Fig. 5(b)", there are four operating modes for any half cycles. This converter receives and delivers power in discontinues conduction mode (DCM) on its both sides. For first operating mode, Q₁ switches on and stays for an online calculated duty cycle (K) part of the constant switching period (T). The current rises up from zero to a predefined value as seen in "Fig. 4(a)". This value of current is calculated in control unit and is a function of power rating of the given DC load (or next inverter). In this mode Q₁ switches on under Zero Current Switching (ZCS) conditions but not under Zero Voltage Switching (ZVS). At start of mode (b), Q1 switched off and current decreasing in line side inductor forces D₁ to be on ("Fig. 4(b)"). This action as called freewheeling causes to Q1 switches off without current stress but a voltage stress begins to demonstrate on Q1 because of DC link voltage appearance on line side inductor and causes additional voltage stress. Of course this stress doesn't have major effect on switching losses in this mode but causes an additional voltage rating for switches in their off conditions which in secondary side that's related diode is on (mainly mode (c)). Nevertheless, time of this mode is shorter than other operating modes. As seen in "Fig. 5(a)" at mode (c), Q_1 is compeletly off, D_1 is on and the stored energy in magnetic field is transferring to DC link capacitor and the load. Along this mode, the current of load side inductor falls down to zero because of DC link voltage. By decreasing of D_1 current to zero, the last mode, mode (d) begins. As seen in "Fig 5(b)" for mode (d) both sides are in off state, ready for next switching cycle. As Q₁ switches on, the line side inductor current rises up in next switching cycle. At the end of mode (c) D₁ switches off under Zero Voltage and Zero Current Switching (ZCS & ZVS). The length of these modes can be variable depends on voltage amplitude variations or distortions of line voltage waveform. Along mode (a) diode D₁ that is in off state suffers an additional voltage stress because of appearance of a multiple (ratio of load side to line side coils turns, like transformer turn ratio) of line voltage in DC voltage (low voltage) side, causes additional voltage rating. Exactly like these operating modes there is for other elements (Q2, D2 and

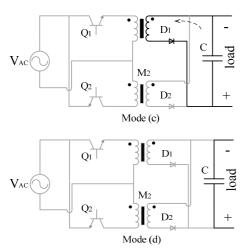


Fig. 5. Operating modes: (a) mode (c), (b) mode (d)

M₂) at line voltage negative half cycle. In this structure like other flyback converters, at mode (a) line voltage deals with a bigger inductance indicated as (1) and along mode (b) deals with a lower inductance indicated as (2).

$$L_H = L_I \tag{1}$$

$$L_L = L_I - M \tag{2}$$

For mode (a) and mode (b), "Fig. 6(a)" and "Fig. 6(b)" respectivly are their models. These models certify (1) and (2). At mode (a) input voltage deals with a constant inductance as indicated in (1), results in Q_1 switches on under ZCS. As seen in "Fig. 6(a)" in DC side the current is suppressed by D_1 and as said above, in AC side the line voltage deals only with a uncoupled inductance (L_H). As seen in "Fig. 6(b)", at mode (b) Q_1 begins to be off, its current and AC side coil magnetic flow decrease, D_1 begins to be on and DC side current and magnetic flow increase. But the current increasing in AC side coil retains stored energy in magnetic field. As indicated in (3) in linear circuits, for an almost constant magnetic flow at a certain time and for a given currents I_1 and I_2 , by decreasing of the portion of AC side flow (L_1I_1) and increasing of the portion of DC side flow (L_1I_1) in total (linkage) flow, as indicated in (2) in fact I_1

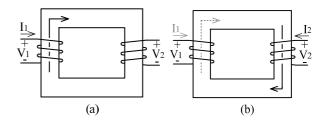


Fig. 6. Coupled inductors models: (a) model of mode (a), (b) model of mode (b)

deals with a lower inductance that results in fast and low stress current falling and near to ZCS switching at beginning of mode (2).

$$\lambda = L_1 I_1 + M I_2 \tag{3}$$

In load side, DC link voltage has similar conditions, in other word it deals with a higher inductance for mode (c) but at mode (d) because of DCM operation it doesn't experience the conditions like beginning of mode (b). As said above this specification is due to inductors pair coupling. Due to this, switches suffer lower losses because in mode (b) by lower inductance, switch current quickly falls down to zero and at commence of mode (a) higher inductance guarantees suitable ZCS. In (1 - 3), L₁ and M is respectively demonstrator of self inductance and mutual inductance.

3. Control Strategies

For this unity power factor rectifier a PWM control method is used but it is different from traditional ones together with a traditional PI controller. This is a PWM with a variable online duty cycle generated by control unit and uses online measurements on output DC link voltage and line voltage. In this manner instead of current sensing, a simple sample and hold unit is used for voltages sensing and measurement. expected a constant DC link voltage for a wide range of line voltage variations. One of the main merits of the proposed rectifier is its stable operation for distorted line voltage waveforms. Line voltage sensing has a quick dynamic on achieving an online duty cycle calculation and it's an open loop path but V_{out}

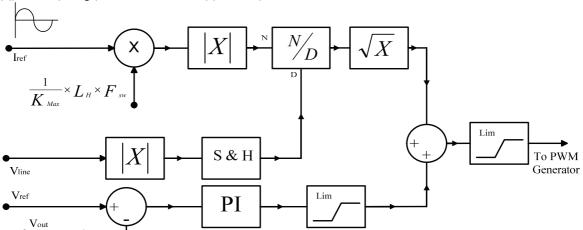


Fig. 7. Used control block diagram of proposed rectifier

feedback loop has a pretty slow response and its output adds on resultant duty cycle of aforementioned open loop. In this control method a low THD and unity power factor is expected.

In fact the open loop controller is used for quick calculations against line voltage distorted waveforms, in other words for this part of controller, the distorted sinusoidal waveform and pure one don't have not so difference. By high rate of sample per second of sample and hold unit, the calculated duty cycle for drawing a sinusoidal current from the line, is calculated for any value of voltage at that sampling time. This method doesn't inject any excessive harmonic for distorted sinusoidal line voltage but it has a compensatory effect on line current THD. The other part of controller uses a feedback from DC link voltage to participate in duty cycle calculation. The main effect of this part demonstrates in voltage falling or overvoltage conditions. The pretty high time constant of PI controller (about the line voltage period) provides a constant voltage on DC link without interference on the open loop controller. The PI controller dosen't have any sensible effect on operation of open loop part and its generated duty cycle.

4. Simulation Results

As said previously one of the prominent merits of the proposed rectifier is its constant output despite of line voltage variations. This specification is due to its control strategy. For a 10% overvoltage and 35% under voltage, these variations and output DC voltage are shown in "Fig. 8". In the case of both control loop operation, output and line voltages variation are shown in "Fig. 8(a)" and as a suitable response, output voltage stays constant. In other case only open loop controller is used and as seen in "Fig. 8(b)" output DC voltage has been shown lower percent of variations. In both cases, simulation results show the input current THD (in percent). At deferent modes of operation power electronics components, mainly switches, suffer some voltage and current stresses as seen in "Fig. 10". As seen in this figure current rising and falling slopes are different as expected because of flyback characteristic. Other main and vital merit of this rectifier like others is its unity power factor characteristic. For the complete controller the first harmonic of drawn current together voltage on varies conditions of line voltage amplitudes, as seen in "Fig. 11(a) – (c)" respectively for voltage falling, nominal voltage and overvoltage, that they certify the unity power factor operation of this rectifier.

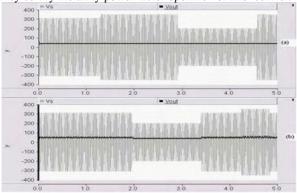


Fig. 8. Line and output voltages: (a) with complete controller, (b) only with open loop controller.

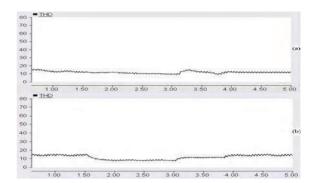


Fig. 9. Drown current THD (pu): (a) with complete controller, (b) only with open loop controller

For the open loop controller, the first harmonic of drawn current together line voltage are shown in "Fig. 12(a) - (c)" that respectively for voltage falling, nominal voltage shown in "Fig. 13" appears on input of proposed rectifier. Overvoltage conditions certify the unity power factor operation of the proposed rectifier. In fact the unity power factor of this structure is result of symmetry on its circuit and controller for positive and negative halve cycles of line voltage. As said above in section 3. For this open loop controller there is no difference between distorted and pure sinusoidal line voltage. Moreover as a result of this specification this rectifier according to its power rating, improves and compensates the line THD that has been issued from other nonlinear loads like conventional diode bridge rectifiers. The distortion caused by a conventional diode

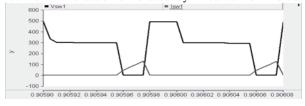


Fig. 10. Voltage and current (×10) waveform of rectifier switches

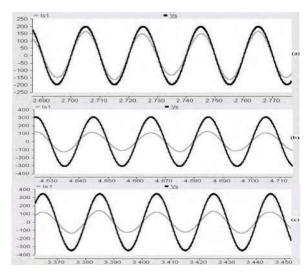


Fig. 11. Line voltage and first harmonic of drown current (×100) for complete controller: (a) voltage falling, (b) nominal line voltage, (c) overvoltage.

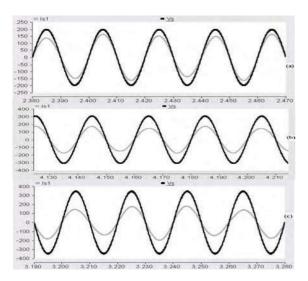


Fig. 12. Line voltage and first harmonic of drown current (×100) for open loop controller: (a) voltage falling, (b) nominal line voltage, (c) overvoltage

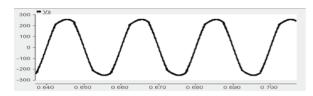


Fig. 13. Distorted line voltage caused by conventional diode bridges

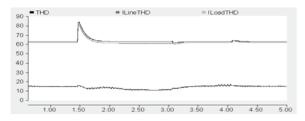


Fig. 14. THD compensation by proposed UPF rectifier: (light gray) conventional bridge diode current THD, (dark gray) line current THD after connection of proposed rectifier, (black) THD of proposed rectifier for a distorted line voltage

bridge as seen in "Fig. 14" for three states of voltage amplitude, THD of the drown current from line (dark gray) is decreased after connection node of this UPF rectifier rather than THD of drown current by conventional diode bridge (light gray) and the black THD related to proposed rectifier.

5. Conclusions

The proposed converter, as named, supplies a constant DC load for vide rang of line voltage in unity power factor conditions. Unlike traditional rectifiers it's not uses any diode bridge or other current shaping equipments. Its structure is simple, uses pretty simple and flexible controller, provides galvanic isolation between load and line, its switches operate under very close conditions to soft switching and draws current with low THD even for voltage falling. Moreover the proposed rectifier according to its power rating, improves line current THD for high THD

currnt drawn by nonlinear loads. Controller unit and operation modes has been described, simulation results are proposed to confirm expectancies.

7. References

- [1] IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power Systems, IEEE Std. 519, 1992.
- [2] A. A. Badin, I. Barbi, "Unity power factor isolated threephase rectifier with split DC-bus based on the Scott transformer," IEEE Transactions on Power Electronics, vol. 23, no. 3, May 2008, pp. 1278-1287.
- [3] L. Dixon, "High power factor preregulators for off-line power supplies," in Unitrode Switching Power Supply Design Seminar Manual. Merrimack, NH: Unitrode Corp., 1990, pp. 12.1–12.16.
- [4] M. H. Kheraluwala, R. L. Steingerwald, and R. Gurumoorthy, "A fastresponse high power factor converter with a single power stage," in Proc. IEEE Power Electron. Spec. Conf., 1991, pp. 769–779.
- [5] J. Y. Lee, G. W. Moon, and M. J. Youn, "Design of a power-factor correction converter based on half-bridge topology," IEEE Trans. Ind. Electron., vol. 46, no. 4, pp. 710–723, Aug. 1999.
- [6] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor corrected converter topologies," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 23–35, Feb. 2005.
- [7] J. Y. Lee, "Single stage AC/DC converter with inputcurrent dead-zone control for wide input voltage ranges," IEEE Transactions on Industrial Electronics, vol. 54, no. 2, April 2007, pp. 724-732.
- [8] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control," in Proc. IEEE Appl. Power Electron. Conf., 1994, pp. 569– 575.
- [9] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch, power factor correction (S4-PFC) AC/DC converters with DC bus feedback for universal line applications," in Proc. VPEC Seminar, 1997, pp. 29–35.
- [10] L. Yan and G. Moschopoulos, "A DC bus voltage reduction technique for single-stage AC–DC forward converters," in Proc. IEEE Appl. Power Electron. Conf., 2004, pp. 744–749.
- [11] J. Y. Lee, "Single-stage power factor correction converter with parallel power processing for wide line and load changes," Electron. Lett., vol. 38, no. 9, pp. 421–423, Apr. 2002.
- [12] W.Wu,W. Qiu, K. Rustom, S. Luo, and I. Batarseh, "Efficient high power factor single-stage AC/DC converter," in Proc. IEEE Power Electron. Spec. Conf., 2002, pp. 1143–1148.
- [13] K. Rustom and I. Batarseh, "Recent advances in singlestage power factor correction," in Proc. IEEE Ind. Technol. Conf., 2003, pp. 1089–1095.
- [14] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Transactions on Industrial Electronics, vol. 56, no. 4, April 2009, pp. 1147-1157.