# NEURAL NETWORK BASED TRANSISTOR MODELING AND ASPECT RATIO ESTIMATION FOR YITAL 1.5 MICRON PROCESS

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## ABSTRACT
The channel length and width of a MOSFET are two important parameters selected by the experience of the designer. In this work neural networks are used to decide the most suitable selection of channel length and width of MOSFET for both p-channel and n-channel transistors. Multi layer perceptron (MLP) decided the aspect ratio. Training and test data are obtained from HSpice design environment with YITAL 1.5 micron parameters.

## I. INTRODUCTION
The MOSFET channel length and channel width decision directly effects the current driving capability of the transistor [1]. Since the MOSFETs are modeled by too complex nonlinear equations, it is too hard to estimate and calculate the required channel length and width exactly. The input voltages are gate-source, drain-source, bulk-source potentials and the output is drain current for a MOSFET. Under constant input voltages, channel length and width parameters nonlinearly change the output current.

Supervised neural nets are good function approximators [2]. Therefore, they are suitable for prediction of transistor aspect ratios. If the applied input voltages and the drain current of a MOSFET are given to a neural network as inputs, the channel length and width can be estimated by the network.

Signal and noise behaviors of microwave transistors are modeled by MLP neural networks in [3], [4], [5], [6]. Small signal and noise behaviors are obtained using s-parameters modeling approach. Inputs of the neural networks are operation frequency vector, small signal input voltage, small signal output current and configuration type. The outputs are scattering and noise vector parameters. In all previous works analytical models are used to obtain the training and test data for the network.

Unlike the previous papers, in this work, the transistor is not modeled by scattering and noise parameters or small signal model. The training and test data are obtained from the simulation of n- and p-channel MOSFETs in HSpice environment. The level 3 transistor model is used with YITAL 1.5μ [7] process parameters. The aspect ratio elements were obtained by MLP neural networks. The input gate-source voltage and the drain current of the MOSFET were applied to the inputs of MLP and the outputs were channel length and width parameter values. Drain-source and bulk-source voltages are assumed as constants. The neural network directly models the transistors and decides the required channel length and width values using given input voltage and required output current.

## II. ANALYTICAL LEVEL 3 MOSFET MODEL
The Level 3 model has been developed for simulation of short-channel MOS transistors; it can represent the characteristics of MOSFETs quite precisely for channel lengths down to 2μm [1]. The YITAL 1.5μ [7] process uses level 3 model. Although current and voltage equations are obtained as in the level 2 model, the short-channel and other small geometry effects are considered for the threshold voltage and mobility calculations.

$$I_D = \frac{\mu_s C_{OX}}{(1-\lambda V_{DS})} \cdot \frac{W}{L_{eff}} \left\{ \left[ V_{GS} - V_{FB} - 2\Phi_f - \frac{V_{DS}}{2} \right] V_{DS} - \frac{2}{3}\gamma \left[ \left( V_{DS} - V_{BS} + 2\Phi_f \right)^{\frac{3}{2}} - \left( V_{BS} + 2\Phi_f \right)^{\frac{3}{2}} \right] \right\} \quad (1)$$

Equation (1) shows the general formula for calculating the drain current. Equation (2) and (5) show the linear and saturation operation regions of the drain current calculation, respectively for n-channel MOSFET.

$$I_D = \mu_s . C_{OX} . \frac{W}{L_{eff}} \left[ V_{GS} - V_T - \frac{1+F_B}{2} . V_{DS} \right] V_{DS} \quad (2)$$

where

$$F_B = \frac{\gamma . F_S}{4.\sqrt{|2.\Phi_F| + V_{SB}}} \qquad (3)$$

and

$$\mu_s = \frac{\mu}{1 + \theta.(V_{GS} - V_T)} \qquad (4)$$

$$I_D = \mu_s C_{OX} \frac{W}{L_{eff}} \left\{ \left[ V_{GS} - V_{FB} - 2|\Phi_F| - \frac{V_{DS}}{2} \right] V_{DS} - \frac{2}{3}\gamma \left[ (V_{DS} - V_{BS} + 2|\Phi_F|)^{\frac{3}{2}} - (-V_{BS} + 2|\Phi_F|)^{\frac{3}{2}} \right] \right\} \quad (5)$$

$$L_{eff} = L - \Delta L \qquad (6)$$

The calculations of flat band voltage $V_{FB}$, mobility $\mu_s$ and effective channel length $L_{eff}$ are shown in equations (3), (4) and (6), respectively. The symbols in the above equations are: $I_D$ drain current, $V_{GS}$ gate-source voltage, $V_{DS}$ drain-source voltage, $V_{BS}$ bulk-source voltage, $V_{FB}$ flat band voltage, $\gamma$ body effect parameter, $\lambda$ channel length modulation, $2\Phi_F$ surface inversion potential, $C_{OX}$ total oxide capacitance, W channel width, $\mu_s$ short channel mobility, $L_{eff}$ effective channel length [1].

It is obvious from the equations the selection of W and $L_{eff}$ directly changes the drain current. It will be too hard to calculate the accurate aspect ratios from the equations since their parameters nonlinearly depend on each other. A neural network can easily estimate the aspect ratios. In this work, neural networks were used for function approximation for the equations above. These equations are over threshold models for the MOSFET. The sub-threshold attitude is not modeled in this work. Equations for p-channel MOSFET are also valid [1].

### III. THE MULTILAYER PERCEPTRON

Multilayer Perceptron (MLP) is the most common neural network model, consisting of successive linear transformations followed by processing with non-linear activation functions. MLP represents a generalisation of the single layer perceptron, which is only capable to construct linear decision boundaries and simple logic functions. However, by cascading perceptrons in layers complex decision boundaries and arbitrary Boolean expressions can be implemented. MLP is also capable to implement non-linear transformations for function approximations. [8], [9], [10].

The network consists of a set of sensory units (source nodes) that constitute the input layer, one or more hidden layers of computation nodes, and an output layer. Each layer computes the activation function of a weighted sum of the layer's inputs. The input signal propagates through the network in a forward direction, on a layer-by-layer basis. The learning algorithm for multilayer perceptrons can be expressed using generalised Delta Rule and gradient descent since they have non-linear activation functions. [11], [12], [13].

In general form of an MLP network, the $x_i$ inputs are fed into the first layer of $x_{h,1}$ hidden units. The input units are simply 'fan-out' units: no processing takes place in these units. The activation of a hidden unit (neuron $j$) is a function $f_j$ of the weighted inputs plus a bias, as given in equation (7).

$$x_{pj} = f_j \left( \sum_i w_{ji} x_{pi} + \theta_j \right) = f_j ( y_{pj} ) \qquad (7)$$

Where $w_{ji}$ is the weight of input $i$ to neuron $j$, $x_{pi}$ is input $i$, that is, output $i$ from the previous layer, for input pattern $p$ and $\theta_j$ is the threshold value. The output of the hidden units is distributed over the next layer of $x_{h,2}$ hidden units until the last layer of hidden units, of which the outputs are fed into a layer of $x_o$ output units [13].

### IV. THE IMPLEMENTATION CIRCUIT

Fig. 1 shows the n- and p-channel MOSFET circuit connections to obtain the training and test data. Supply voltage $V_{DD}$ was kept constant 5 V and -5 V for n- and p-channel, respectively. As can be seen from the Fig. 1, drain-source voltages $V_{DS}$ are equal to $V_{DD}$ and bulk-source potentials $V_{BS}$ are 0 V.

In this application, the MOSFETs were modeled between 1 V to 5 V range. The neural network structure shown in Fig.2 was used to model different operation regions. The MLP network consists of two inputs, seven hidden layer neurons and two output neurons. Activation functions of hidden and output layers were tangent hyperbolic sigmoid and linear transfer functions, respectively. The network was separately trained for each 1 V interval between 1 to 5 V since the MOSFET cannot be accurately modeled in a wide input gate-source voltage range.

Gate-source potential $V_{GS}$ and drain current $I_D$ were applied to the inputs of MLPs. The outputs of the MLPs were channel width W and effective channel length $L_{eff}$. The training and test data were obtained from HSpice 99.2. Both channel length and width were changed between 1.5μ to 3μ. Training data, in this range, were obtained with 0.5μ step for each parameter using 0.1 V step for gate-source voltage between 1 to 5 V. The test data were obtained randomly in the same range and they were different from the training data. Totally, 680 data was obtained from Hspice simulations. The simulation of network was performed in the Matlab 6.1 program. 640 of data were used to train the network and the remaining 40 were applied for testing. After the gate-source or source-gate voltages and required drain currents were applied to

the neural networks, the estimated aspect ratios were simulated in HSpice to check the validity of drain currents at the same input voltages.
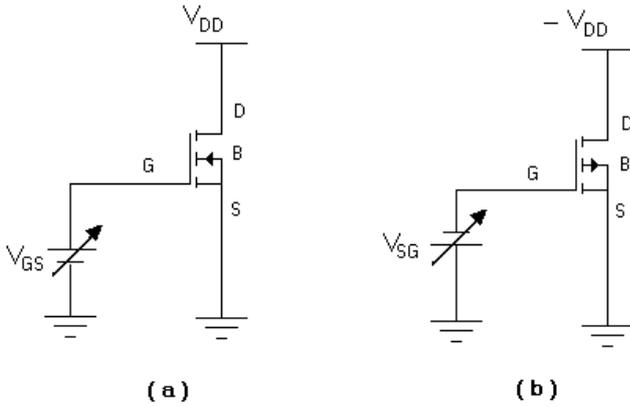


**Fig. 1.** MOSFET circuits for producing test and training data: a) n-channel, b) p-channel
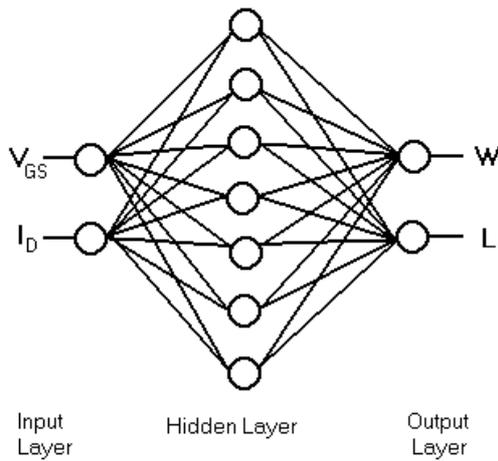


**Fig. 2.** The MLP neural network used for the implementation

Results for n-channel and p-channel MOSFETs were shown in Fig.3, 4, 5 and 6. Fig.3 and 4 illustrates the performance of the networks for training data, and Fig.5 and 6 for test data. For all figures the vertical axis is the amplitude of the drain current and the horizontal one is the gate-source or source-gate voltages with respect to the channel types. The sign showing current direction is not considered. The dotted lines in all figures represent the drain current with estimated aspect ratio and the solid lines represent the required drain currents.
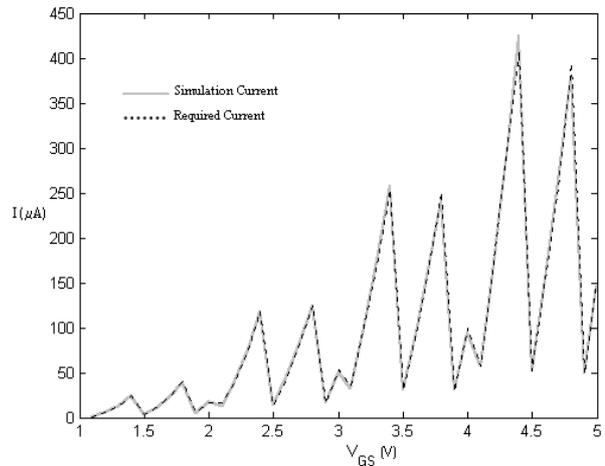


**Fig. 3.** The drain current (μA) v.s. gate-source voltage (V) for n-channel training data
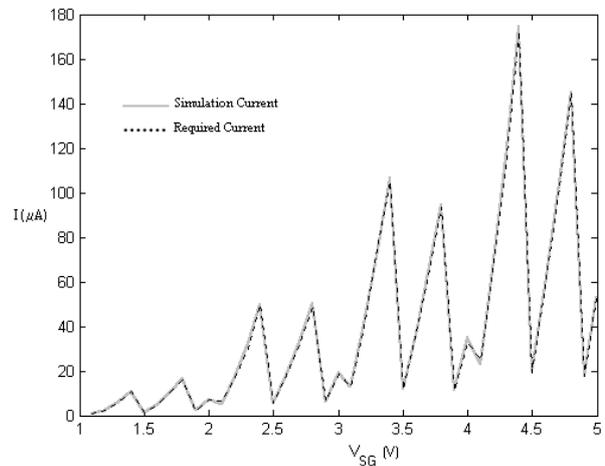


**Fig. 4.** The drain current (μA) v.s. gate-source voltage (V) for p-channel training data
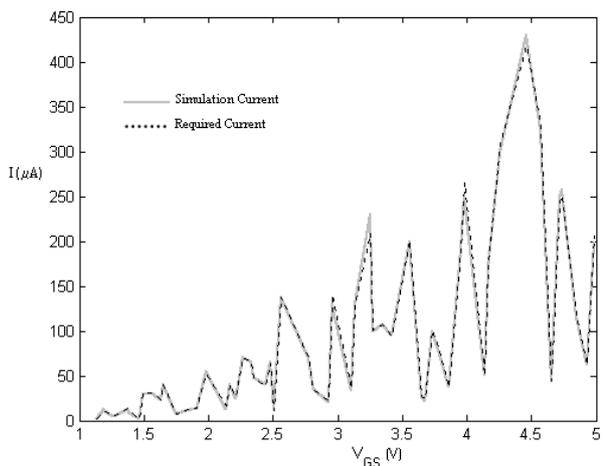


**Fig. 5.** The drain current (μA) v.s. gate-source voltage (V) for n-channel test data
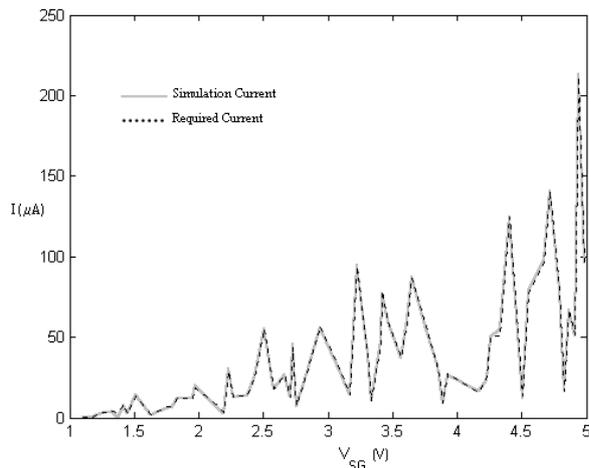
**Fig. 6.** The drain current (µA) v.s. source-gate voltage (V) for p-channel test data

The figures show that the estimated and required drain currents are very close to each other with maximum error of 7 %. This proves the effectiveness of the neural networks estimation.

## VI. CONCLUSION

The application results proved that the neural networks can decide channel width and length values accurately. The network has a very close function approximation for the MOSFET level 3 model. This work has a great importance for the MOS VLSI designers who have to decide the aspect ratio parameters by the experience. Improvements in this work can make it possible to design analog or digital integrated circuits with perfect approximations to the required functions. In complex design programs like CADENCE, addition of the aspect ratio decision approximation would be very useful. The application is a good starting strategy for the design of complex MOSFET circuits.

## REFERENCES

1. Kang, S., M., Leblebici, Y.: CMOS Digital Integrated Circuits Analysis and Design, 3rd Edition, McGraw Hill Colege Div (2002)
2. Ozyilmaz, L., Yildirim, T., Koklu.K.: Comparison of neural algorithms for function approximation, Pakistan Journal of Applied Sciences, Vol.2 (3) (2002) 288-294
3. Yildirim, T., Torpi, H., Özyilmaz, L.: Modelling of Active Microwave Transistors Using Artificial Neural Networks, Proceedings of IJCNN'99 Int. Joint Conf. on Neural Networks, Vol. 6. IEEE publication, Washington (1999) 3988–3991
4. Gunes, F., Torpi, H., Çetiner, B.A.: Neural Network Modeling of Active Devices for Use in MMIC Design, Artificial Intelligence in Engineering, Vol. 13. Elsevier (1999) 385–392
5. Gunes, F., Torpi, H., Gurgen, F.: Multidimensional Signal-Noise Neural Network Model, Circuits Devices and Systems, Vol. 145. IEE Proceedings (1998) 111-117
6. Gunes, F., Gurgen, F., Torpi, H.: Signal-Noise Neural Network Model for Active Microwave Devices, Circuits Devices and Systems, Vol. 143. IEE Proceedings (1996) 1-8
7. Leblebici, D., Caliskan, A., U., Ilyas, S., I., Ergintav, A.: 1.5 Micron CMOS-ASIC Fabrication Technology, NATO-TU MICROFAB II Report, Marmara Research Center (1998)
8. Geva, S., Sitte, J.: A Constructive Method for Multivariate Function Approximation by Multilayer Perceptrons, IEEE Transactions on Neural Networks, Vol. 3 (4) (1992) 623-624
9. Haykin, S.: Neural Networks: A Comprehensive Foundation, Macmillan College Publishing, New York (1994)
10. Hush, D., R., Horne, B., G.: Progress in Supervised Neural Networks, IEEE Signal Processing Magazine, January (1993) 8-39
11. Jondarr, C., G., H.: Back propagation Family Album, Technical Report C/TR9605, Dept. of Computing, Macquarie University (1996)
12. Rumelhart, D., E., Hinton, G., E., Williams, R., J.: Learning Internal Representations by Error Propagation, In Parallel Distributed Processing, Vol.1, Cambridge, MIT Press MA 318-362
13. Zurada, J.,M.: Introduction to artificial Neural systems, PWS Publishing Boston (1995)