A NOVEL CMOS 1-BIT FULL ADDER CELL WITH THE GDI TECHNIQUE

Alireza Saberkari
e-mail: a_saberkari@ee.iust.ac.ir

Shahriar Baradaran Shokouhi
e-mail: bshokouhi@iust.ac.ir

College of Electrical Engineering, Iran University of Science & Technology, Tehran, Iran

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ABSTRACT

In this paper, a novel design of a low-power 1-bit full adder cell is proposed, where the GDI technique has been used for the simultaneous generation of XOR and XNOR functions. Simulation results are performed by HSPICE based on 0.18 μm CMOS technology, shows that the new full adder circuit has the lowest power-delay product over a wide range of voltages among several low-power adder cells of different CMOS logic styles.

I. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance.

Recently, building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology does not advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high performance adder cells are of great interest.

A structured approach for designing and analyzing an adder cell is based on decomposing it into smaller modules. Each of these modules is implemented, optimized, and tested separately. Several full adder cells are composed by connecting these modules.

The goal of this paper is designing a low-voltage and so low-power full adder cell with the GDI[1] technique. This technique that was recently developed and presented in [1], proposes an efficient alternative for logic design in standard CMOS and SOI technologies.

The rest of this paper is organized as follow; in section II, we review the previous designs of 1-bit full adder cells. In section III, the GDI technique and implementation method of XOR and XNOR functions using this technique are presented. In section IV, we present the new design of proposed low-voltage and low-power 1-bit full adder circuit. In section V, we describe simulation results and compare the performance of the new full adder with other circuits. Finally, we make conclusions in section VI.

II. PREVIOUS CMOS 1-BIT FULL ADDER CELLS

The block diagram of the full adder cell and its building blocks are shown in Figure 1. In addition, various circuits have been proposed for each module [2].

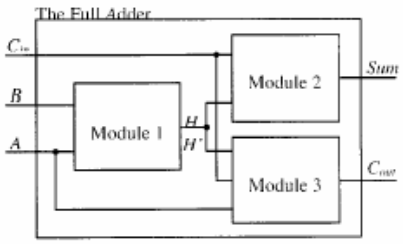

Figure 1. The adder cell divided into three main modules

In [3], the conventional 20-transistor transmission gate full adder has been proposed which is called the conventional full adder (TGA) in this paper. In [4], Zhuang and Wu simplified the conventional transmission gate full adder by using the transmission function theory and then proposed a new cell, which is called the transmission full adder (TFA). The transmission full adder has 16 transistors, which consumes less power and operates faster than the conventional one. In [5-8], some high performance 1-bit full adder cells have been proposed which only need 10-16 transistors to implement. All of them perform well at a normal 3.3V supply voltage, but all such full adders suffer the problem of signal degradation and therefore can not work properly in low voltage systems. In [6], a 14-transistor 1-bit full adder cell is proposed. In [9], Lee and Sobelman alleviated the problem of threshold voltage and non-zero standby power consumption in 14-transistor full adder proposed in [6],

[1]- Gate-Diffusion-Input

and presented an 18-transistor low-voltage full adder. In [7], a 10-transistor 1-bit full adder cell is proposed which can not work correctly at low voltage.

Recently, a structural approach towards the low-power adder cell design has been adopted where the adder cell is partitioned into two stages. The first stage is to generate the intermediate logic functions of XOR and XNOR. This stage is usually implemented in pass transistor logic to reduce the transistor count. These complementary outputs, together with other inputs, will be fed to the second stage. The *Sum* and *Carry* outputs are generated from the second stage.

Since adder cells are normally cascaded to form a usual arithmetic circuit, their drivability must be ensured. In short, the driving cell must provide almost full swing outputs to the driven cell. Otherwise, the performance of the circuit will be degraded dramatically or become non operative at low supply voltage. For the adder cells of TGA and TFA, they can not be cascaded without additional buffers attached to the outputs of each cell.

III. THE GDI TECHNIQUE AND IMPLEMENTING OF XOR AND XNOR FUNCTIONS

GDI method is based on the use of a simple cell as shown in Figure 2 [1]. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: (1) GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies.

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions [1]. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

As can be seen in [1], GDI cell structure is different from the existing PTL techniques and has some important features, which allows improvements in design complexity level, transistor counts, static power dissipation and logic level swing.

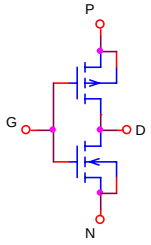

Figure 2. GDI basic cell [1]

Table I. Some logic functions that can be implemented with a single GDI cell [1]

N	P	G	D
'0'	B	A	A'B
B	'1'	A	A'+B
'1'	B	A	A+B
B	'0'	A	AB
C	B	A	A'B+AC
'0'	'1'	A	A'

XOR and XNOR functions are the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. In this new cell, we have used the GDI technique for generating of XOR and XNOR functions. It uses only six transistors to generate the balanced XOR and XNOR functions, as shown in Figure 3.

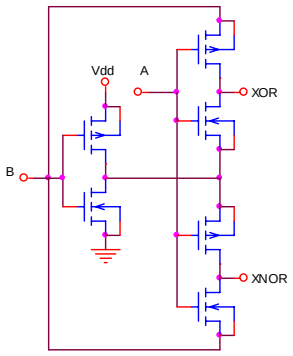

Figure 3. XOR/XNOR cell with the GDI method

Figure 4 shows the waveforms of the output nodes of this cell for the inputs *A* and *B*. As can be seen, the XOR function has generated a weak low when the inputs are *AB:00*, and the XNOR function has generated a weak high for inputs *AB:11*. It caused that, the transmission of the signal is performed through the diffusion nodes of the GDI cells and it might cause a swing drop of V_{TH} in the output signals.

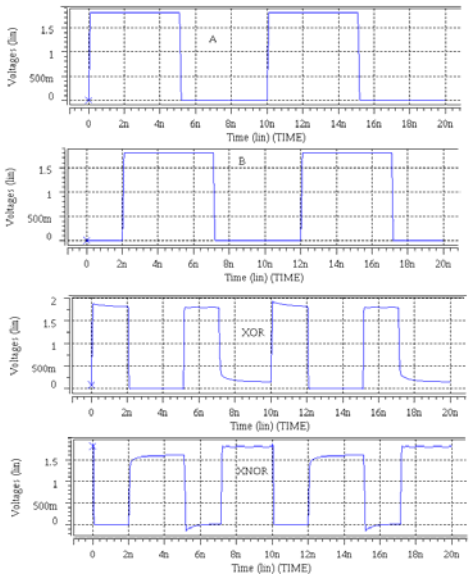

Figure 4. Waveforms of the outputs of XOR/XNOR cell

In order to overcome this problem, 4 transistors are added to the XOR/XNOR cell, as shown in Figure 5. The two series connected PMOS help pulling up the XNOR to a strong "1" when the input combination *AB:11* occurs, whereas two series NMOS help pulling down the XOR to a strong "0" when the input combination is *AB:00*.

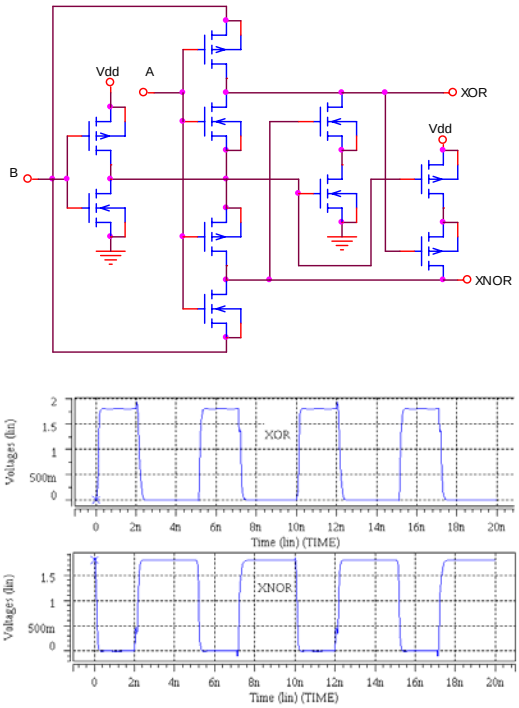

Figure 5. Improved XOR/XNOR cell with the GDI method and its output waveforms

IV. PROPOSED FULL ADDER CIRCUIT

The proposed full adder circuit is shown in Figure 6. In the first stage of this cell, the GDI technique is used for generating of XOR and XNOR functions.

As mentioned in section II, one important requirement of full adder cells especially at low voltage, is to provide enough driving power to the following circuits. The drivability is ensured by the full signal swing and decoupling of inputs and outputs (at least one inverter per cell) so that the adder cell can be cascaded arbitrarily and work reliably in any circuit configuration. So the second stage of full adder cells which generate *Sum* and *Carry* must have enough drivability.

In addition, there are several choices of circuits to generate signal *Sum*. We use a similar circuit as that of TFA, but fully exploit the available XOR and XNOR outputs from stage I to allow a single inverter to be attached at the last stage. The output inverter guarantees sufficient drive to the cascaded cells.

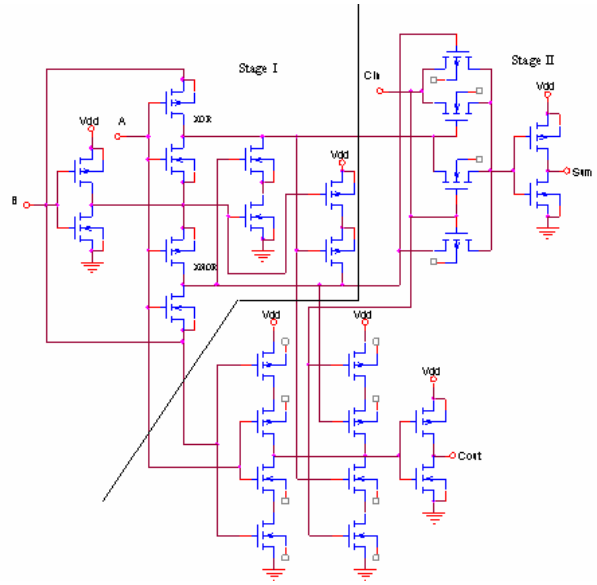

Figure 6. The proposed full adder cell

The smallest number of transistors for generating the C_{out} signal is two, which is used in 10-transistor 1-bit full adder cell. But it suffers from the threshold voltage drop problem. Although a 4-transistor circuit can be used to generate a full swing C_{out} signal, it does not provide enough driving power. In this full adder cell, a circuit based on complementary CMOS logic style is used. Its robustness against voltage scaling and transistor sizing enables it to operate reliably at low voltage. Also, the output inverter guarantees sufficient drive to the cascaded cells.

V. SIMULATION RESULTS

Simulation results are performed by HSPICE based on 0.18 μm CMOS technology. The supply voltages range from 0.5V to 3.3V. The operating frequency is 100MHz

for supply voltages above 1V, and 10MHz for supply voltages below 1V. The snapshot of the waveforms at 1.8V is shown in Figure 7.

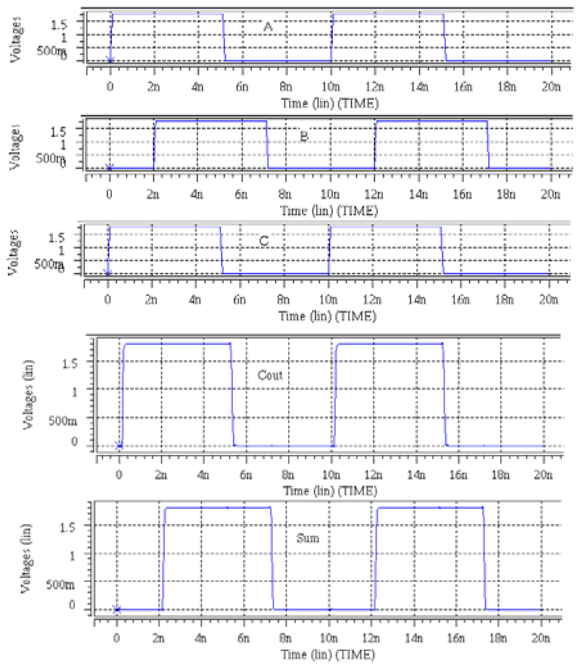

Figure 7. Snapshots of waveforms at 1.8V and 100MHz

The power and delay plotted against supply voltages of the five full adders are shown in Figure 8. Simulation results show that the 10T adder cell fails to function at low voltage. The lowest voltage that it can work at 100MHz is 1.8V. The excessive power and delay attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full swing transitions. The speed of the 14T decreases faster with the supply voltage than other adder cells. This circuit does not work at supply voltages below 0.8V at 10MHz. Simulation results also show that the new cell, together with TGA and TFA can work reliably at low supply voltages down to 0.5V at 10MHz. Although TGA and TFA have lesser transistor count, additional buffers are required at each output to boost up its drivability, which increases their short circuit and switching power. As can be seen, the new full adder cell is the most energy efficient cell.

VI. CONCLUSION

In this paper, a new low-power full adder capable of operating down to 0.5V has been presented. In this cell, the GDI technique has been used for generating of intermediate functions of XOR and XNOR. The new circuit is the most energy efficient cell compared to several recently proposed circuits.

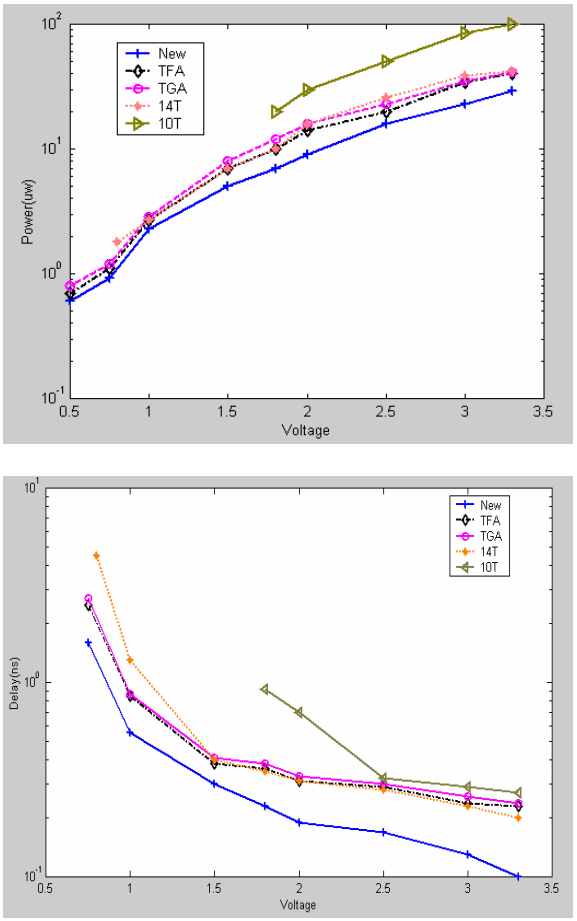

Figure 8. Compared results of power and delay of adder cells

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