An Investigation of the SONOS with Side-Block Oxide for Non-Volatile Memory

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Abstract

In this paper, a novel device structure called the SONOS non-volatile memory with side-block oxide (SBOSONOS-NVM) has been demonstrated. The SBOSONOS-NVM enhances the program/erase (P/E) speed and memory window by using Fowler–Nordheim (FN) injection mechanism, when compared with SONOS non-volatile memory without side-block oxide (SONOS-NVM). The SBOSONOS-NVM still has excellent characteristics with gate length downs to 40 nm. The side-block oxide structure can suppress the Source/Drain electric field encroachment, so its gate controllability over the channel charges can be improved. Also, the SBOSONOS-NVM is also fully compatible with standard CMOS process technology.

1. Introduction

Non-volatile memory devices can be divided into two kinds. One is the floating gate (FG) device, and the other is the charge trapping device. They can maintain data after charging without power supply [1]. Conventional floating gate flash EEPROM devices will face many challenges as gate length scaling down, such as Stress Induced Leakage Current (SILC), short channel effects (SCEs), and reduction of Floating Gate coupling ratio [2-3]. In addition, a single defect of tunneling oxide will generate a leakage path, and then causes the stored charges loss. As a result, it will reduce retention time and worsen endurance performance [4]. Consequently, the charge trapping Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile memory have been proposed to overcome the above-mentioned problems [5]. The SONOS NVM can be considered that it will replace the conventional floating gate EEPROM devices in the sub-30-nm technology node [6]. The Si_3N_4 trapping layer has localized trapping charges characteristic, so that it can achieve 2-bit/cell operation. Also, a single defect will not cause all of the stored charges loss, just a few charges loss do not affect the reliability of the SONOS NVM. Therefore, retention time of the SONOS NVM can be improved. Furthermore, SONOS NVM also possesses low P/E voltages due to its better scalability, and simple device process [7]. However, conventional SONOS NVM still has many issues, so many of studies have been published, such as multigate or gate all around device structures for SONOS NVM applications to enhance the P/E efficiency [8]. The reason is that the gate controllability has been ameliorated. Unlike the previous described, here, we demonstrate a novel device structure called the SONOS NVM with side-block oxide (SBOSONOS-NVM) on the premise of improving the P/E efficiency. This novel device structure is not only applying to SONOS NVM, but also compatible with standard CMOS process technology. In our study, the SBOSONOS-NVM compared with the SONOS-NVM without side-block oxide (SONOS-NVM) is performed in terms of P/E speed, memory window, and retention time performance.

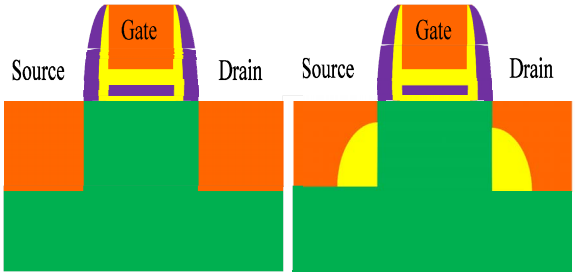

Fig. 1. A schematic cross-sectional view of the SONOS-NVM and the SBOSONOS-NVM.

2. Device Structure and Fabrication

Silvaco TCAD simulation was used to fabricate the SBOSONOS-NVM. The main key processes are shown in Fig. 2. First, the starting material is p-type (100) silicon wafer (Fig. 2(a)), and the tunneling oxide 3 nm was grown with thermal oxidation. Next, 4 nm thickness LPCVD Si_3N_4 layer was deposited as trapping layer, followed by CVD deposition of 6 nm blocking oxide. Poly-Si layer was formed as the gate structure, and the oxide layer and Si_3N_4 layer as hard mask were also deposited, respectively (Fig. 2(b)). After the gate patterning, the oxide and Si_3N_4 were deposited and etched as spacer to protect gate from dry etching when forming the side-block oxide structure (Fig. 2(c-e)). In order to form the S/D regions, poly-Si was deposited, and then planarized by the chemical mechanical polishing (CMP). After that, the S/D was implanted by arsenic ions and by means of annealing processes. Finally, back end of line processes would end up by a standard Si process so that the SBOSONOS-NVM was produced (Fig. 2(f)).

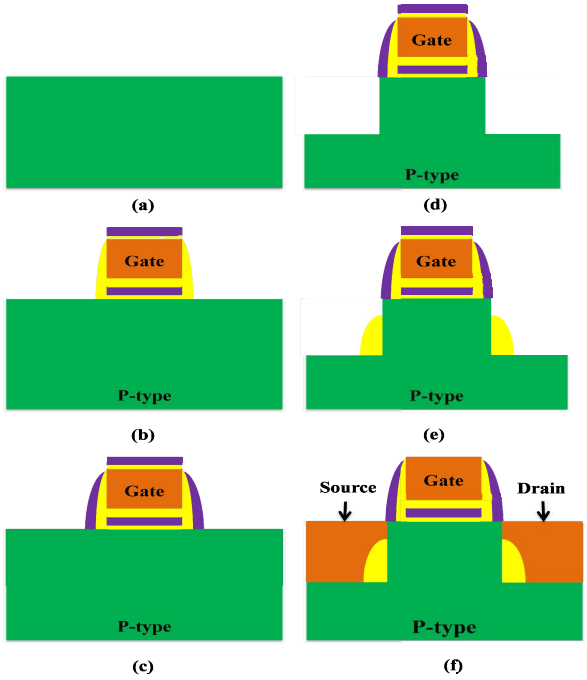

Fig. 2. The main process flows of the SBOSONOS-NVM devices. (a) P-type Si-Sub. (b) Gate pattering. (c) Si_3N_4 spacer as hard mask. (d) Dry etch of p-type Si-Sub. (e) Formation of side-block oxide. (f) Formation of the SBOSONOS-NVM.

3. Results and Discussion

Fig. 3. shows that the programming time versus V_{th} shift by using FN tunneling mechanism. We can see that the SBOSONOS-NVM has fast program speed when compared with the SONOS-NVM at V_p = 12, 14, and 16 V, respectively. Also, for all operation voltage, its programmed V_{th} shift can be improved 16 %, 16 %, and 9 % when programming time reaches to one second. Owing to that its side-block oxide can restrain S/D electrical field encroachment, so it can make better gate controllability.

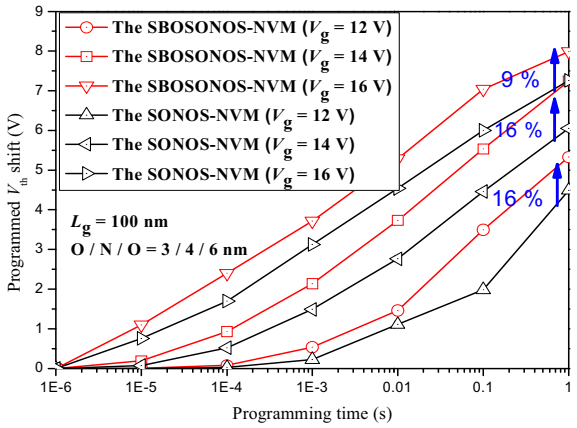

Fig. 3. The programming operations of the SBOSONOS- NVM and the SONOS-NVM.

After one second programming operation at V_p = 12, 14, and 16 V, respectively. The erase behavior for both of them are shown in Fig. 4. Due to the side-block oxide structure, the erased V_{th} shift also can be improved 9 %, 14 %, and 11 % at V_e = -12, -14, and -16 V.

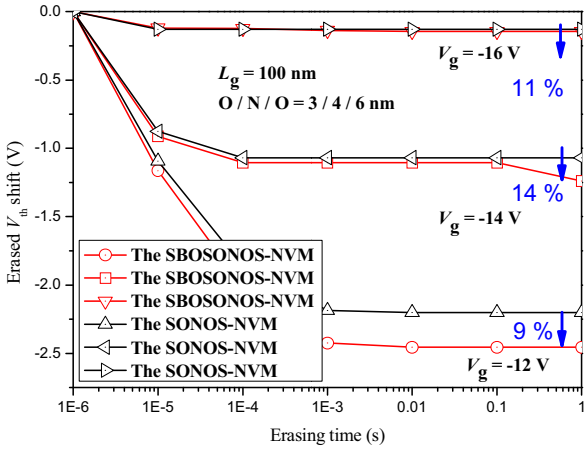

Fig. 4. The erase operations of the SBOSONOS-NVM and the SONOS-NVM.

Fig. 5 exhibits programmed V_{th} shift versus four kinds of gate length by using FN tunneling mechanism subjected to a programming bias of 12 V for 1 s. We can observe that the SBOSONOS-NVM has larger V_{th} shift when compared with the SONOS-NVM. The reason is that the side-block oxide structure can restrain S/D electrical field encroachment so that the gate controllability can be enhanced even when gate length scaling down to 40 nm.

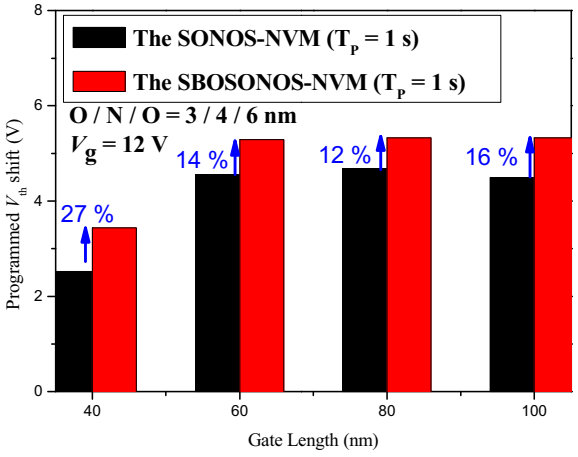

Fig. 5. Programming operation of the SBOSONOS-NVM and the SONOS-NVM under four kinds of gate length.

Next, the erasing operation can be seen from the Fig. 6. After one second programming operation at V_p = 12 V, the erase efficiency of the SBOSONOS-NVM is also superior under four kinds of gate length. As above mentioned, the side-block oxide is also helpful for erasing operation.

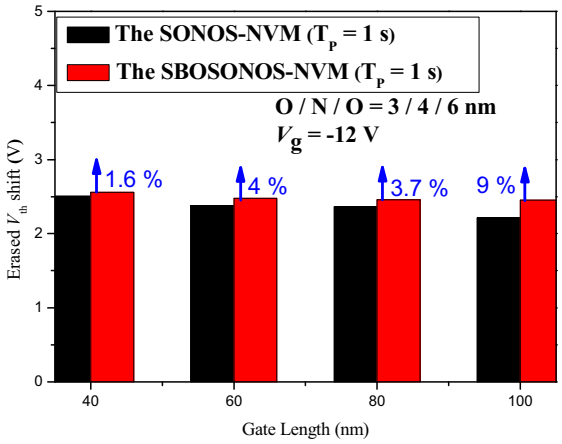

Fig. 6. Erasing operation of the SBOSONOS-NVM and the SONOS-NVM under four kinds of gate length.

In Fig. 7, we show and discuss the retention time characteristic of the SBOSONOS-NVM and the SONOS-NVM subjected to a programming bias of 14 V for 0.01 s. Also, the memory windows for both of them are measured at room temperature. We can see that the SBOSONOS-NVM has higher V_{th} state when retention time at 1 s. Due to its side-block oxide can enhance the gate controllability to store more charges. The more electrons can be captured by the Si_3N_4 layer so that it will has larger V_{th} state. As a result, the remaining charges of the SBOSONOS-NVM at extrapolated 10-year line is still more than the SONOS-NVM. Additionally, the retention time of the SBOSONOS-NVM can be improved more than 17 % when compared with the SONOS-NVM

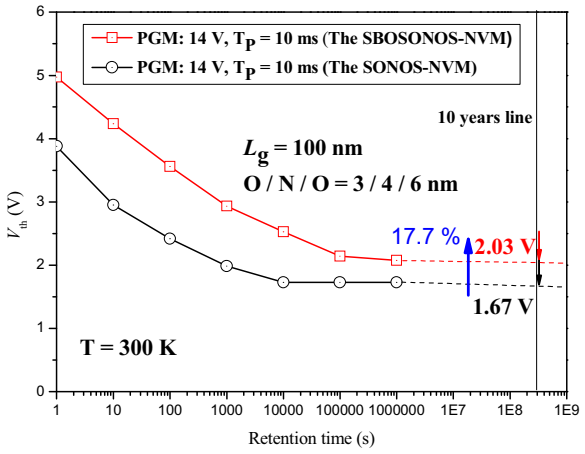

Fig. 7. Retention time of the SBOSONOS-NVM and the SONOS-NVM.

4. Conclusions

In this paper, the SBOSONOS-NVM have been proposed, and the effects of the side-block oxide for SONOS- NVM characteristics have been also investigated. The side-block oxide structure can reduce the PN junction area, therefore it can suppress S/D electric field encroachment. When gate length is 100 nm, we found that the programmed/erased V_{th} shift of the SBOSONOS-NVM have been improved 9 % and 11 % at V_p = 12 V. Besides, when gate length scaling down to 40 nm, the programmed/erased V_{th} shift of the SBOSONOS-NVM still have been improved 27 % and 1.6 % at V_p = 12 V. This is mainly due to the fact that the gate controllability can exhibit better behavior than the SONOS-NVM, so the SBOSONOS-NVM has better program/erase performance. Also, retention time of the SBOSONOS-NVM can be ameliorated more than 17 % when compared with the SONOS-NVM.

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