FLOATING GATE MOS TRANSISTOR BASED LOW VOLTAGE NEURON DESIGN AND XOR PROBLEM IMPLEMENTATION

Fatih Keleş[1] Mutlu Avcı[2] Tülay Yıldırım[2]
e-mail: fatih@ce.yildiz.edu.tr *e-mail: mavci@yildiz.edu.tr* *e-mail: tulay@yildiz.edu.tr*
[1]*Yildiz Technical University, Faculty of Electrical & Electronics, Department of Computer Engineering, 34340,Besiktas, Istanbul, Turkey*
[2]*Yildiz Technical University, Faculty of Electrical & Electronics, Department of Electronics and Communication Engineering, 34340,Besiktas, Istanbul, Turkey*

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ABSTRACT

In this study, a floating-gate MOS (FGMOS) based neuron model using four-quadrant analog multiplier with rail-to-rail linear input and FGMOS based differential comparator has been designed and simulated in HSPICE environment with YİTAL 1.5μm process parameters. Using the proposed neuron circuits a neural network was realized. XOR problem was applied to test accuracy of the network and the results were concluded.

I. INTRODUCTION

Neural network hardware implementations are important to realize any required function. Nowadays, one of the greatest aim of microelectronics science is to develop a general purpose integrated circuit which can change own characteristics or transfer functions with respect to any condition. Neural integrated circuits are this kind of proposed circuits with on chip or off chip learning capabilities.

FGMOS structures are also known as neuron MOS because of functional similarity of the neuron [1]. Their multi input advantages make it simpler to realize an artificial neuron circuit. The FGMOS drain current is proportional to the square of the weighted sum of the input signals [1]-[4]. In the last few years, FGMOS transistors have found many applications in electronic programming [2], Op-amp offset compensation [3], D/A and A/D converters [4], inverters and amplifiers [5], voltage attenuators [6] and current mirrors [7]. Recently, an increased number of publications on the use of the FGMOS in analog computational circuits have been reported voltage squarers and multipliers [8]-[9].

In previous works, the neuron circuit generally has the following components; current mode multiplier, an Op-amp based adder and activation function generator [10]. The summation and the activation function were realized in different blocks. In this paper unlike the previous works, these functions were realized in the same FGMOS comparator block.

In this work, using FGMOS based multiplier and FGMOS differential comparator, a neuron was designed. Combining the neuron blocks a Multi Layer Perceptron (MLP) neural network was realized. XOR problem was used to test the neural network. The weight and bias values to apply XOR function were developed in MATLAB 6.0 environment using the same network architecture with the realized neural network circuit. Finally the designed FGMOS based neural network circuit was simulated in HSPICE environment with YITAL 1.5μm process parameters to realize XOR function. All simulation results were shown and concluded.

II. FGMOS TRANSISTOR

The multiple-input-floating-gate transistor is an ordinary MOS transistor which the gate is floating. The basic structure of an n-channel FGMOS transistor with n-input voltages V_1, V_2, . . ., V_n, is shown in Figure 1(a). The floating-gate is formed by the first polysilicon layer over the n-channel while the multiple-input gates are formed by the second polysilicon layer and they are located over the floating gate. This floating gate is capacitively coupled to the multiple-input gates. The symbolic representation of such devices is shown in Figure 1(b). The drain current of a FGMOS transistor with n-input gates in the saturation region, neglecting the second-order effects, is given by the following equation:

$$I_D = \beta[k_1(V_1 - V_S) + k_2(V_2 - V_S) + \cdots + k_n(V_n - V_S) - V_T]^2 \quad (1)$$

where

β = $(\mu_n Cox/2)(W/L)$ transconductance parameter;
μ_n electron mobility;

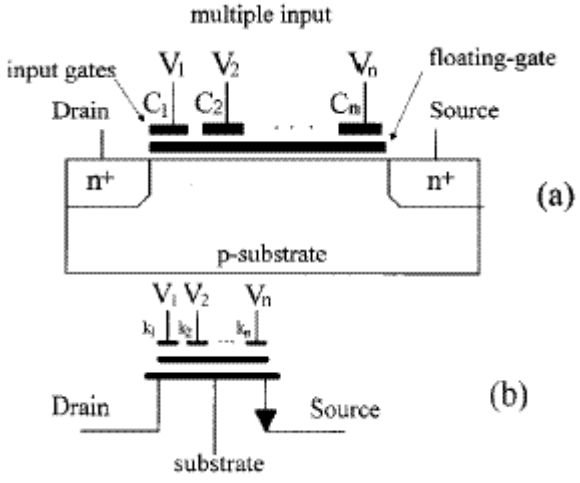

Figure 1. (a) Basic structure of an NMOS floating-gate transistor with n input gates. (b) Symbolic representation.

C_{OX}	floating-gate to oxide capacitance;
W / L	aspect ratio of the transistor;
k_i (i = 1, 2 . . . n)	input capacitive-coupling ratios;
V_S	source voltage;
V_T	threshold voltage of the transistor.[1], [5], [6]

The input capacitive-coupling ratios k_i , neglecting the overlap capacitances, are defined as,

$$k_i = \frac{C_i}{\sum_{i=1}^{n} C_i + C_{GS}} \tag{2}$$

where C_i are the input capacitances between the floating gate and each of the *i*th input [see Figure 1(a)] and C_{GS} is the floating-gate to source capacitance which is equal to (2/3)Cox for operation in saturation region.

From (2), it is clear that the summation of all capacitive-coupling ratios is always less than 1, $\sum_{i=1}^{n} k_i = \sum_{i=1}^{n} C_i / \left(\sum_{i=1}^{n} C_i + C_{GS}\right) < 1$, due to the capacitance C_{GS}, which is located in the denominator.

III. BUILDING BLOCKS

The proposed neuron circuit contains two main blocks. These are FGMOS multiplier and FGMOS differential comparator units.

FGMOS MULTIPLIER

Figure 2 shows the single-ended squarer circuit. It is constructed by a simple squarer with balanced inputs and two linear attenuators which act as input stages. The circuit of the simple squarer based on the multitail technique [11], is realized by using the transistors Ma, Mb, and Mc which operate in the saturation region, where

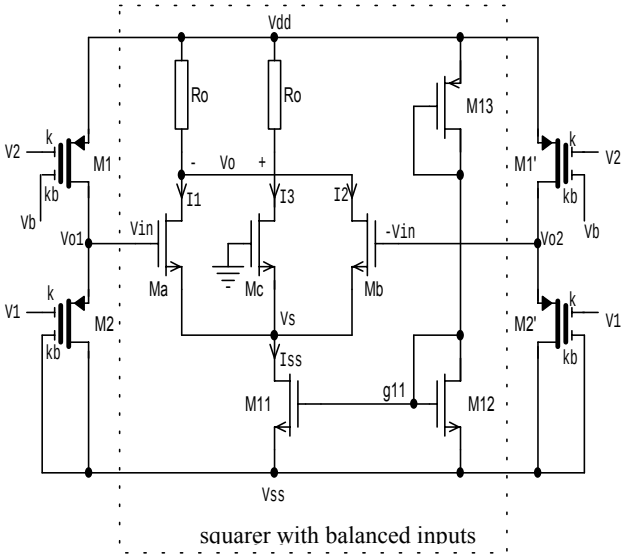

Figure 2. Single-ended voltage squarer with attenuators based on FGMOS transistors.

the aspect ratio of Mc be half that of Ma and Mb, $\beta = \beta_a = \beta_b = \beta_c/2$. The balanced input voltage Vin is applied to the gate of Ma and Mb, while the gate of Mc is connected to ground. The common-mode input voltage is zero. The balanced inputs Vin and -Vin are generated by the two attenuators. Taking the well-known square-law model of the MOS transistors operating in the saturation region and neglecting the second order effect, the output voltage of the squarer can be expressed as

$$V_o = 2R_o \beta V_{in}^2 \tag{3}$$

The squarer function is thus realized. The differential balanced inputs can be realized using two attenuators as input stages. The voltage V_1 applied to the one input gate of M1 and M2' and the voltage V_2 to the one input gate of M2 and M1'. The voltage V_B is adjusted to set the output offset zero. Thus, the output voltages V_{o1} and V_{o2} of the two attenuators are given by

$$V_{o1} = \alpha (V_1 - V_2) \tag{4a}$$
$$V_{o2} = -\alpha (V_1 - V_2) \tag{4b}$$

Combining (3), (4a), and (4b), the output voltage of the overall circuit is given by

$$V_o = 2R_o \beta \alpha^2 (V_1 - V_2)^2 \tag{5}$$

which is proportional to the square of the voltage difference V_1-V_2. It should be noted here that all the even harmonics and the dc component which are produced by the two attenuators and the simple squarer are eliminated due to differential structure of the overall circuit.

If we assume that a transistor of the squarer is in cutoff, $V_{GS} - V_T = 0$ then the maximum input range is determined by the inequality

$$(V_1 - V_2)^2 \le \frac{I_{SS}}{6\alpha^2\beta} \tag{6}$$

According to (6), an increase of the value of the current source I_{SS} results in a higher input-voltage range. However, increasing the bias current a larger voltage drops across resistance R_O, causing the transistors to operate in the linear region. This applies especially in the second quadrant where the voltage V_1 takes the maximum value $V_1 = V_{DD}$ while V_2 takes its minimum value $V_2 = V_{SS}$ and in the forth quadrant where the voltage V_1 takes the minimum value $V_1 = V_{SS}$ while V_2 takes maximum the values $V_2 = V_{DD}$. For proper operation, the dependence on the maximum load resistance is

$$R_{o\max} = \frac{V_{DD}(1-2\alpha)+V_T}{\frac{I_{SS}}{2}+4\beta\alpha^2 V_{DD}^2} \tag{7}$$

The input range is limited for load resistance values smaller than $R_{O\max}$.

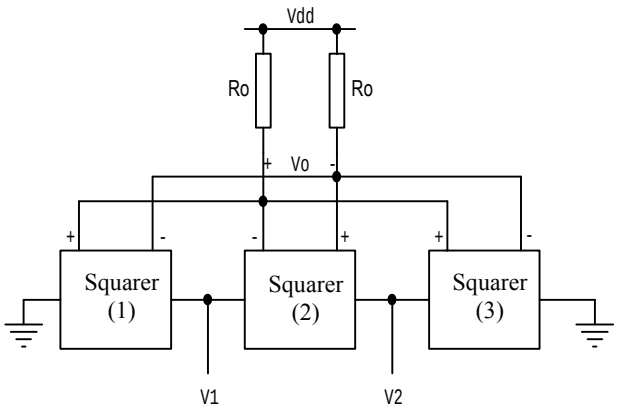

Figure 3. Single-ended four-quadrant multiplier.

A four-quadrant multiplier can be easily implemented using the proposed voltage squarer circuit as shown in Figure 3. Three squarers are used, where the input voltages of the first squarer are V_1 and 0, the input voltages of the second are V_1 and V_2 and the input voltages of the third squarer are 0 and V_2. This multiplier implementation is based on the identity $x^2 + y^2 - (x - y)^2 = 2xy$. After routine calculations, the output voltage of the multiplier is given by

$$V_o = 4R_O\beta\alpha^2 V_1 V_2 \tag{8}$$

The advantages of the multiplier is that the voltage V_1 and V_2 are two single-ended signals and may have rail-to-rail dynamic range.

For our application, the p-channel FGMOS based attenuator is chosen in order to avoid body effect, since we have used N-well 1.5 μm YİTAL CMOS process parameters. The supply voltage for all circuits was ±1.5V. All circuits were simulated using HSPICE simulator.

The linear attenuator has attenuation factor α = 1/9, rail-to-rail voltage input range and zero-output offset. The capacitance coupling ratio of the attenuator were set as k=0.1 and k_B = 0.8 while the bias voltage V_B = 0.1875 V. The aspect ratios of the transistors were $(W/L)_{M1,2}$ = 20/5. Thus, the capacitances C and C_B must have the values C = 93 fF and C_B = 744 fF, respectively.

The current source and the load resistance of the squarer with two attenuators were set 200 μA and 5 KΩ, respectively. The aspect ratio of transistors Ma, Mb, and Mc were set $(W/L)_{Ma,\ b}$ = 33/5 and $(W/L)_{Mc}$ = 66/5, respectively. The common-mode input signal were set equal to zero. The dc transfer characteristics of the differential squarer with the input V_1 varied rail-to-rail and the input V_2 taking values from -1.5 V to 1.5 V with 0.5 V-steps is plotted in Figure 4.

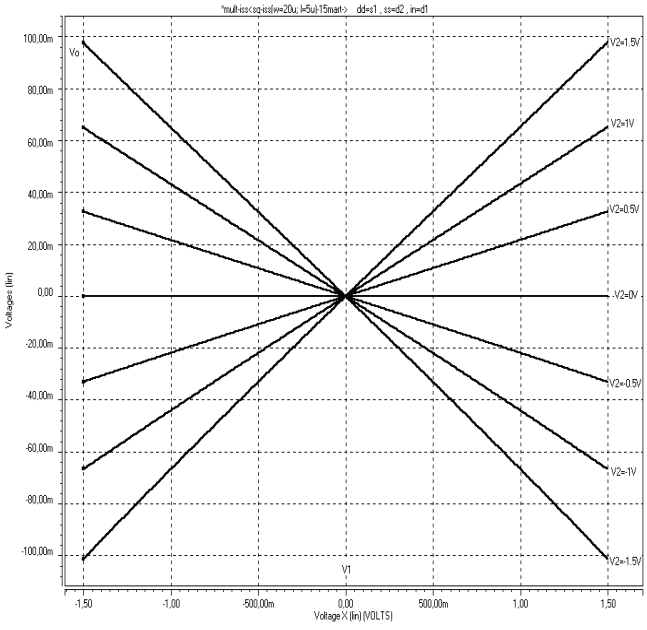

Figure 4. DC transfer characteristics of the multiplier.

FGMOS COMPARATOR

By substituting FGMOS transistors instead of input stage MOS transistors in a standard comparator the FGMOS comparator is obtained as in Figure 5. Since FGMOS has a summation of weights, a standard comparator structure with FGMOS directly realizes sum of multiplication. Since the output of the FGMOS is a curve as seen in Figure 6, containing a slope depending on the channel length and width, the activation function like a sigmoid is directly obtained.

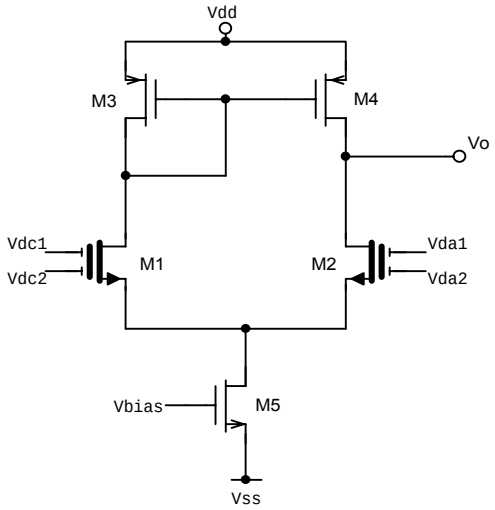

Figure 5. FGMOS differential comparator circuit.

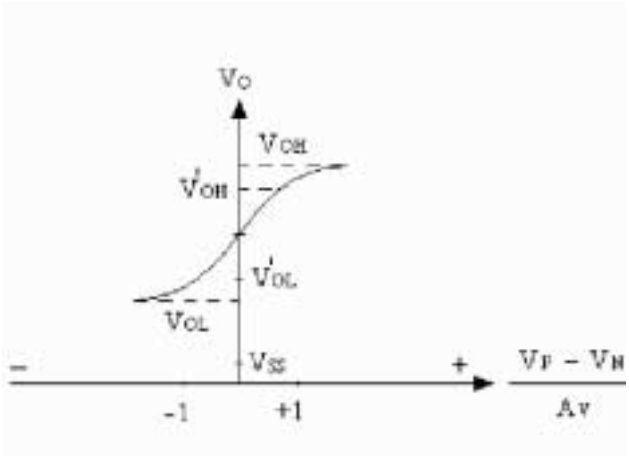

Figure 6. DC transfer characteristics of the comparator

IV. THE NEURON CIRCUIT

In the Figure 7. a neuron circuit block diagram is shown. As shown in figure by the combination of the building blocks neuron is obtained.

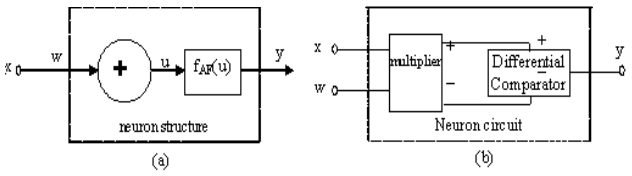

Figure 7. (a) Neuron model, (b) Neuron circuit

V. THE XOR IMPLEMENTATION AND SIMULATION

The neural network to realize XOR is shown in Figure 8. Table 1 shows a mapping between standard logic and low voltage circuit input voltages. In this realization each neuron has three multiplier units. These are for weight, bias and input calculation. The MLP ANN developed for this application as in Figure 8 contains 1 hidden layer with two neurons and an output layer with a single neuron. In MATLAB 6.0 environment error backpropagation is applied with the values in Table 1. The weight and bias values are taken from MATLAB 6.0 to apply to the circuit.

The simulation results are shown in Figure 9.

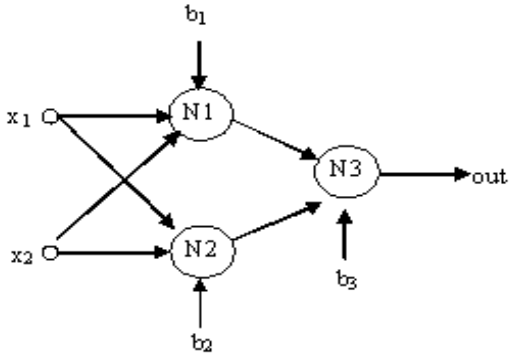

Figure 8. Network structure for realizing XOR problem.

x1 ⊕ x2	y	x1 ⊕ x2	out
0 ⊕ 0	0	-1.5 ⊕ -1.5	-1.2
0 ⊕ 1	1	-1.5 ⊕ 1.5	1.2
1 ⊕ 0	1	1.5 ⊕ -1.5	1.2
1 ⊕ 1	0	1.5 ⊕ 1.5	-1.2

Table 1. A mapping between standard logic and low voltage circuit input voltages.

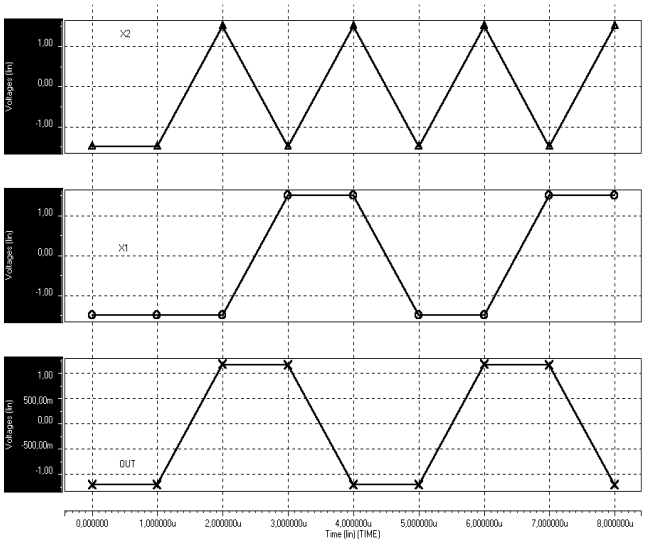

Figure 9. Simulation results of XOR circuit.

VI. CONCLUSION

In this work a modular neuron structure is introduced and applied effectively. The simulation results of the XOR application circuit proved the efficiency of the proposed neuron circuit and cascadebility of it. FGMOS based

proposed neuron circuit has single block summation and activation function realization advantage. For complex neural hardware implementations or neural integrated circuit realizations this neuron block can be used accurately

REFERENCES

1. T. Shibata and T. Ohmi, A functional MOS transistor featuring gate-level weighted sum and threshold operations, IEEE Trans. Electron Devices, vol. 39, pp. 1444–1455, June 1992.
2. Y. Berg and T. S. Lande, Programmable floating-gate MOS logic for low-power operation, in Proc. IEEE Int. Symp. Circuits and Systems, Hong Kong, 1997, pp. 1792–1795.
3. M. Lanzoni, G. Tondi, P. Galbiati, and B. Ricco, Automatic and continuous offset compensation of MOS operational amplifiers using floating-gate transistors, IEEE J. Solid-State Circuits, vol. 33, pp. 287–290, Feb. 1998.
4. Y. Liming, S. H. K. Embabi, and E. Sanchez-Sinencio, A floating-gate MOSFET D/A converter, Proc. IEEE Int. Symp. Circuits and Systems ISCAS'97, pp. 409–412, 1997.
5. K. Yang and A. G. Andreou, The multiple input differential amplifier based on charge sharing on floating-gate MOSFET, Anal. Integr. Cir-cuits Signal Process., vol. 6, pp. 197–208, 1994.
6. S. Vlassis and S. Siskos, Differential-Voltage Attenuator Based on Floating-Gate MOS Transistors and Its Applications, IEEE Transactions on Circuits and Systems-I, 48(11),. 1372-1378, 2001.
7. S. Yan and E. Sanchez-Sinencio, Low Voltage Analog Circuit Design Techniques: A Tutorial, IEICE Trans.Analog Integrated Circuits and Systems,vol. E00 –A, no.2, Feb. 2000
8. S. Vlassis and S. Siskos, Analogue squarer and multiplier based on floating-gate MOS transistors, Electron. Lett., vol. 34, pp. 825–826, Feb. 1998.
9. H. R. Mehrvarz and C. Y. Kwok, A novel multi-input floating-gate MOSfour-quadrant analog multiplier, IEEE J. Solid-State Circuits, vol. 31, pp. 1123–1131, Aug. 1996.
10. İ. Bayraktaroğlu, A. S. Öğrenci, G. Dündar, S. Balkır and E. Alpaydın, ANNSyS: an Analog Neural Network System, Neural Networks 12, 325-338, 1998.
11. G. Giustolisi, G. Palmisano, and G. Palumbo, A novel CMOS voltage squarer, in Proc. IEEE Int. Symp. Circuits and Systems ISCAS'97, 1997, pp. 253–256.