A New 7th-Order Log-Domain Elliptic Video Filter Using E-Cell Circuits Approach

Murat Dindar[1], Ali Kircay[2], and Erkan Yuce[3]

[1]TUBITAK National Observatory, 07058 Antalya, Turkey
murat.dindar@tubitak.gov.tr
[2]Harran University, Electrical and Electronics Engineering, 63000 Sanliurfa, Turkey
kircay@harran.edu.tr
[3]Pamukkale University, Electrical and Electronics Engineering, 20070 Denizli, Turkey
eyuce@pau.edu.tr

Abstract

This study proposes a new current-mode class-A log-domain elliptic filter for video frequency applications. The design is based on the topological simulation of the passive prototypes by using E-cells. The proposed filter has *3.42 MHz* cut-off frequency with maximum *0.119 dB* passband ripple and attenuation greater than *40 dB* at *4.78 MHz*. Only BJTs and grounded capacitors were implemented and operated with the symmetrical power supply of *±1.5 V*. The cut-off frequency of the filter can be electronically tuned by changing external currents. SPICE simulations are given to confirm the theoretical design results. The proposed filter is simulated by using both idealized BJT models and AT&T CBIC-R type transistors.

1. Introduction

Log-domain filtering is an important technique for realizing high-performance current-mode analogue signal processing systems [1-3]. The nature of the log-domain filter is that it uses the companding whereby the signals at the input are compressed by the logarithmically, processed by the log-domain filter core and expanded by the exponentially at the output stage. The compression and expansion processes are implemented by using the I-V characteristic of BJT or MOS transistor operated in the subthreshold region [2-7]. Log domain filters are of interest, mainly due to their suitability for low voltage, low power, low impedance levels, large dynamic range, high frequency applications and for being electronically tunable [1-7].

In the typically log-domain class-A operation, the actual AC signal I_{out} is superposed on the DC bias current I_{DC} and the dc equilibrium solution for the all nodes must be strictly positive [3]. It is easy to hold the input at positive; but for all nodes at the circuit, it will be difficult. In the literature, dc equilibrium problem can be solved by the solution mentioned by [3], but the higher filter design is, the more complex solution is needed. For that reason, simulating the topology of the passive prototype by using E-cell method is so quick and simple design method that it is chosen from all the others [4].

In the literature, several elliptic video filters have been reported up to now, [5-7]. To the best knowledge of the authors, proposed filter is the first 7th-order current-mode class-A log-domain elliptic lowpass filter by the simulating the topology of the passive prototype by using E-cell method for the video frequency applications. The advantages of the proposed filter are that the passband ripple is about *0.119 dB* and operated as class-A filter type. Only BJTs and grounded capacitors are required in order to realize the filter and operated with symmetrical power supply of *±1.5 V*. It has a lower THD value due to the advantages of log domain and Monte Carlo analysis is given for the BJT parameters.

2. The Proposed 7th-Order Log-Domain Elliptic Video Filter Using E-Cell Circuits

E-cell blocks are used to simulate the passive elements in order to design high order filters because of the quick and simple design methodology. As a consequence of the literature survey, the most popular E-cell blocks are chosen to design the proposed filter and the analysis of them will be given this section.

The main idea of the simulating passive elements is to be fulfilled the two conditions: a) The current that flows into the terminal of the passive element should be equal to the current that flows into the simulated active one, b) The voltage at the each terminal of the passive element should be also equal to voltage at the each terminal the simulated active one [4].

In the literature, the elliptic filters designed by using simulating passive elements topology are generally LC ladder filter type as shown in Fig. 1. Therefore, the passive elliptic filter is chosen in concordance with the video standards defined by ITU 601. According to the chosen passive elliptic filter prototype, the passive elements to be simulated are floating inductor, floating capacitor, grounded capacitor and the grounded resistor.

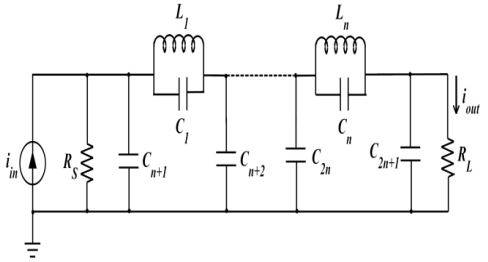

Fig. 1. General current-mode LC ladder elliptic lowpass filter prototype

The linear operation of the whole filter can be achieved by fulfilling the conditions, a and b; under these circumstances the mapping could be done from linear domain to log domain by using the equivalent of the passive elements. For the mapping from the linear domain (1) to the log domain (2), the voltage expressions and the current in log domain (3) could be defined as

$$v = EXP(\hat{v}) = V_T e^{\hat{v}/V_T} - V_T \tag{1}$$

$$\hat{v} = LOG(v) = V_T In\left(\frac{v + V_T}{V_T}\right) \tag{2}$$

$$\hat{i} = I_0 e^{\hat{v}/V_T} - I_0 \tag{3}$$

Using (1), (2) and (3), the passive elements could be easily simulated by using E – cells shown in single – input positive exponential transconductor cell (Fig. 2), single – input negative exponential transconductor cell (Fig. 3), dual – input positive exponential transconductor cell (Fig. 4) and dual – input negative exponential transconductor cell (Fig. 5).

In the linear domain the equation of grounded resistor could be defined as

$$i = \frac{v}{R} \tag{4}$$

By using (1), the equation could be transformed into the log domain (5)

$$\hat{i} = \frac{EXP(\hat{v})}{R} = \frac{V_T e^{\hat{v}/V_T} - V_T}{R} \tag{5}$$

Above equation (5) can be arranged by using definition in equation (6) as the following equation (7)

$$R = \frac{V_T}{I_0} \tag{6}$$

$$\hat{i} = I_0 e^{\hat{v}/V_T} - I_0 \tag{7}$$

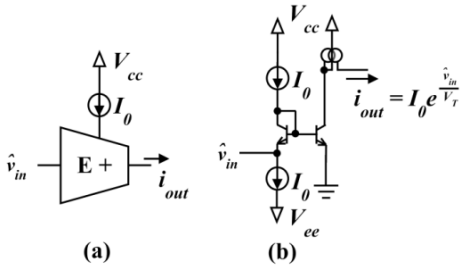

Fig. 2. Single – input positive exponential transconductor cell (E+ cell). (a) Used symbol (b) Transistor level representation

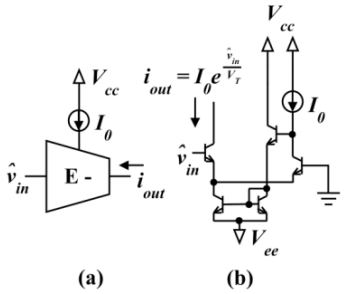

Fig. 3. Single – input negative exponential transconductor cell (E- cell). (a) Used symbol (b) Transistor level representation

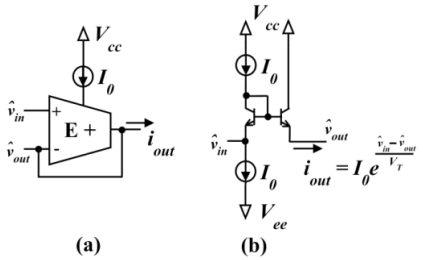

Fig. 4. Dual – input positive exponential transconductor cell (E+ cell). (a) Used symbol (b) Transistor level representation

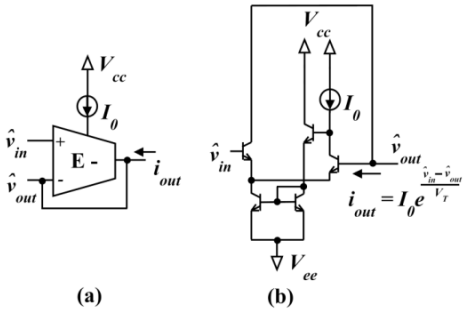

Fig. 5. Dual – input negative exponential transconductor cell (E- cell). (a) Used symbol (b) Transistor level representation

According to (7), the grounded resistor can be easily realized by taking into the account (1), (3) as shown the following figure (Fig. 6).

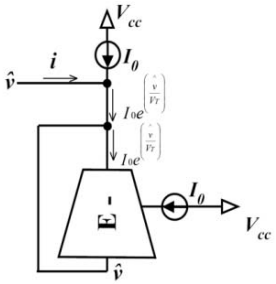

Fig. 6.E-cell grounded resistor

In order to realize the capacitor and inductor elements in the log domain, the equations in derivative and integral forms are

needed to obtain because of the characteristics of the capacitor and inductor in linear domain. Therefore, (8) could be simply defined so as to derive the those elements,

$$\hat{C}\frac{d\hat{v}_c}{dt} = I_0 e^{\frac{\hat{v}_a - \hat{v}_c}{V_T}} - I_0 e^{\frac{\hat{v}_b - \hat{v}_c}{V_T}} \tag{8}$$

By using (1), the capacitor voltage could be defined in log domain as (9)

$$v_c = EXP(\hat{v}_c) = V_T e^{\hat{v}_c / V_T} - V_T \tag{9}$$

(10) could be obtained by using (9), (8) and multiplying both side of the equation with the term $\frac{V_T}{I_0} e^{\hat{v}_c / V_T}$

$$\frac{dEXP(\hat{v}_c)}{dt} = \frac{I_0}{\hat{C} V_T}\left(EXP(\hat{v}_a) - EXP(\hat{v}_b) \right) \tag{10}$$

The capacitor and inductor elements could be realized by using (10) easily. In order to realize the grounded and floating capacitor, the $\hat{v}_b$ should be connected the ground.(10) can be arranged by using (1) for $\hat{v}_a$

$$\hat{i} = C\frac{dEXP(\hat{v}_c)}{dt} = I_0 e^{\hat{v}_a / V_T} - I_0 \tag{11}$$

The log domain equivalent of the grounded (Fig. 7) and floating (Fig. 8) capacitor could be implemented easily by achieving only voltage and current expressions (10) and (11) because of the derivative characteristic of the capacitor.

$$\frac{dEXP(\hat{v}_c)}{dt} = \frac{dEXP(\hat{v})}{dt} \tag{12}$$

$$\frac{dEXP(\hat{v}_c)}{dt} = \frac{d}{dt}\left[EXP(\hat{v}_1) - EXP(\hat{v}_2) \right] \tag{13}$$

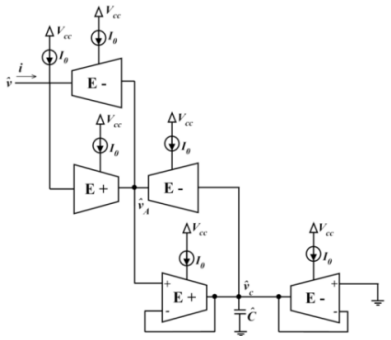

Fig. 7.E-cell grounded capacitor

As can be seen at Fig. 7 and Fig. 8, (11), (12) for grounded capacitor and (11), (13) for the floating capacitor are achieved.

Therefore, the capacitor value in linear domain is equal to the log domain equivalent one.

.

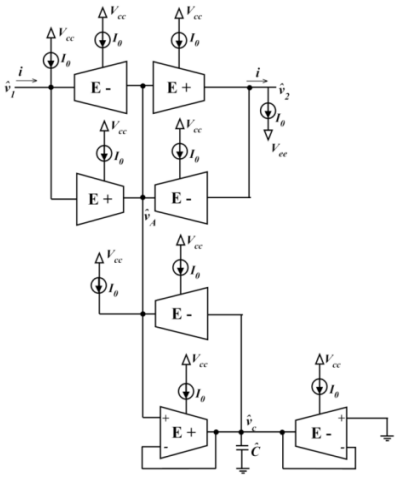

Fig. 8.E-cell floating capacitor

In order to get the log domain equivalent of the inductor, (10) could be arranged by integrating both side, then make the left side of the expression (10) alone

$$EXP(\hat{v}_c) = \frac{I_0}{\hat{C} V_T}\int\left(EXP(\hat{v}_a) - EXP(\hat{v}_b) \right) \tag{14}$$

The current that flows through the log domain floating inductor could be defined as (15)

$$\hat{i} = I_0 e^{\hat{v}_c / V_T} - I_0 = \frac{V_T}{I_0} EXP(\hat{v}_c) \tag{15}$$

(14) could be manipulated by using (15) and the log domain floating inductor value can be found as (17)

$$\hat{i} = \frac{1}{\frac{\hat{C} V_T^{\,2}}{I_0^{\,2}}}\int\left(EXP(\hat{v}_a) - EXP(\hat{v}_b) \right) \tag{16}$$

$$L = \frac{\hat{C} V_T^{\,2}}{I_0^{\,2}} \tag{17}$$

The log domain floating inductor could be realized by using the current definition in (16). The value of the log domain floating inductor can be easily found by using (17).

As can been at (Fig. 9), the current that flow through the element in log domain also should be taken into account as defined in (3).

The passive elliptic video filter was chosen as following figure (Fig. 10) for video frequency application [7]. According to the passive filter, all log domain equivalent of elements were calculated and given at "Table 1". The log domain design of the elliptic filter (Fig. 11) were implemented the log domain equivalent of the passive elements which were given at this section.

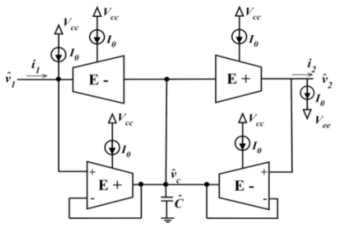

Fig. 9.E-cell floating inductor

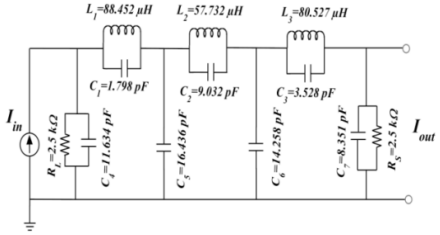

Fig. 10. Passive elliptic video filter

3. Simulation Results

The proposed 7th-order elliptic lowpass filter was simulated with PSPICE simulation program by using ideal transistor models, β_F equal to 1000, and AT&T CBIC – R type transistors. The circuit parameters are chosen as, the value of the capacitors were given at "Table 1", V_{cc} = *+1.5 V*, V_{ee} = *-1.5 V*, I_0 = *10.24* µA for grounded resistor value in log domain; I_0 = *25 µA* for floating inductor and capacitor, grounded capacitor values in log domain; V_T = *25.6 mV*, f_0 = *3.42 MHz*, α_{min} > *40 dB*, α_{max} = *0.119 dB* and ω_s/ω_p= *1.4*.

The DC current, I_{DC} = *40.96 µA*, source is used for bias in the *I-V conversion and compression (input grounded resistor, R_L) circuit* in order to obtain for class-A operation at log-domain. The gain response of the elliptic filter is shown in Fig. 12. Maximum passband ripple (α_{max}= *0.119 dB*) is shown in Fig. 13. The cut – off frequency of the filter can be electronically tuned by changing external currents as shown in Fig. 14. The cut – off frequency could be tuned from *1 MHz* to *15 MHz*.

Table 1. The value of the passive and log domain elements

	Passive LC Ladder	Log Domain
$R_L = R_S$	2.5 kΩ	2.5 kΩ
C_1	1.738 pF	1.738 pF
L_1	88.452 µH	88.452 pF
C_2	9.032 pF	9.032 pF
L_2	57.372 µH	57.372 pF
C_3	3.528 pF	3.528 pF
L_3	80.527 µH	76.823 pF
C_4	11.634 pF	11.634 pF
C_5	16.436 pF	16.436 pF
C_6	14.258 pF	14.258 pF
C_7	8.351 pF	8.351 pF

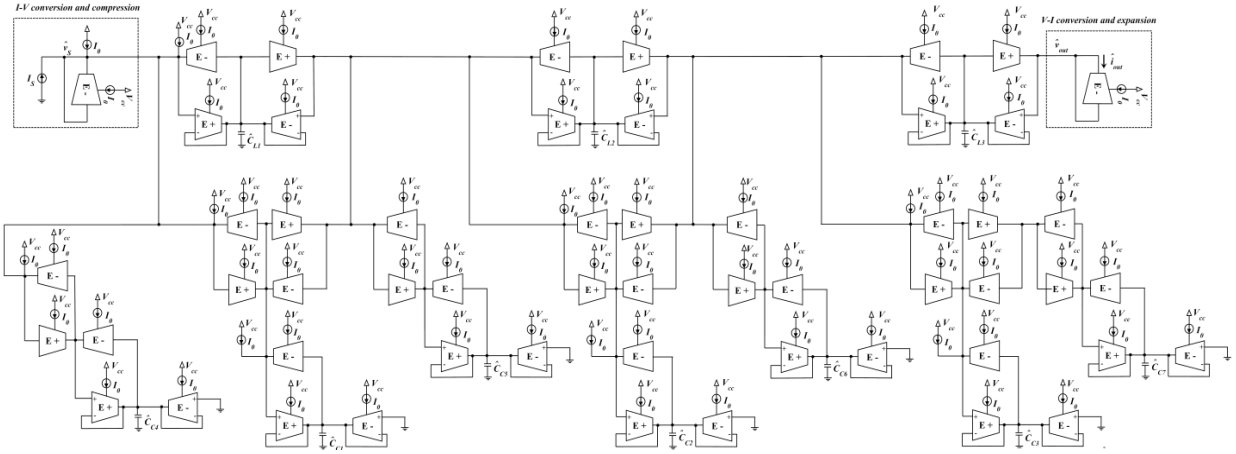

Fig. 11. The proposed log domain elliptic lowpass video filter

The power consumption of the proposed filter is 12.2 mW. Filter distortion is also investigated using PSPICE program. For this purpose an input current with a modulation index factor ($m = i_{s,peak}/I_0$) which was calculated and THD (Total Harmonic Distortion) is given according to *m* in Fig. 15.

PSPICE program was used to perform Monte Carlo analysis for the important parameters of the proposed filter as; 10% tolerance on the resistances (R_B, R_C, R_E) of BJTs, 25% tolerance on the current gains β_F, 20% tolerance on the currents I_S, 20% tolerance on Early voltages V_{AF}, 20% tolerances on the grounded capacitors (Fig. 16).

Log domain filter suffer from transistor – level effects such as parasitic emitter and base resistance, finite β_F, Early voltage and area mismatched. Up to now, several simple electronic compensation circuits were design for this purpose [8]. As can be seen in Fig. 14, the gain response of the CBIC – R transistor filter has attenuation because of the transistor level effects.

Those effects are clearer on the E – cell design of the simulated passive topologies [4, 8]. Those effects also can be seen on the tuning performance of the filter, because the design method depends on the values of the elements which are used in the passive design.

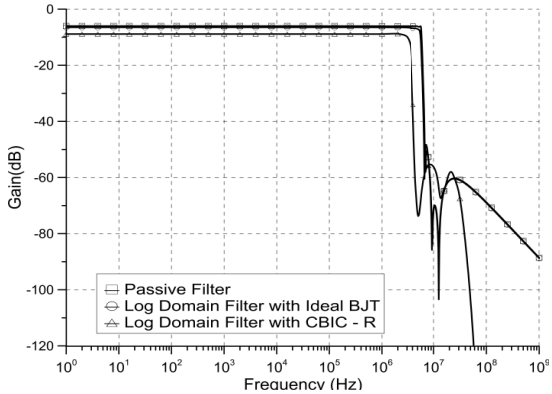

Fig. 12. The gain response of the proposed elliptic filter

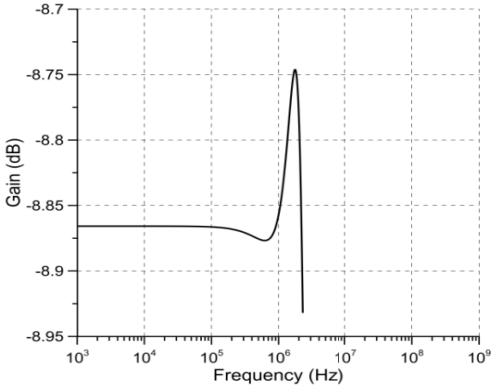

Fig. 13. Maximum 0.119 dB passband ripple

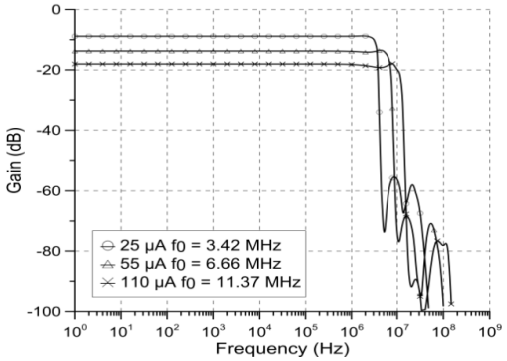

Fig. 14. The tuning characteristic of the proposed filter

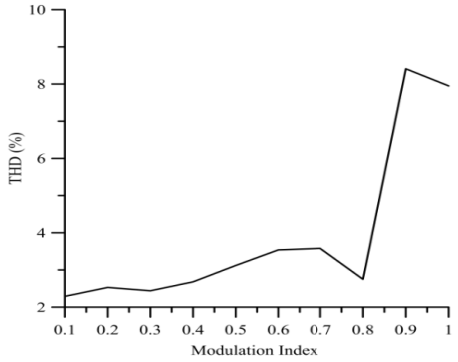

Fig. 15. Total harmonic distortion of the filter

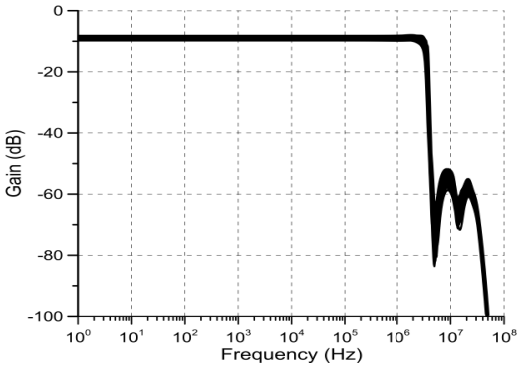

Fig. 16. Gain response of the proposed elliptic lowpass filter under different parameter tolerances

4. Conclusion

A new current mode 7th – order class-A elliptic lowpass filter is proposed in this study. The proposed filter is designed by using the simulating the passive prototypes with E-cells. The specifications of the filter are suitable for the video frequency operations determined by ITU 601 standards.

5. References

[1] R. Adams, "Filtering in log-domain", in *63rd Audio Engineering Society Conf.*, New York, 1979, Preprint#*1470*.

[2] D. R. Frey, "Log-domain filtering: An approach to current – mode filtering", *Circuits and Systems Devices*, *IEE Proceedings – G,* vol. *140*, no. *6*, pp. *406 – 416*, 1993.

[3] E. M. Drakakis, A. J. Budett, "Operational dc constraints for a class – A, third order, observer canonical – form log domain filter", *Circuits and Systems I: Fundamental Theory and Applications*, vol.*50*, no. *10*, pp. *1337 – 1342*, 2003.

[4] N. Kontogiannopoulos, C.Psychalinos, "Log – Domain Filtering by Simulating the Topology of Passive Prototypes", *IEEE Transactions On Circuits And Systems—I: Regular Papers*, v. *52*, no. *10*, pp. *2043 – 2054*, 2005.

[5] V. Gopinatham, Y. Tsividis, K. –S. Tan, R. K. Hester, "Design considerations for high – frequency continuous – time filters and implementation of an antialiasing Filter for digital video", *IEEE Journal of Solid – State Circuits*, vol.*25*, no. *6*, pp. *1368 – 1378*, 1990.

[6] A. Kircay, U. Cam, "A new 5th – order differential type class AB log-domain elliptic lowpass filter for video frequency applications", Analog Integrated Circuits Signal Processing, vol.60, no. 3, pp. 221–229, 2009.

[7] A. Uygur, H. Kuntman, "7th – order elliptic video filter with 0.1 dB passband ripple employing CMOS CDTAs", *International Journal of Electronics and Communications,* vol. *61*, no. 5, pp. *320 – 328*, 2007..

[8] G. W. Roberts, V. W. Leung, "Effects of transistor nonidealities on high – order log – domain ladder filter frequency responses", *IEEE Transaction on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. *47*, no. *5*, pp. *373 – 387*, 2000.