A NEW CMOS DIFFERENTIAL OTRA DESIGN FOR THE LOW VOLTAGE POWER SUPPLIES IN THE SUB-MICRON TECHNOLOGIES

Alper Duruk[1] Hakan Kuntman[2]
e-mail: alper.duruk@st.com *e-mail: kuntman@ehb.itu.edu.tr*

[1]*ST Microelectronics*
Değirmen Yolu Cad. Huzur Hoca Sok. No: 84 Kat: 24, İçerenköy, İstanbul

[2]*İstanbul Technical University, Department of Electrical & Electronics Engineering, Electronics and Communication Engineering, 80626, Maslak,İstanbul*

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ABSTRACT

In this study, a new CMOS differential OTRA topology is proposed. This topology can operate with a very low voltage power supply as 1.2V. In this design, CMOS 0.13 µm ST Microelectronics technology transistor models are used for the simulations. The designed CMOS OTRA has a transresistance gain (Rm) of 8657 V/I with a 36.29 MHz bandwidth (-3dB) and a transresistance unity-gain bandwidth of 2.91 GHz.

I. INTRODUCTION

The growing demand for mobile communications has led to high level of chip integration and directed research towards the field of high frequency applications. In the new designed circuit topologies for high frequencies, current-mode approach is preferred rather than the traditional voltage-mode structures. OTRA (Operational Transresistance Amplifier), which is commercially available under the name of Norton amplifier has been attracted attention by its advantages in the current-mode circuit design [1, 2]. Low input and output impedances, a bandwidth independent of the device gain can be considered the main advantageous properties of the OTRA. These commercial realizations don't provide a true virtual ground at the input terminals and they allow the input current to flow in one direction only. In order to remove these disadvantages of the OTRA, some topologies are proposed in the literature [3-8]. But these solutions are both complex structures and do not operate properly in the low power supplies like 1.2V in the sub-micron technologies. In todays technology, circuits which use power supplies as 1V, and fabricated in the CMOS 0.09 µm technology can be designed. So for the future design concept the main interest is designing circuitries with low power supplies. This demand leads designing a high performance differential OTRA for the current-mode analog systems design. For these reasons, using the ST Microelectronics CMOS 0.13 µm technology, a differential OTRA is designed for 1.2V power supply. This new differential OTRA topology is characterized by the CADENCE simulation tool and the characterictic results showing its high performance is given.

II. PROPOSED CMOS DIFFERENTIAL OTRA

The Differential Operational Transresistance Amplifier (OTRA) is a four terminal analog building block with a describing matrix in the form given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_{OA} \\ V_{OB} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ -R_m & R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_{OA} \\ I_{OB} \end{bmatrix} \quad (1)$$

Circuit symbol of the differential OTRA is illustrated in Figure 1.

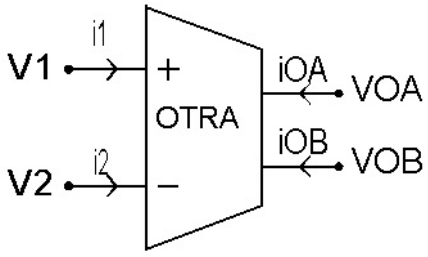

Figure 1: Circuit symbol of the differential OTRA

Both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded, leading to circuits that are insensitive to the stray capacitance as reported in [4].

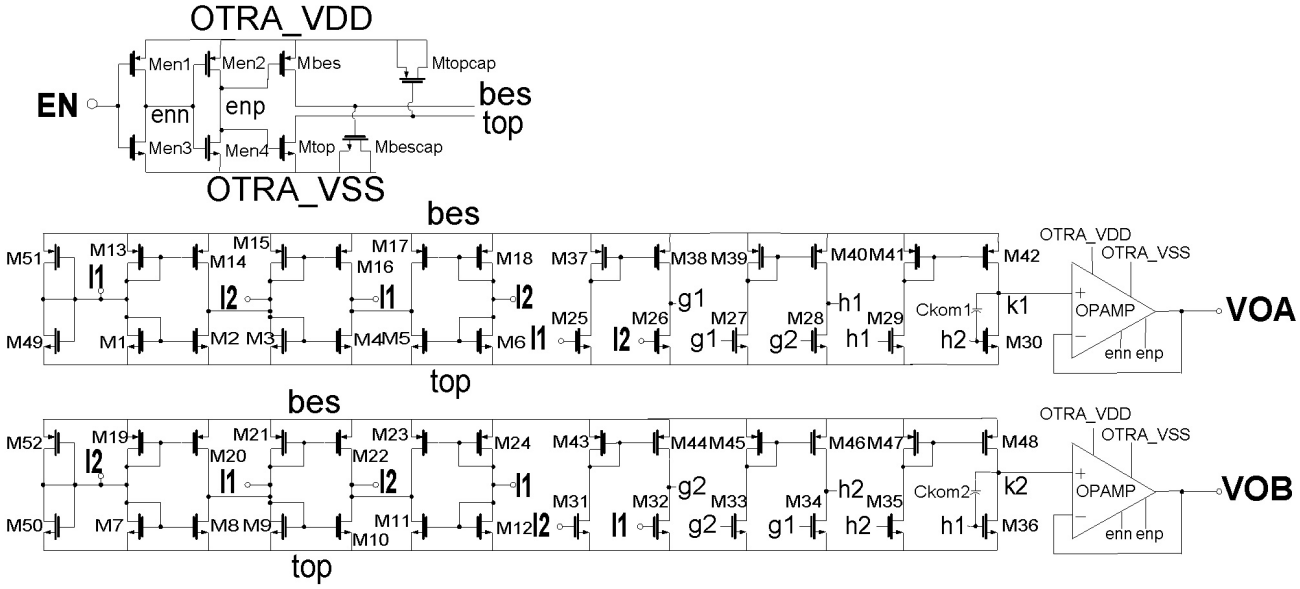

Figure 2: Proposed differential CMOS OTRA topology

For ideal operation, the transresistance gain, Rm approaches infinity forcing the input currents to be equal. Thus the OTRA must be used in a negative feedback configuration in a way that is similar to conventional op amps. OTRA has similar transmission properties to the current-feedback op-amp, but with two low-impedance inputs and two low-impedance output for the differential OTRA. Since the input terminals of these circuits are virtually grounded, they are suitable for cascade connection.

The proposed CMOS differential OTRA is shown in Figure 2. This circuitry also includes the four power-down transistors which creates the enabled power-supplies named as “bes” and “top”. OTRA is active when the “EN” input is at the VSS voltage level. When the “EN” input is at the VDD voltage level, all the system is in the power-down mode and the output “VOA” and “VOB” behaves as a high impedance output. Mbescap and Mtopcap are MOS capacitances, which filter the power supply to ground, and avoid nodes “bes” and “top” from being floating nodes in the power down mode.

This basic input cell consists of four transistors. These four transistors create two Class AB current mirror connection [8]. In the static state I1 and I2 are biased automatically to the half of the power supply. For this design the initial value for I1 and I2 is 0V as virtually grounded (in ±0.6V power supply operation). The input currents are directly connected to the I1 and I2 nodes. So the input currents directly flow through the drains of the transistors. If one basic cell is used, the OTRA input will not be symmetrical. Because, for the given basic cell, the input I1 is formed by the use of two diode connected NMOS (M9) and PMOS (M21) transistors, but at the input I2 there are no diode connections. For that reason, a second basic cell is placed into the design, by replacing the input pins, that input I2 is applied to the two diode connected input part of the basic cell and input I1 is applied to the other input as given in Figure 2 (the transistors M3, M4, M15 and M16 in the top-middle level). Afterwards in order to decrease the process variation effects and to have a stronger input part, four basic cells are also connected to this block as illustrated in Figure 2. Totally both inputs I1 and I2 are formed with three diode-connected NMOS, three diode-connected PMOS, and one not-diode-connected NMOS and one not-diode-connected PMOS transistors. The inputs I1 and I2 are also connected to the differential amplifier in the gain stage. This negative feedback is helping to decrease the input impedance in I1 and I2 nodes. Also one-pair of diode-connected NMOS and PMOS transistors which have large width values are connected both to the inputs I1 and I2 in order to decrease the input impedance of the I1 and I2 nodes which are the input nodes for the OTRA. This connection also can be thought as an inverter whose output is connected to its own input. The only disadvantage of this connection is using more current from the power supply.

The basic cell of the gain part is composed of four transistors, namely M25, M26, M37 and M38 as illustrated in Figure 2. This differential amplifier is not a classical amplifier with a fixed current source biasing the NMOS transistors M25 and M26. This amplifier can work independent of any fixed current. This cell is converting the two input differential signals to one single ended signal.

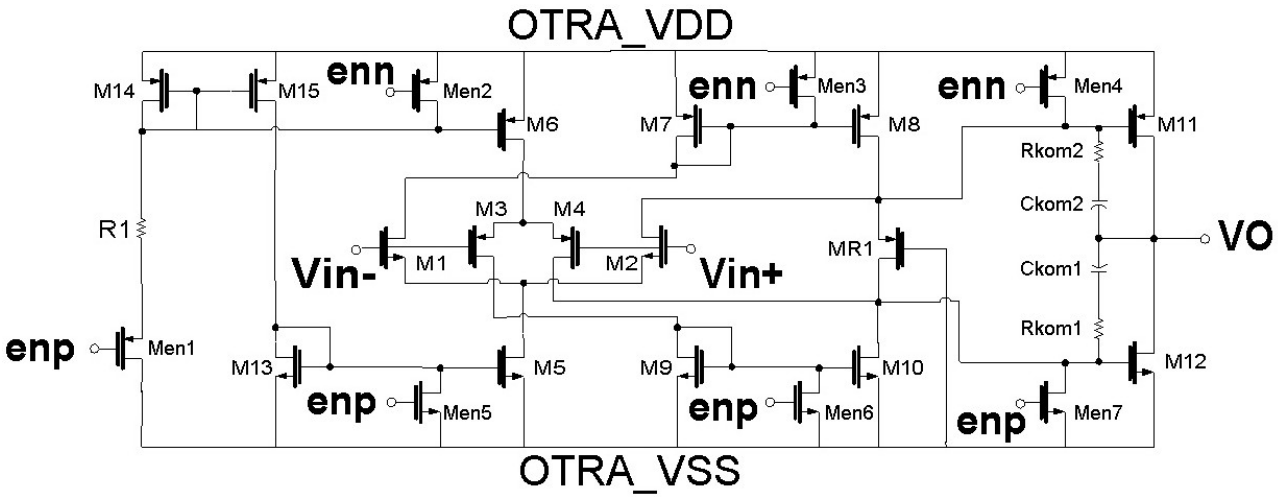

Figure 3: New proposed opamp used in the as a unity gain output buffer

In order to have a symmetrical output in g1 and g2 nodes, two basic cells are used within the same idea in the input part of the OTRA. For the second basic cell which consist with the transistors M31, M32, M43 and M44 in Figure 2, the input pins reversed. So both I1 and I2 input directly connected to one diode-connected PMOS (M37 and M43) and one not-diode-connected PMOS (M44 and M38). The first gain outputs which are "g1" and "g2" in names, are connected to the second same structured gain stage like the first gain stage. The outputs of the second gain stage which are "h1" and "h2" in names, are connected to the third, same structured gain stage as the first gain stage. The outputs of the third gain stage which are "k1" and "k2" in names are the non-buffered dual outputs of differential OTRA.

The non-buffered dual outputs are buffered with the unity-gain configuration by using OPAMP which is shown in Figure 3. The VOA is the same functional output as the VO in the classical single output OTRA, VOB is the dual output of VOA, which is just differ from the VOA output in the phase level.

III. SIMULATION RESULTS

The proposed CMOS differential OTRA, is simulated in the CADENCE simulation program, with the ST Microelectronics CMOS 0.13 μm technology *spectre* models by using the transistor and element values listed in Table 1 for OTRA and Table 2 for OPAMP. Power supply is used as ± 0.6V.

The typical dc simulation results are shown in Figure 4 and Figure 5. According to these results the maximum output voltages are reached with at least 200 μA of input difference current. The maximum output voltage in the dc analysis is 0.469mV, and the minimum output voltage is -0.470mV with 200μA input current. Another typical dc test simulation result is shown in Figure 6. According to these result, it is shown that this OTRA can work within the limits of -2 mA and 2 mA. If one of the input node is biased with more 2 mA, it is also possible to work. But the 2mA input current limit will be more than enough for a classical operation. The normalized transresistance gain is shown in Figure 7. The transresistance gain is 8657 V/I. The -3 dB point of the transresistance gain is at 36.29 MHz. It is a good range for the CMOS 0.13μm technology. Also the unity gain-bandwidth is 2.91 GHz. This bandwidth region gives the oppurtunity of designing high bandwidth filters and inductance simulators.

The performance characteristics of the CMOS differential OTRA is shown at the Table 3.

IV. CONCLUSION

In this study, a new CMOS differential OTRA for the low power supplies like 1.2V is proposed. This current-mode active element is suitable for high frequency applications, including filter, inductance simulator applications. Characterization simulations of the differential OTRA is done with the CADENCE tool and 36.29 MHz transresistance gain bandwidth is achieved.

This CMOS differential OTRA structure is also very suitable for the high frequency (up to 3.2 GHz) differential signaling receiver I/O circuitry in the *SONET / SDH* (Synchronous Optical Network / Synchronous Digital Hierarchy) or *XAUI* (10 Gigabit Attachment Unit Interface – 10 Gigabit Ethernet) chipsets. Both LVDS (Low voltage differential signaling) and CML (Current-mode logic) receivers can be easily designed by removing the large input diode-connected transistors and by replacing the buffers connected to the output with the inverter based buffer chains. These input and output structures in OTRA, which are removed for the receiver I/O circuitry, have the function of lowering the input and the output resistances to very low values.

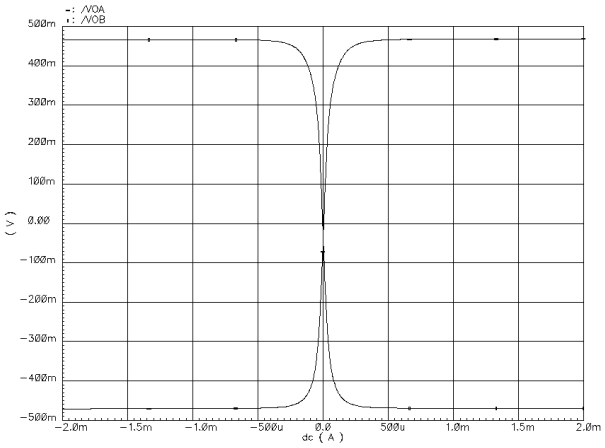

Figure 4: Typical dc simulation result of OTRA

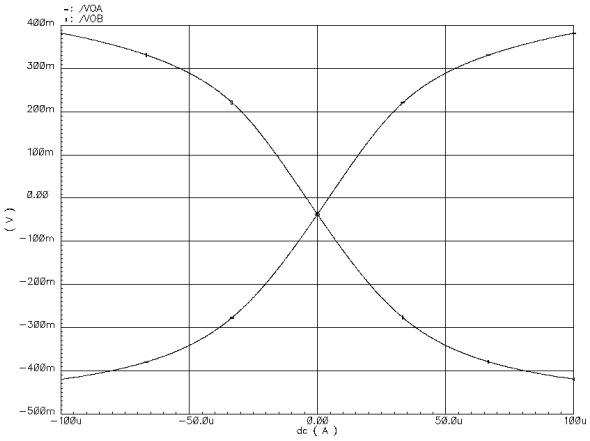

Figure 5: Zoomed typical dc simulation result of OTRA

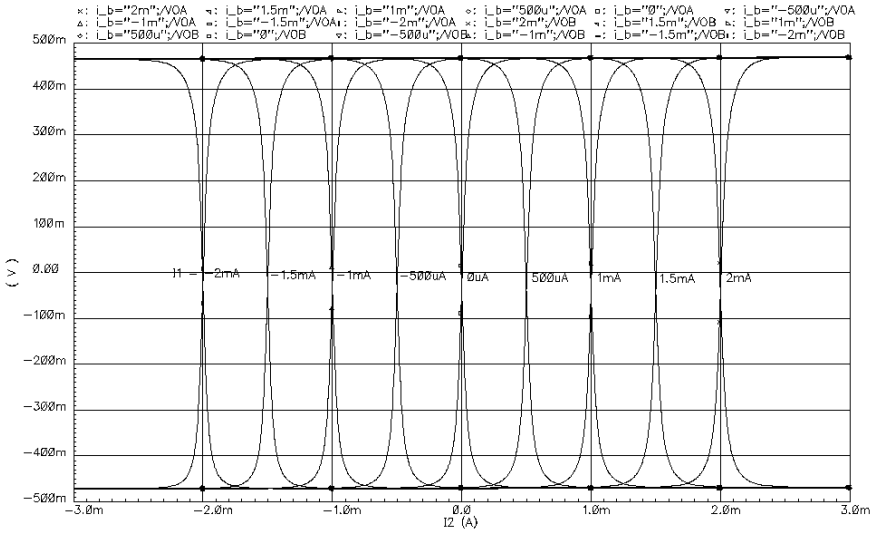

Figure 6: Typical dc simulation result of OTRA with different I1 input current

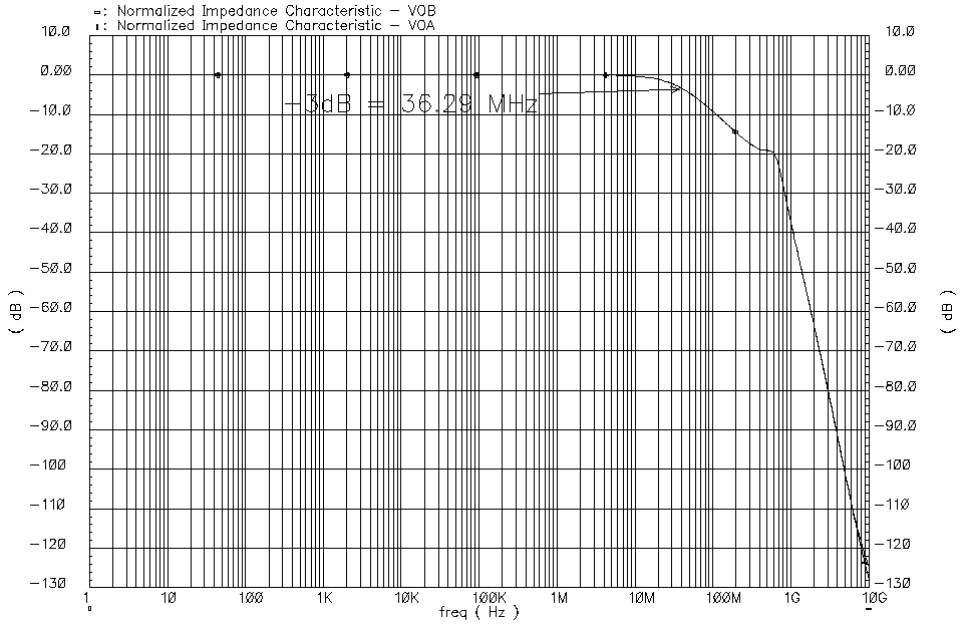

Figure 7: Typical ac simulation result, transresistance gain of the OTRA in a normalized axis

Table 1: Transistor dimensions (W/L) in the proposed CMOS OTRA

Transistor name	W / L
M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12	3.4 µm / 0.15 µm
M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24	7.2 µm / 0.15 µm
M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36	0.85 µm / 0.15 µm
M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48	1.8 µm / 0.15 µm
M49, M50	108.8 µm / 0.15 µm
M51, M52	230.4 µm / 0.15 µm
Men1, Men2	28.8 µm / 0.13 µm
Men3, Men4	13.6 µm / 0.13 µm
Mbes	490 µm / 0.15 µm
Mtop	170 µm / 0.15 µm
Mbescap, Mtopcap	67.84 µm / 5.28 µm
Other devices	**Value**
Ckom1, Ckom2	15 fF

Table 2: Transistor dimensions (W/L) and other devices values in the proposed OPAMP

Transistor name	W / L
M1, M2	8.5 µm / 0.3 µm
M3, M4	18 µm / 0.3 µm
M5	13.6 µm / 0.4 µm
M6	28.8 µm / 0.4 µm
M7, M8	5.1 µm / 0.3 µm
M11	360 µm / 0.3 µm
M12	170 µm / 0.3 µm
M13	3.4 µm / 0.3 µm
M14, M15	7.2 µm / 0.3 µm
MR1	2 µm / 4 µm
Men1	43.2 µm / 0.13 µm
Men2, Men3, Men4	0.4 µm / 0.13 µm
Men5, Men6, Men7	3.4 µm / 0.13 µm
Other devices	**Value**
Ckom1, Ckom2	100 fF
Rkom1, Rkom2	2.5 KΩ
R1	6 KΩ

Table 3: Performance of the proposed CMOS OTRA

Power supply	± 0.6V
Maximum output voltage	0.469 V
Minimum output voltage	-0.470 V
Input resistance	$R\_I_1 = R\_I_2 = 10.5\ \Omega$
Output resistance	0.9 Ω
Input offset current	4.29 µA
Transresistance gain (Rm) (DC)	8657 V/I
Transresistance gain bandwidth (-3dB)	36.29 MHz
Transresistance unity gain-bandwidth	2.91 GHz
Power consumption	29.85mA, 35.82 mW
Expected silicon area	60 µm × 50 µm

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