CURRENT-MODE UNIVERSAL FILTER IMPLEMENTED WITH DVCCs

Çağrı Temizyürek[1] Indrit Myderrizi[2]
e-mail: ctemizyurek@yahoo.com e-mail:myderrizi@itu.edu.tr
[1]*Istanbul University, Faculty of Engineering, Department of Electrical & Electronics Engineering, 34850, Avcilar, Istanbul, Turkey*
[2] *Istanbul Technical University, Faculty of Electrical and Electronic Engineering, Electronics Engineering, 34469, Maslak, Istanbul, Turkey*

Key words: Current-mode, dvcc, universal filter

ABSTRACT

In this paper, the implementation of a current-mode universal filter by using DVCCs and all grounded passive elements is described. The circuit can simultaneously realize low-pass, high-pass, and band-pass filter functions without changing the circuit topology and elements. It has the possibility of independent adjusment of ω_0 without disturbing ω_0/Q. PSPICE simulations are performed employing a standard CMOS technology (0.5µ Mietec) and the performance of the simulation results is tested by comparing with the results of the ideal filter's simulation.

I. INTRODUCTION

Current-mode circuits have been receiving considerable attention owing to their potential advantages such as wider bandwidth, greater linearity, higher slew-rate, wider dynamic range, simple circuitry and low power consumption compared to voltage-mode circuits [1]. Current-mode filters have been found wide applications in instrumentation, analogue signal processing, automatic control and communication. The advantages in the realization of current-mode filters using current conveyors have received significant attention [2]. Thus, several multifunction or universal biquadratic filters using current conveyors have been reported in the literature. The first universal current conveyor active biquad was designed by Toumazou and Lidgey [3]. Since then a number of circuit realizations for universal current-mode current conveyor based filters were proposed [4-7]. Among the several variations of current conveyor, the most successful type is second-generation current conveyor (CCII) introduced by Sedra and Smith [8]. However, conventional CCII cannot be used in applications demanding differential or floating inputs like impedance converter circuits and current-mode instrumentation amplifiers, where as the design of amplifier requires two or more CCIIs. Considering drawbacks of CCIIs, a new building block called a differential difference current conveyor (DDCC) was presented in 1996 [9]. In 1997, a novel differential voltage current conveyor (DVCC) building block was introduced [10]. DVCC is a very versatile building block whose applications exist in the literature [11-15].

In this paper, by using two DVCCs and all-grounded five passive elements, a universal filter is implemented. PSPICE simulation of the CMOS DVCC universal filter is performed to demonstrate the results. The obtained simulation results for the implemented universal filter are compared with the ideal filter's simulation results.

II. DVCC

The DVCC is a five-port building block which is defined by the following matrix equation [10].

$$\begin{bmatrix} V_X \\ I_{Y+} \\ I_{Y-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y+} \\ V_{Y-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

An ideal DVCC building block is shown by the use of symbol in Figure 1.

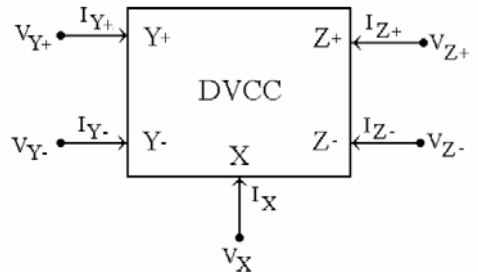

Figure 1. Symbol of the DVCC

The CMOS realization [10] of the DVCC used in this paper for the universal filter implementation is shown in Figure 2.

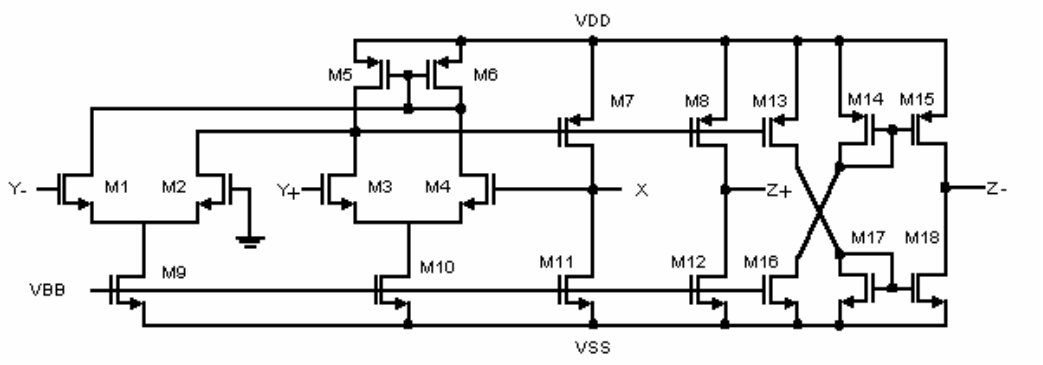

Figure 2. CMOS realization of the DVCC

III. CMOS DVCC FILTER IMPLEMENTATION

The implemented current-mode universal filter is illustrated in Figure 3. Using the standard notation, the DVCC characteristics can be described by $I_{y+}=I_{Y-}=0$, $Vx=V_{Y+} - V_{Y-}$, $I_{z+}=I_x$, $I_{z-}=-I_x$. Routine analysis of the circuit yields the following current transfer functions:

$$\frac{I_{LP}}{I_{in}} = \frac{1/C_1C_2R_1R_3}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{2}$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{3}$$

$$\frac{I_{BP}}{I_{in}} = \frac{s/C_2R_3}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{4}$$

where the pole natural frequency and pole quality factor of the implemented filter are expressed as

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_3}}, \tag{5}$$

$$\frac{\omega_0}{Q} = \frac{1}{C_2R_2} \tag{6}$$

$$Q = \frac{C_2R_2}{\sqrt{C_1C_2R_1R_3}} \tag{7}$$

Thus, second order current-mode low-pass, high-pass, and band-pass filter characteristics given respectively by Eqs. (3), (4) and (5) can be simultaneously realized without changing the circuit configuration. By adding I_{LP} and I_{HP} outputs, the transfer function can be organized giving a notch filter transfer function as follows:

$$\frac{I_{notch}}{I_{in}} = \frac{I_{HP} + I_{LP}}{I_{in}} = \frac{s^2 + 1/C_1C_2R_1R_3}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{8}$$

From Eqs. (5), (6), and (7), it can be seen that ω_0 can be adjusted independently from ω_0/Q by changing the value of R_3. Also, the quality factor Q can be adjusted by changing the grounded resistance R_2 without affecting the pole natural frequency ω_0.

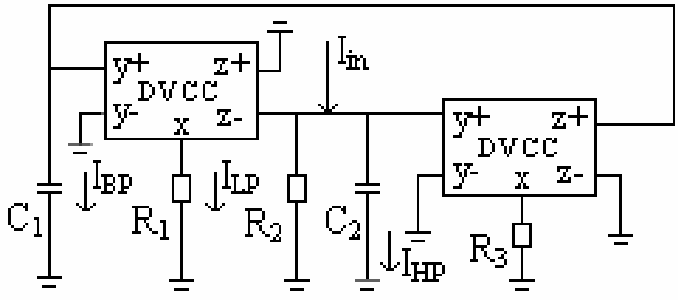

Figure 3. Universal filter

IV. SIMULATION RESULTS

To verify theoretical analysis the implemented circuit has been simulated using PSPICE program by using 0.5μ Mietec technology process parameters. The circuit in Figure 3 was used to realize low-pass, high-pass, band-pass, and notch filters exhibiting a Butterworth characteristic with a cutoff frequency of 255kHz. The all-grounded passive elements of the filter were chosen as $C_1=C_2=1nF$, $R_1=1k$, and $R_2=R_3=0.5k$. The supply voltages were taken as $V_{DD}=2.5V$ and $V_{SS}=-2.5V$. The biasing voltage V_{BB} was taken as -1.7V. The PSPICE simulation results given in Figure 4 for the low-pass, high-pass, and band-pass filter characteristics and in Figure 5 for the notch filter characteristic verify the theoretical analysis.

As it can be seen from Figure 4 and Figure 5, the pole natural frequency is in a good agreement with the frequency calculated using the derived analytical formula given by Eq. (5).

V. CONCLUSION

In this paper, a current-mode universal filter implemented with two DVCCs and five all-grounded passive elements is introduced. The filter can simultaneously realize low-pass, high-pass, and band-pass filter functions without changing the topology and elements. A notch filter characteristic can also be obtained by getting a suitable output. Also, the adjustment of bandwidth and quality factor without affecting each other is possible. The workability of the filter is confirmed by the PSPICE simulation results.

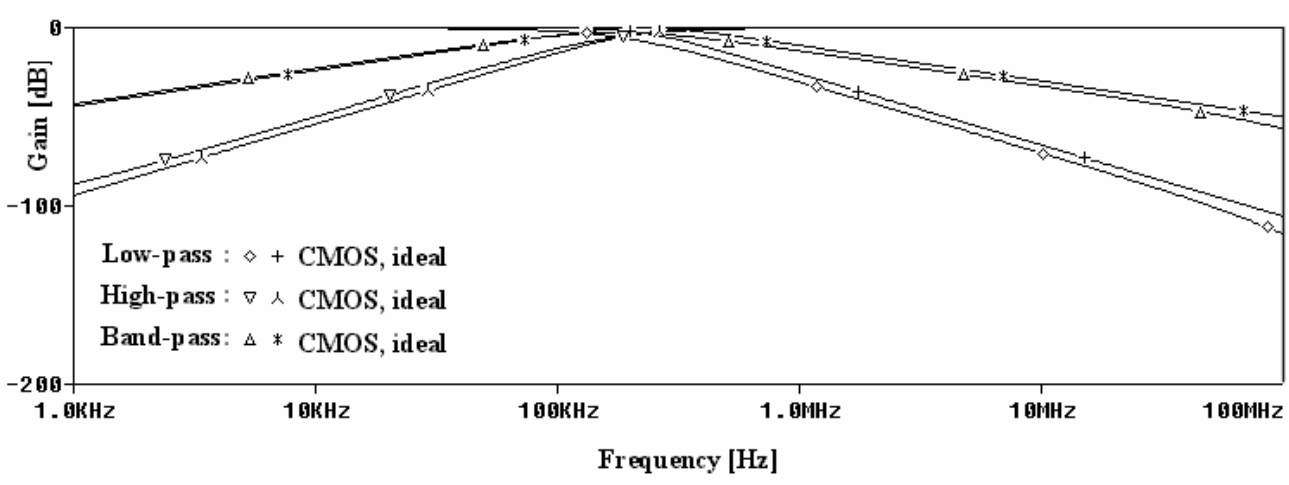

Figure 4. Gain-frequency characteristic of the low-pass, high-pass, and band-pass outputs

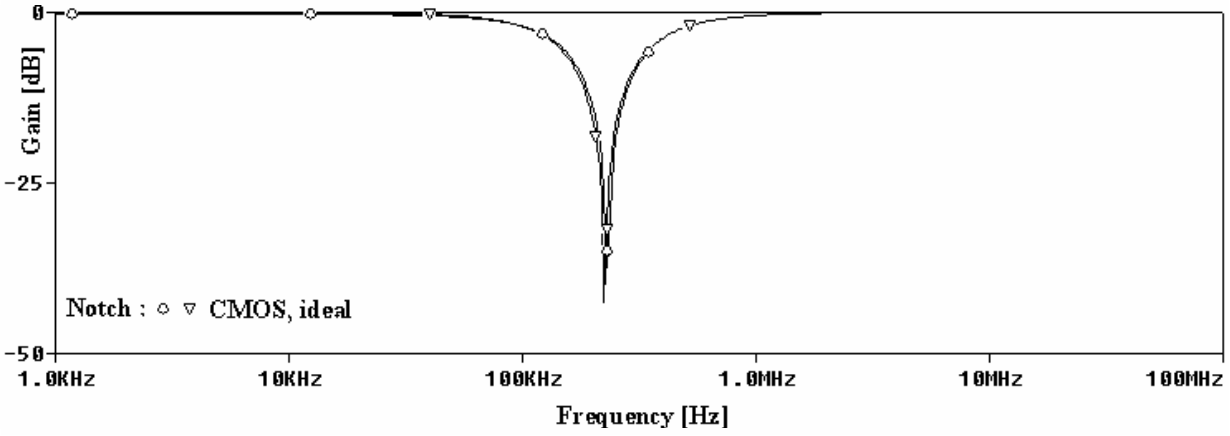

Figure 5. Gain-frequency characteristic of the notch output

REFERENCES

1. C. Toumazou, F. J. Lidgey, D. Haigh, Analog IC design: The current-mode approach. Exeter, UK: PeTer Peregrinus, 1990.
2. B. Wilson, Recent developments in current conveyors and current-mode circuits, Proc. IEE Pt. G 137, pp. 63-77, 1990.
3. C. Toumazou, F. J. Lidgey, Universal active filter using current conveyors, Electronics Letters 22, pp. 662-663, 1986.
4. C. A. Papazoglou, C. A. Karybakas, Noninteracting electronically tunable CCII-based current-mode biquadratic filters, IEE Proceedings-Circuits Devices Systems 144, pp. 178-184, 1997.
5. S. Ozoguz, A. Toker, O. Cicekoglu, High output impedance current-mode multifunction filter with minimum number of active and reduced number of passive elements, Electronics Letters 34 (19), pp. 1807-1809, 1998.
6. M. T. Abuelma'atti, N. A. Tasadduq, A novel three inputs and one output universal current-mode filter using plus-type CCIIs, Microelectronics Journal (30), pp. 287-292, 1999.
7. U. Cam, O. Cicekoglu, A. Toker, H. Kuntman, Current-mode high output impedance multifunction filters employing minimum number of FTFNs, Analog Integrated Circuits and Signal Processing, 28, pp. 299-307, 2001.
8. A. Sedra, K.C. Smith, A second generation current conveyor and its applications, IEEE Trans., CT-17, pp. 132-134, 1970.
9. W. Chiu, S. I. Liu, H. W. Tsao, J. J. Chen, CMOS differential difference current conveyors and their applications, IEE Proc. Circuits Devices Syst. 144, pp. 91-96, 1996.
10. H. O. Elwan, A. M. Soliman, Novel CMOS differential voltage current conveyor and its application, IEE Proc. Circuits Devices Syst. 144, pp. 195-200, 1997.
11. H. Sedef, C. Acar, A new floating inductor circuit using differential voltage current conveyors, Frequenz, vol. 54, pp. 123-125, 2000.
12. H. Sedef, C. Acar, A new floating FDNR circuit using differential voltage current conveyors, Int. J. Electronics and Communications, AEÜ, vol. 54, pp. 297-301, 2000.
13. S. S. Gupta, R. Senani, Grounded capacitor current-mode SRCO, Novel application of DVCCC, Electronics Letters, 36, pp. 195-196, 2000.
14. T. Dostal, D. Biolek, K. Vrba, Adjoint voltage-current mode transformation for circuits based on modern current conveyors, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, 2002.
15. S. Minaei, Ç. Temizyürek, Dual input all-pass filter using DVCC, International Symposium on Signals, Circuits & Systems (SCS), Iasi, Romania, 2003.